Dead Bugging a Passive 2nd-Order Sigma-Delta Modulator for Low-Power ADC

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Objective:

The purpose of this project is to dead bug and test a passive 2nd-order sigma-delta modulator for low-power analog-to-digital conversion.

Equipment Used:

Soldering Iron

Wire

Copper Board

Three (3) Banana Jacks

Three (3) Banana Jack Cables

Two (2) BNC Jacks

Two (2) Coaxial Cables

One (1) 1x Probe

LT 1671 Comparator Chip

One (1) 500kΩ Resistors

Two (2) 100kΩ Resistors

Two (2) 10kΩ Resistors

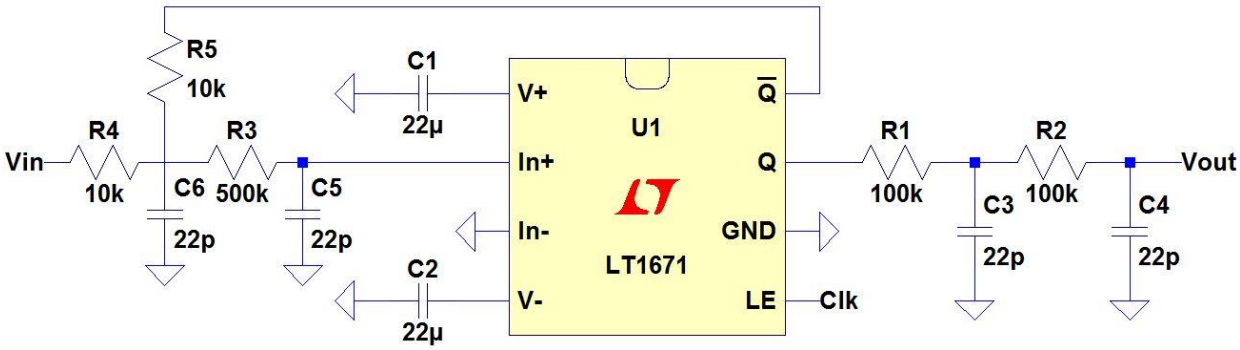
Two (2) 22uF Capacitors

Four (4) 22pF Capacitors

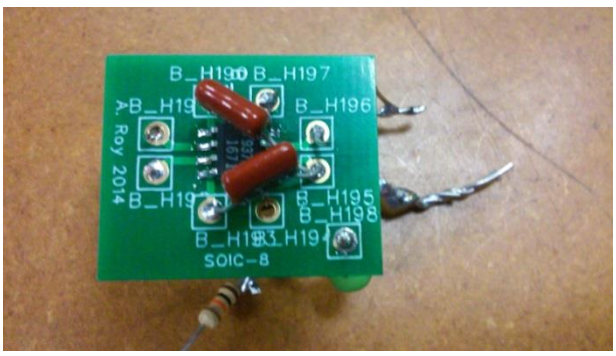
Background:

Improved resolution for sigma-delta modulation in analog-to-digital conversion has been researched in "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion" in which Angsuman Roy and R. Jacob Baker explore the addition of a passive second-order RC filter circuit to a sigma-delta modulator used for low-power analog-to-digital conversion.

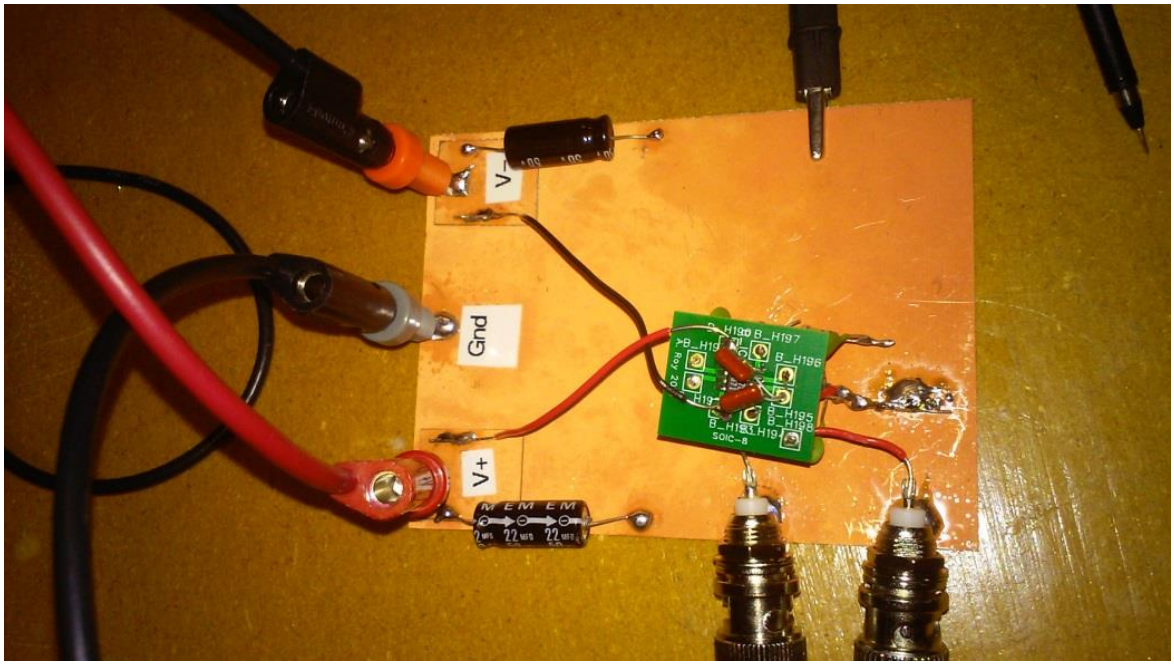
2nd-Order Sigma-Delta Modulator Circuit for Low-Power ADC



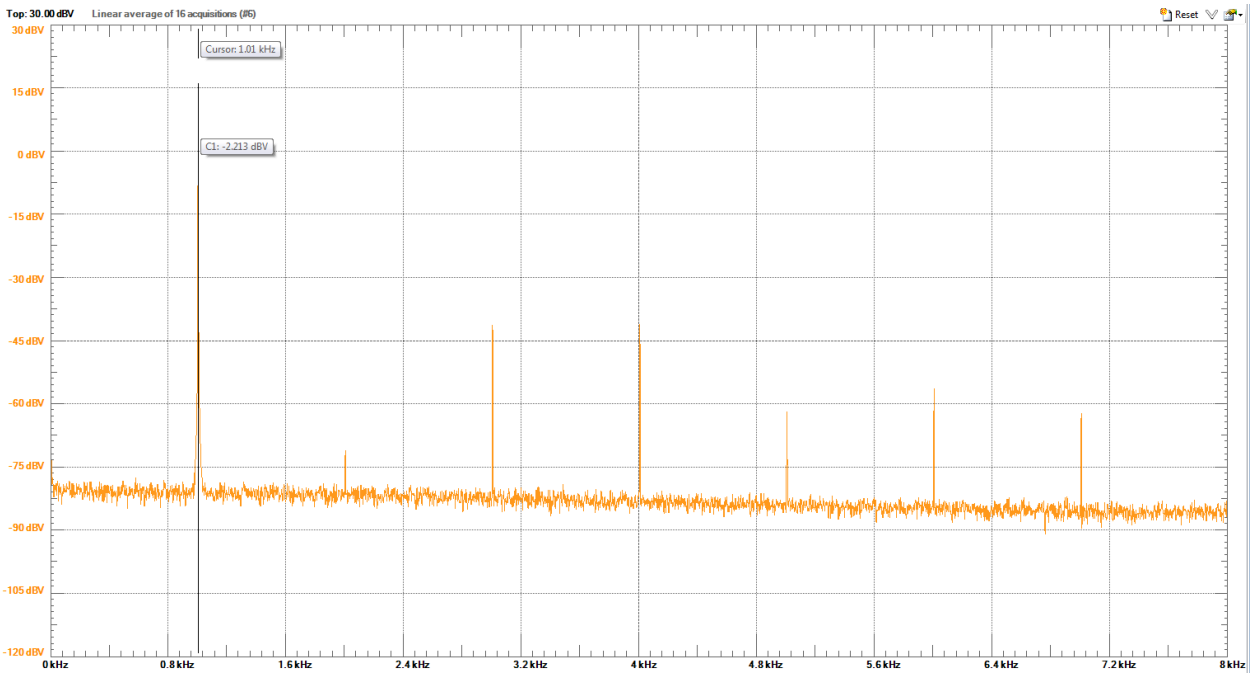
LT 1671 Comparator Chip w/ Soldered Resistor & Capacitor Components



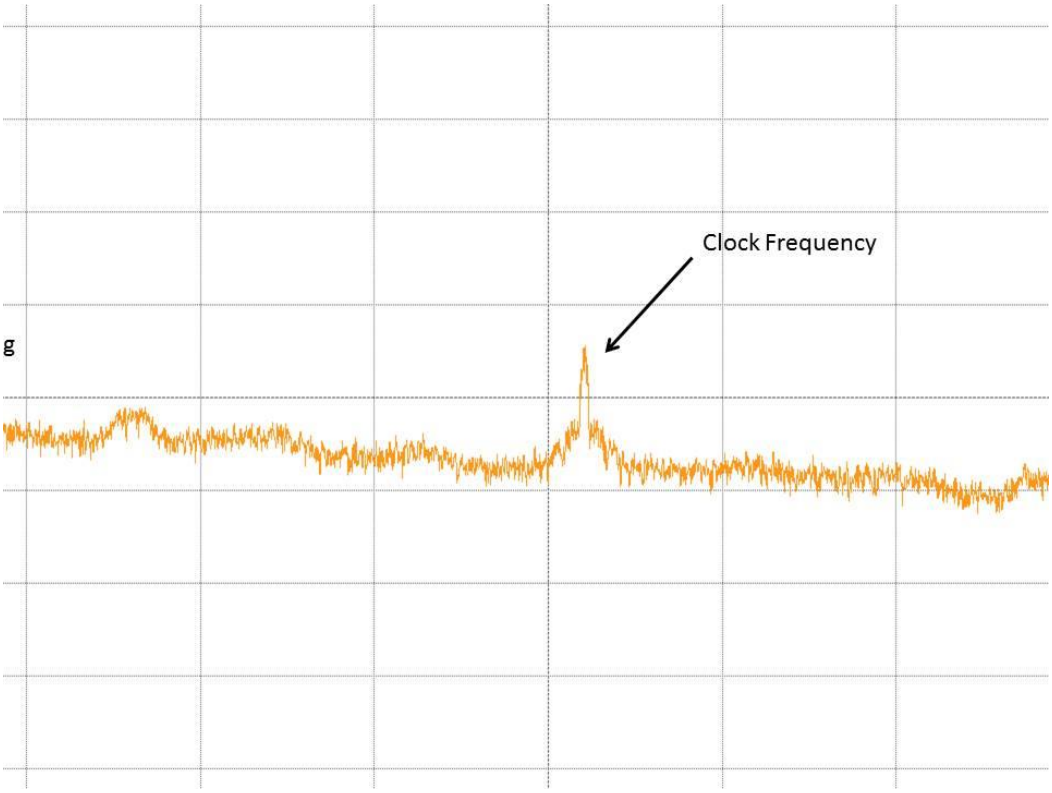
Testing of Passive 2nd-Order Sigma-Delta Modulator Circuit for Low-Power ADC



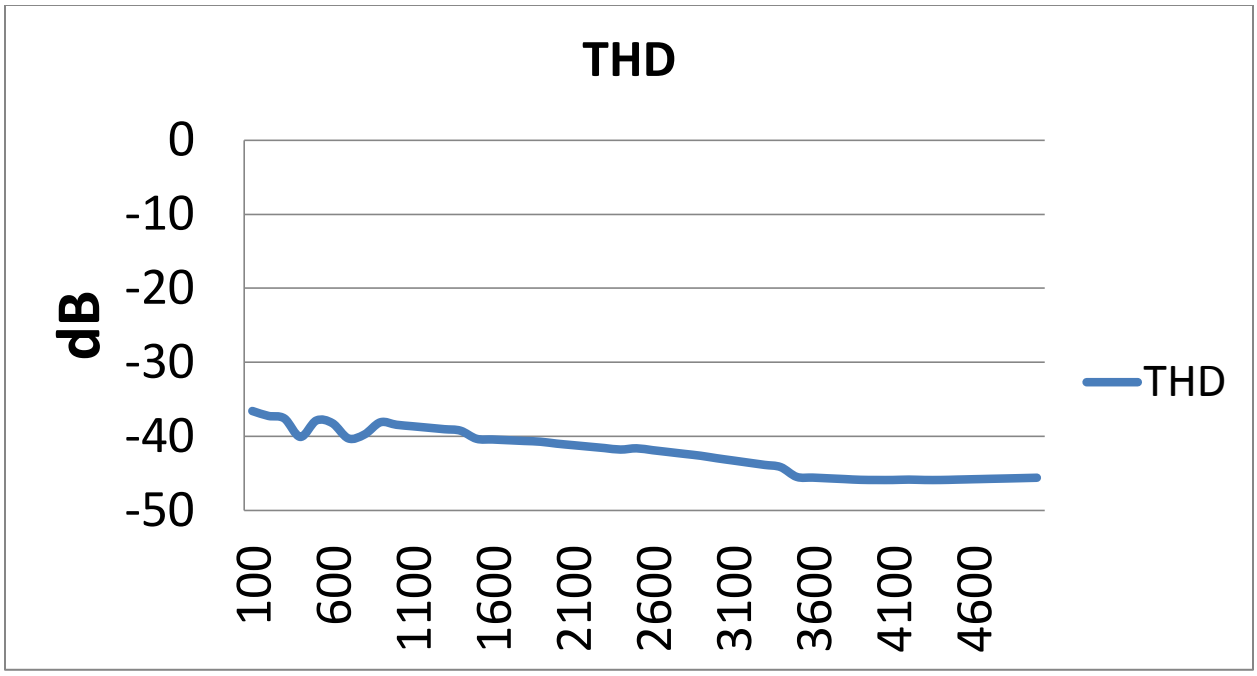
Fast Fourier Transform (FFT) – Total Harmonic Distortion (THD)



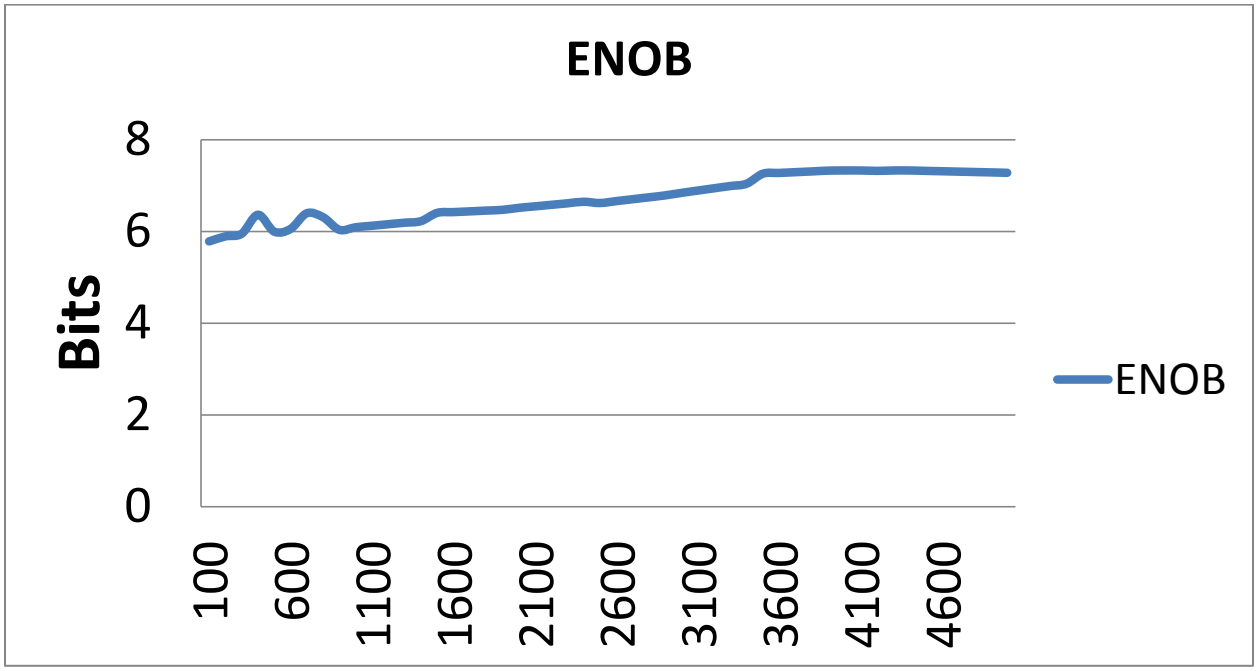
Noise Shaping Displaying Clock Frequency



Graph of Total Harmonic Distortion (THD)



Graph of Effective Number of Bits (ENOB)



Conclusion:

The dead bugged circuit of a passive 2nd-order sigma-delta modulator for low power analog-to-digital conversion performs well as expected and has resulted in accurate and useful data. The graph of Effective Number of Bits (ENOB) suggests the 2nd-order sigma-delta modulator acts as an approximately 7-bit data converter.

Resources:

[1] R. J. Baker and A. Roy, "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion," *IEEE 2014.* (2014): 595-598.