ECG 720 Advanced Analog IC Design
Course Project
Transimpedance Amplifier
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Introduction

The objective of this project is to design a TIA (Transimpedance Amplifier) with two stage gain. The first stage gains equal to 30k and the second stage gain between 10-20, and a bandwidth of at least 250MHz. The main reason for those parameters is because the current going into the input of the TIA is representing the current from an APD (Avalanche Photomultiplier). The sensitivity of the APD requires for high gain and a fast bandwidth.

Design Parameters

- Total gain: First Stage – 30kΩ (Transimpedance amplifier, TIA) and Second Stage 10–20x V/V
- Study of the need for inclusion of a 2nd stage
- TIA Bandwidth minimum of 250 MHz
- Input referred noise: < 5 pA/√Hz but preferably 1.5 pA/√Hz
- 1.5 – 2 V output swing
- 3.3 or 5 V power supply operation with less than 5 mA current consumption
- Amplifier output signal is designed to drive high impedance loads (use 1 pF)
- Slew–rate with maximum load > 100V/microsecond = 100 mV/nanosecond

Table of Basic parameters of complete design

Quiescent Current	2.2mA		
VDD=5	Out swing	Slew rate	
5u input current, 1pF load, no parasitic cap	2.349V	1.3V - rise	770mV - fall
10u input current 1pF load, no parasitic cap	2.6V	1.68 - rise	710mV - fall
	Gain	Bandwidth	Noise performance
With 100f parasitic			
1pF - 5pF	110dB	256MHz – 110MHz	$\frac{857fV}{\sqrt{Hz}}$ to $\frac{1.88pV}{\sqrt{Hz}}$
With 200f parasitic			
1pF – 5pF	110dB	125MHz – 94MHz	$\frac{857fV}{\sqrt{Hz}}$ to $\frac{1.64pV}{\sqrt{Hz}}$
With 300f parasitic			
1pF – 5pF	110dB	94MHz – 79MHz	$\frac{857fV}{\sqrt{Hz}}$ to $\frac{1.72pV}{\sqrt{Hz}}$
With no parasitic			
1pF – 5pF	110dB	360MHz – 112MHz	$\frac{857fV}{\sqrt{Hz}}$

The first TIA Topology (not using)

The first TIA topology used is the one below, however, the output from the second stage could not reach the required bandwidth. The second stage is a common source amplifier, and its output goes into source follower. Even though this topology seems solid and robust the output did not meet the specifications. Increasing the vgs and vsg did help increase the overall speed until the bandwidth was reached, however the gain was killed, and it was pointless to keep moving things around. This is a good example of industry trade off. As the overdrive increases the gain decreases. Minimum L also helps with the speed, but the all the mosfets are already using minimum L (600n). So, diff-amp topologies were selected for the first stage and second stage.

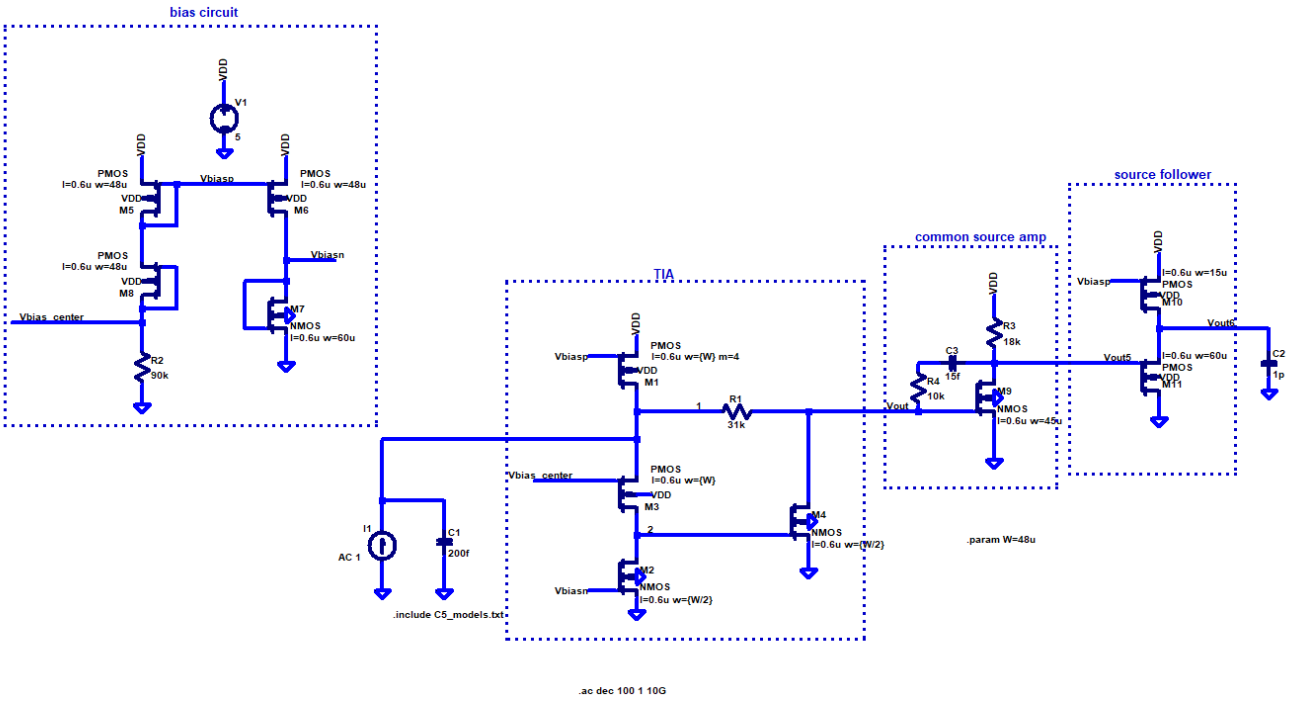

Figure 1 First TIA topology (did not meet requirements)

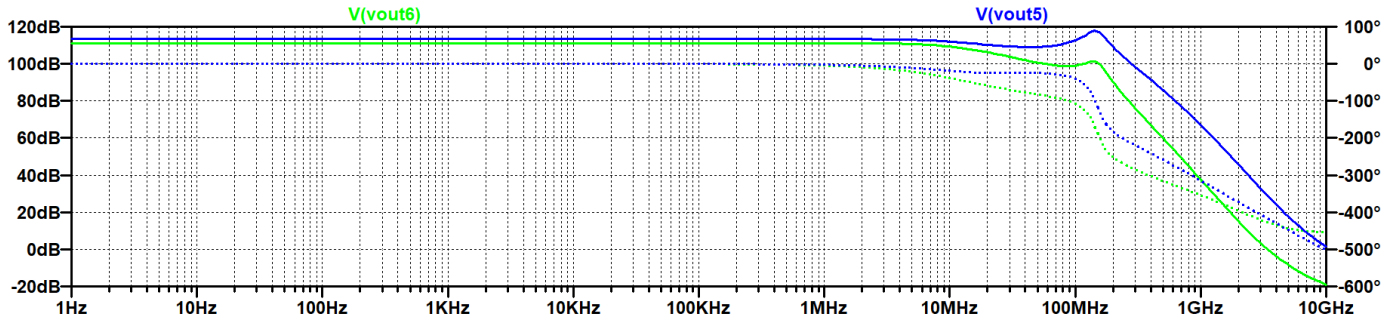

Figure 2 simulation of first TIA, from fig. 1

First Stage (TIA)

A NMOS diff-amp for the first was chosen and the biasing voltages were chosen in respect to simulation results. According to the C5 models text file the threshold voltage for the NMOS and PMOS are 0.6696061V and -0.9214347. Thus, a couple batteries with different ranges were simulated to obtain a decent biasing circuit. Then from there a biasing circuit was designed to give those simulated values. The gain is a little low in order to increase the bandwidth on the last stage.

Below are the schematic and the AC analysis simulation with the biasing circuit selected. The bandwidth shown on the plot is about 619MHz.

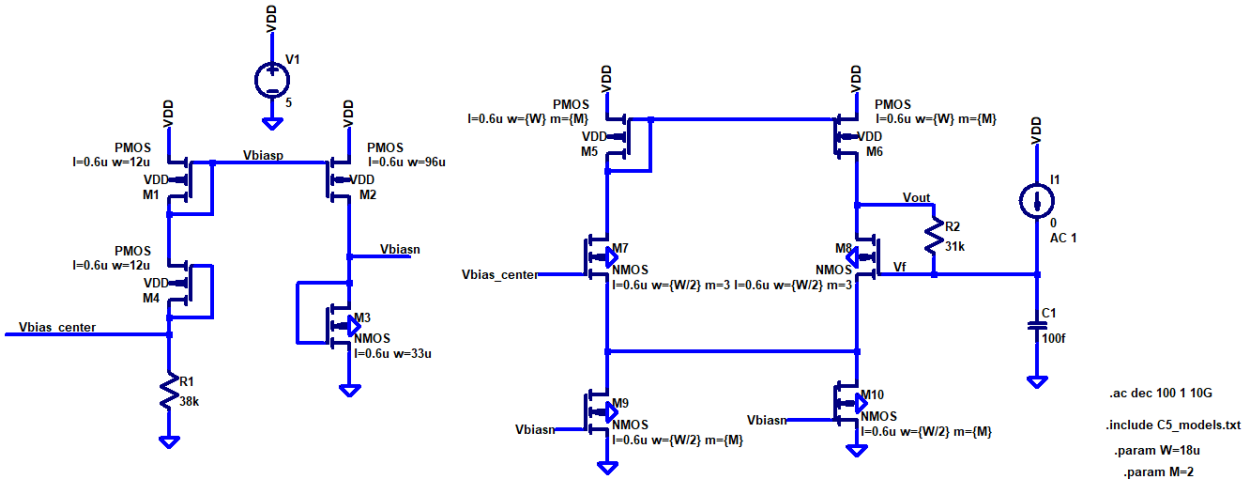

Figure 3 TIA used for this project, diff-amp topology

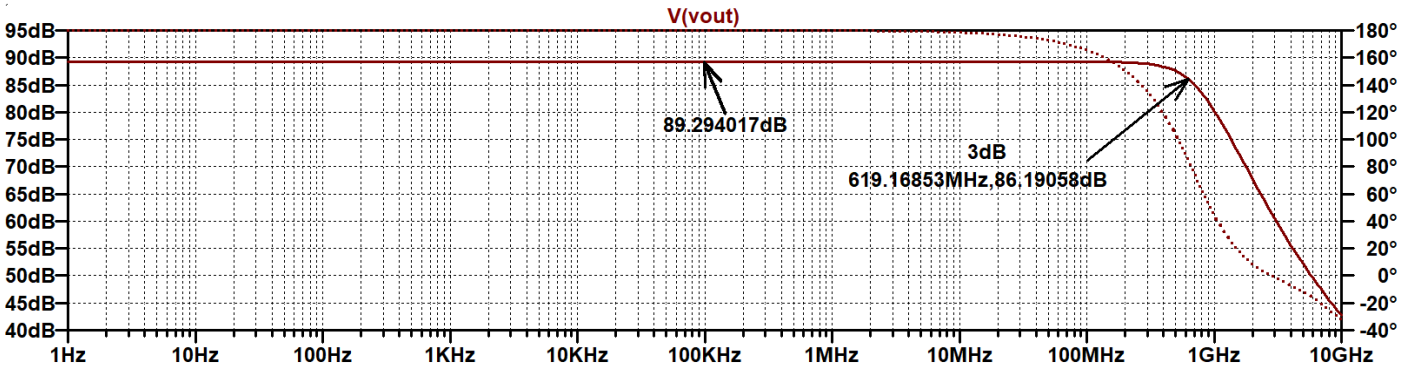

Figure 4 AC simulation of fig. 3

A DC sweep with the current was formulated and taken the derivative of the output in order to see the gain in ohms. The output gain shows a little smaller than is required but this value was used to maximize the bandwidth.

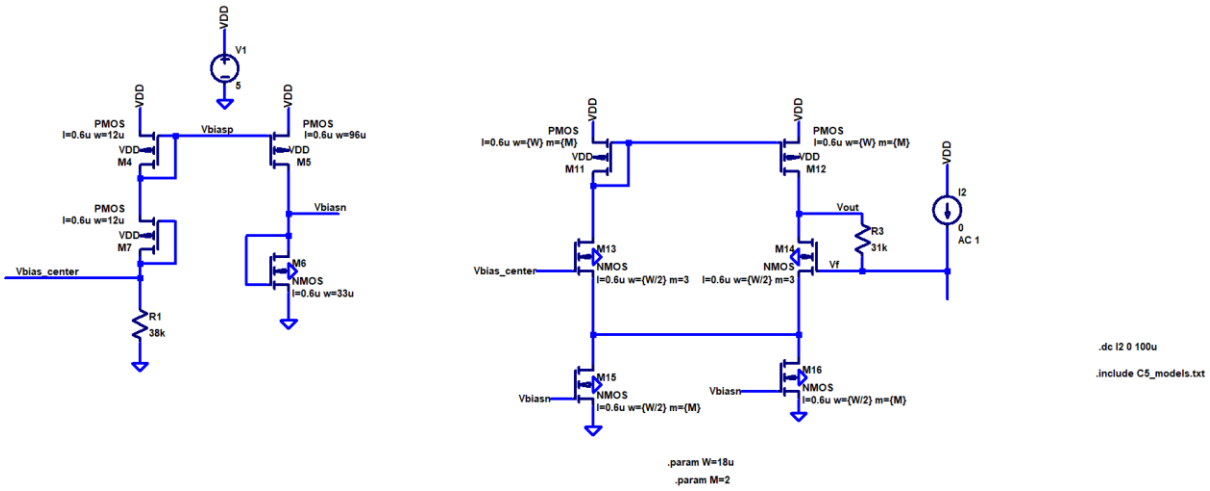

Figure 5 applying a sweep to the current source representing APD

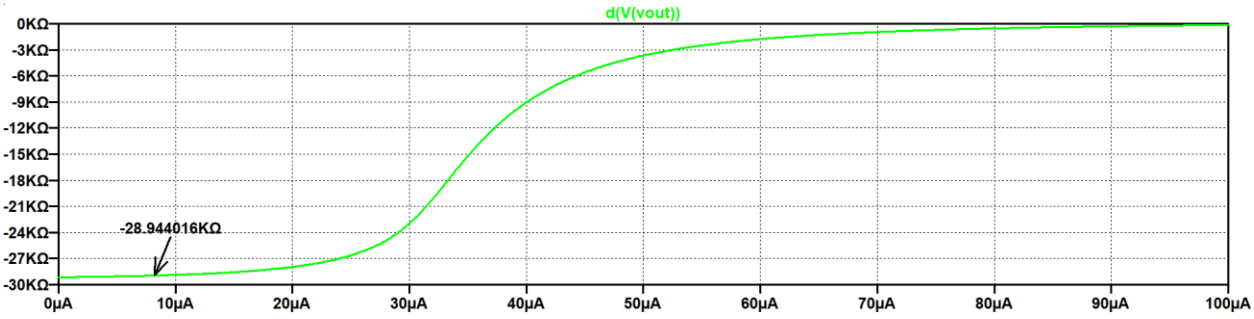

Figure 6 simulation of fig. 5 showing the gain.

Open Loop and Closed loop Gain of TIA

Here we are checking the open loop and close loop gain. The Gm of each devices keep changing in respect to the current and widths. The Transconductance was chosen from the error log. This value along with the formula below was used to calculate the open loop gain (AOL).

$$vgs14 = \frac{(\text{Iin})R_{feed}}{2}, \qquad id14 = (vgs14)(gm14)\,, \qquad Vout = (id14)(r_{op}||r_{on})$$

$$AOL = \frac{\text{Vout}}{\text{Iin}} = \frac{R_{feed}}{2}(gm14)(r_{op}||r_{on})$$

Name:	m16	m15	m14
Model:	nmos	nmos	nmos
Id:	3.26e-04	3.26e-04	3.16e-04
Vgs:	1.07e+00	1.07e+00	1.18e+00
Vds:	1.13e+00	1.13e+00	1.18e+00
Vbs:	0.00e+00	0.00e+00	-1.13e+00
Vth:	6.15e-01	6.15e-01	8.34e-01
Vdsat:	3.02e-01	3.02e-01	2.63e-01
Gm:	1.26e-03	1.26e-03	1.76e-03
Gds:	3.93e-05	3.93e-05	4.31e-05

Name:	m12
Model:	pmos
Id:	-3.91e-04
Vgs:	-1.38e+00
Vds:	-2.69e+00
Vbs:	0.00e+00
Vth:	-8.77e-01
Vdsat:	-4.13e-01
Gm:	1.26e-03
Gds:	3.82e-05

$$AOL = \frac{\text{Vout}}{\text{Iin}} = \frac{31\text{k}}{2}(1.76m)\left[\frac{1}{38.2u}||\frac{1}{23201u}\right] \simeq 335.5k\Omega$$

The simulation below shows the open loop gain, which is somewhat off from what was calculated above.

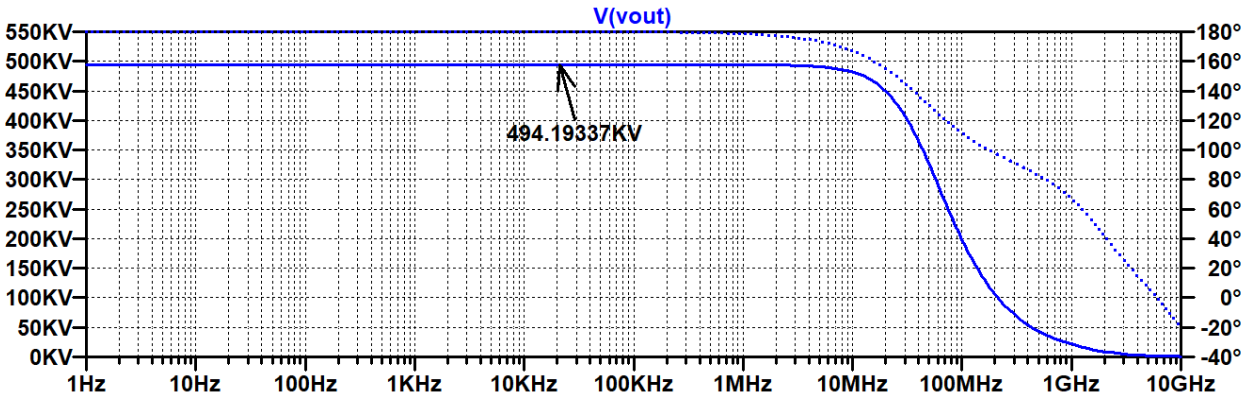

Figure 7 simulation of fig. 5 showing open loop gain

The AOL value was used to calculate the closed loop gain using the formula below.

$$ACL = \frac{AOL}{1 + \beta \mathrm{AOL}}$$

$$ACL = \frac{335.5k}{1 + \frac{1}{31k}(335.5\mathrm{k})} \simeq 28377\Omega$$

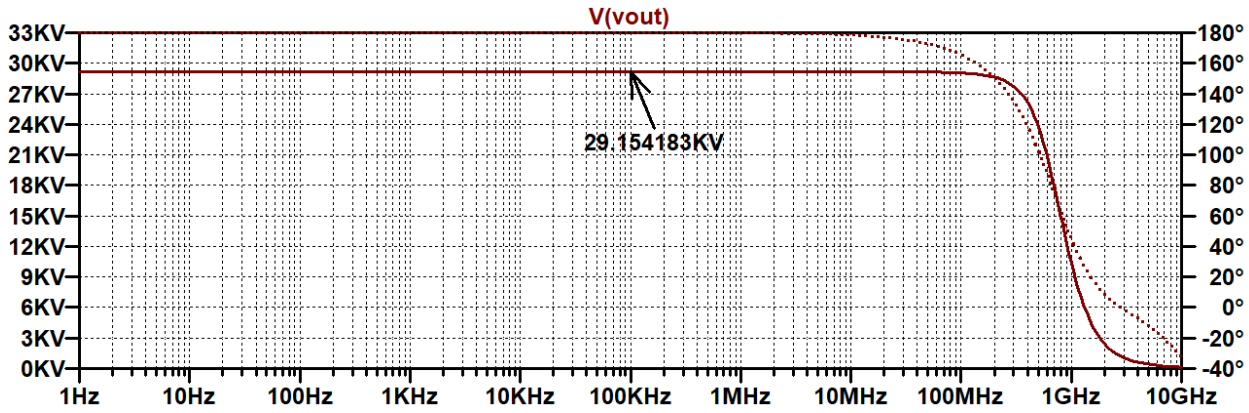

Figure 8 simulation of fig. 5 showing the closed loop gain

Below shows the transient analysis from Vout1, output of the TIA. This was done from the complete design. It seems there's noise and instability.

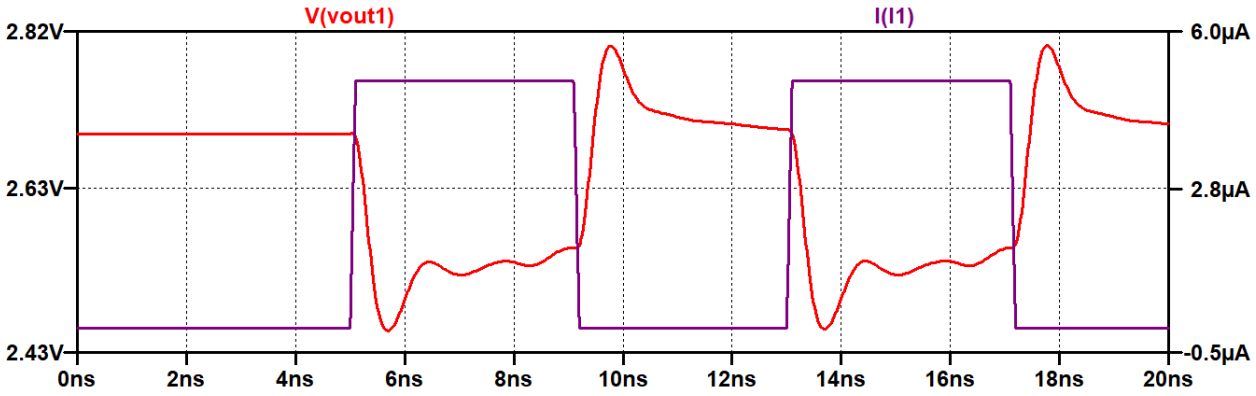

Figure 9 transient simulation of Vout1, TIA, of complete design

Second stage (diff-amp) voltage amplifier with Source follower

The second stage diff-amp was chosen by first using the same values as the previous diff-amp and changed those values a few times to obtain the appropriate gain. The Same biasing circuit was used to bias this second diff-amp. The formula below can be used to calculate the output of this amplifier. The source follower was selected in order to drive the 1pF load. The source follower could bring the gain down by certain amount, but it boosts up the speed.

$$\frac{\text{Vout}}{\text{Vin}} = (g_{mn})[(r_{op}||(r_{on}]$$

$$\frac{\text{Vout}}{\text{Vin}} = (1.23m)[\frac{1}{30u}||\frac{1}{29u}] \simeq 20.8V/V$$

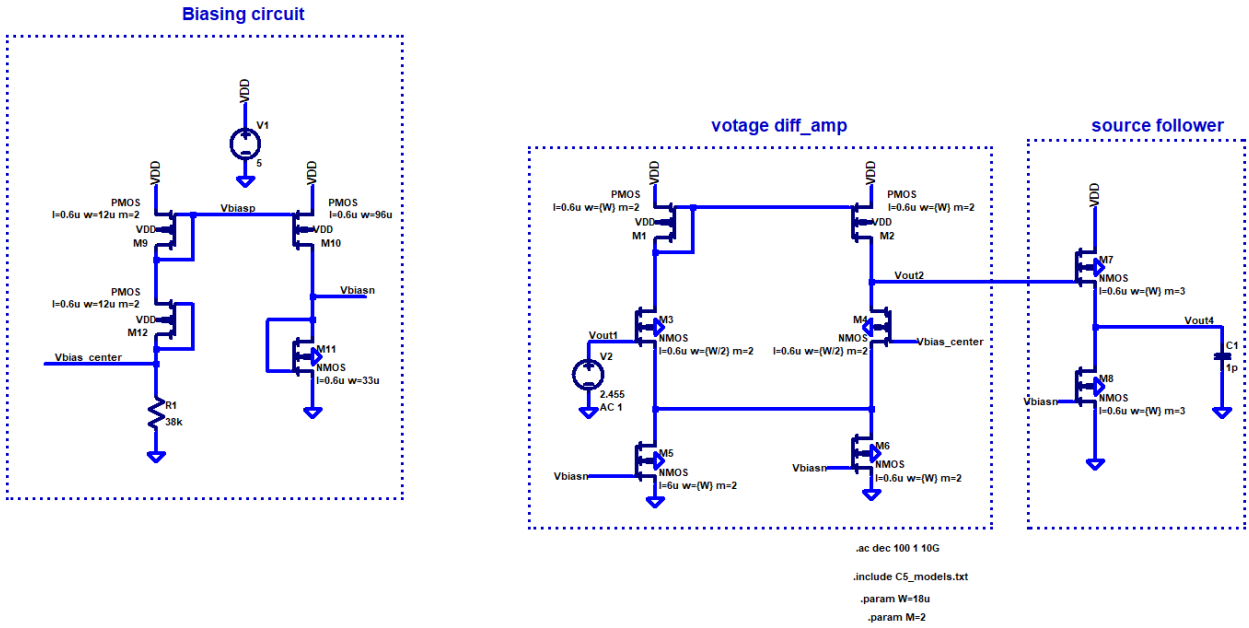

Figure 10 testing the gain of the second stage diff-amp with source follower

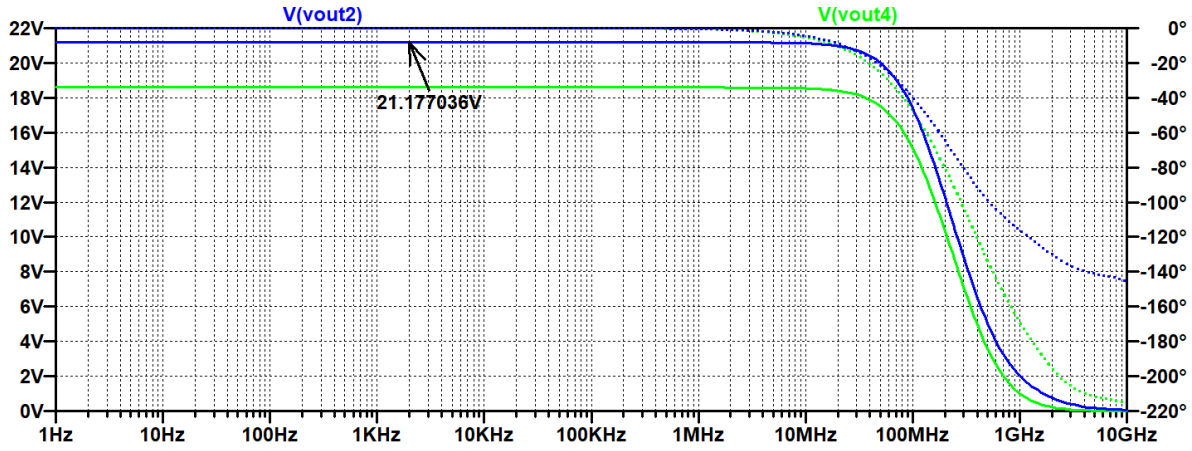

Figure 11 simulation of fig. 9 showing the output gain of the diff-amp and the output of the source follower

Complete Design

The complete design is a diff-amp TIA (first stage) with a Voltage amplifier diff-amp (second stage) and a source follower on the second stage output. Fig. 13 shows the gain and bandwidth of this circuit. The gain 110dB is about 300kV and the 3dB is about 371MHz

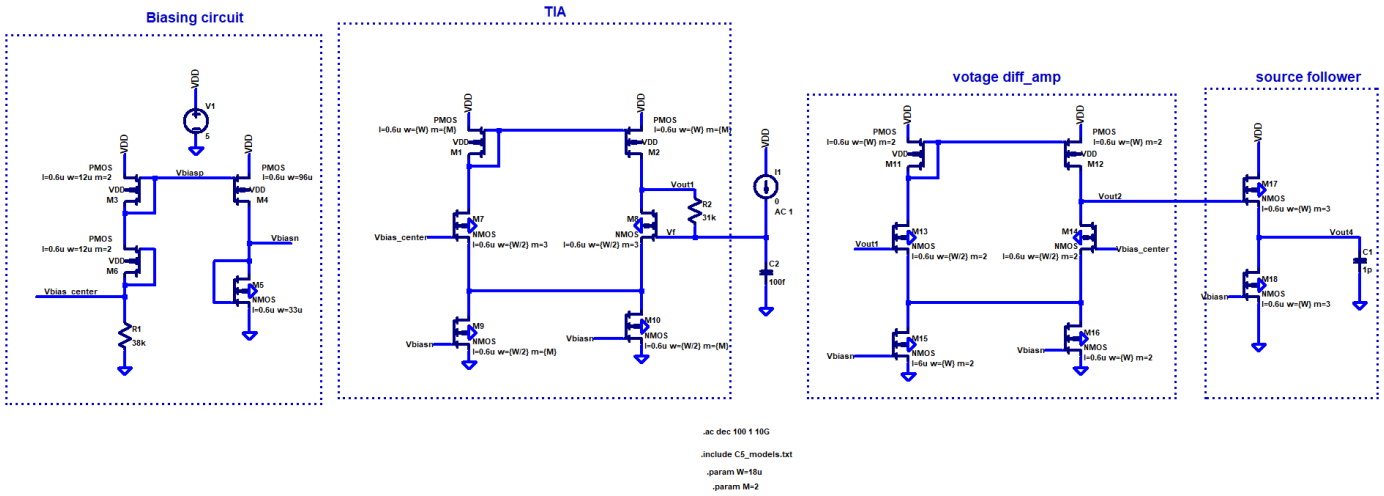

Figure 12 complete project design

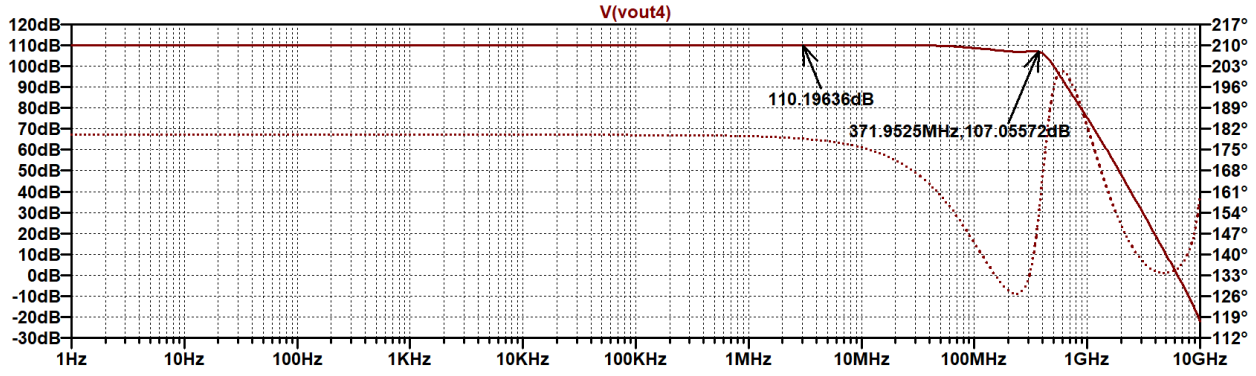

Figure 13 simulation of fig. 12 complete design. Voltage tested is Vout4, output of system.

Setting Time

Here the settling time for the first stage output (TIA) and for Vout4, the output of the system, were tested with different size loads. First, the system was tested with no load, with 1pF load and then with different size loads.

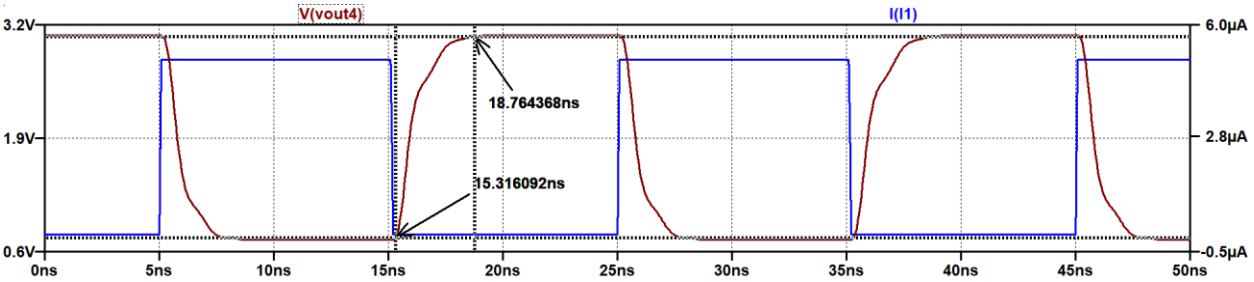

Figure 14 output settling time of complete design. Simulation with no load

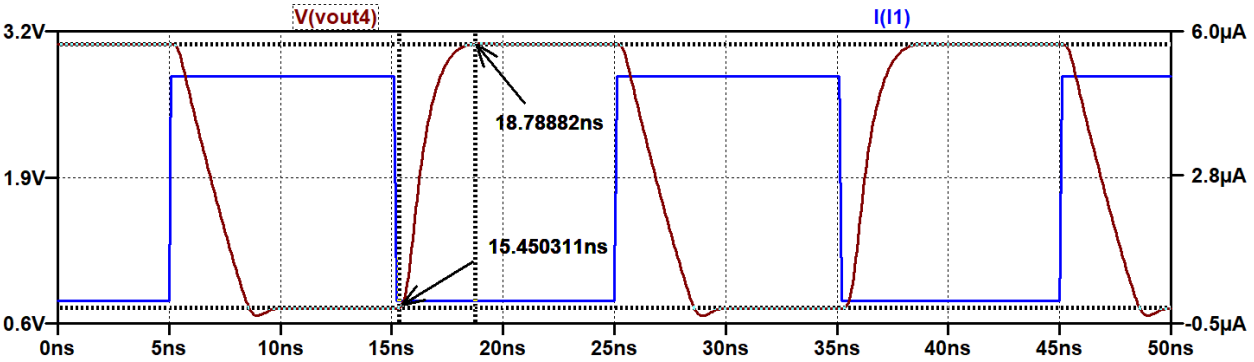

Figure 15 output settling time of complete design. Simulation with 1pF load

The simulation below shows how the output falling time keeps increasing dramatically as the load increases. Perhaps a buffer could help in this situation.

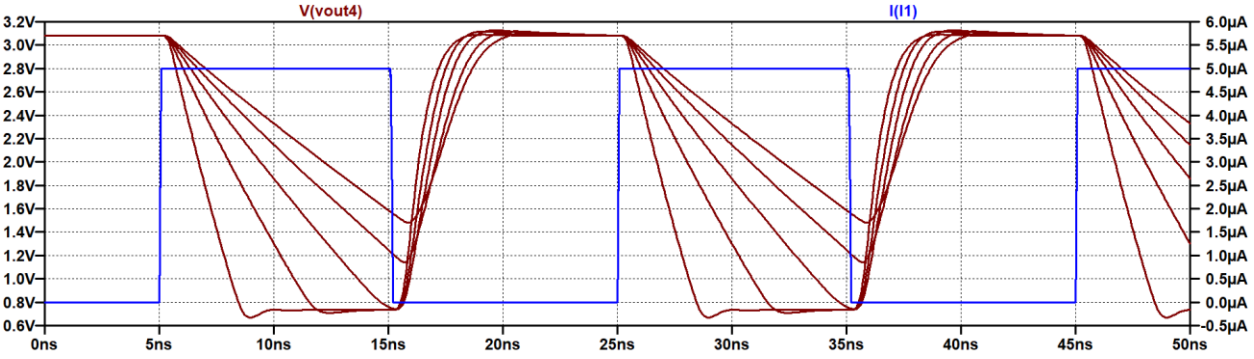

Figure 16 output settling time with different size loads (1pF -5pF)

Slew Rate

The slew rate was tested with 1pF load since the fall increases rapidly with increasing load. For the rise time is about 1.3V per nanosecond, and for the fall time is about 770mV per nanosecond. This slew rate seems to be with the parameters for this design. However, the APD parasitic capacitance needs to be added, which is the next step.

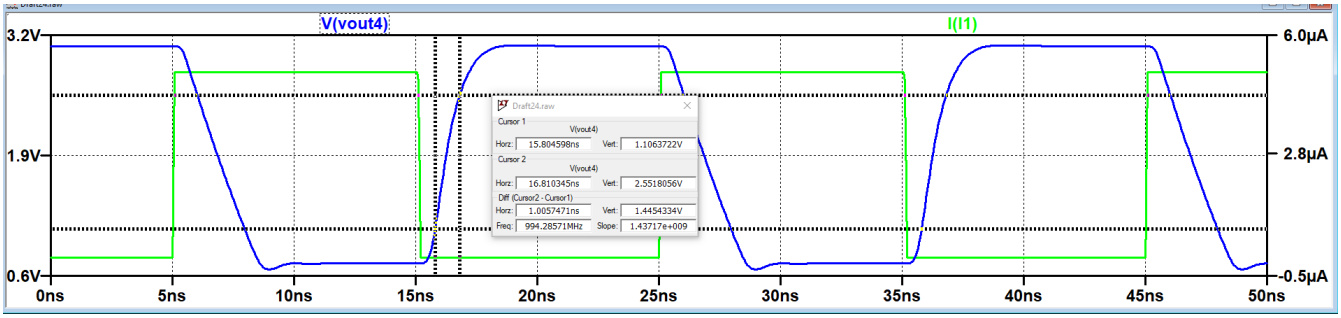

Figure 17 simulation showing slew rate, rise, 1pF load

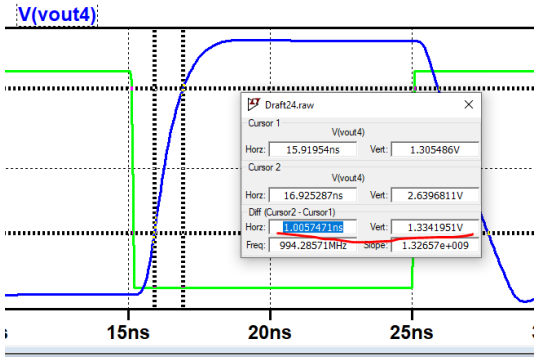

Figure 18 slew rate close-up

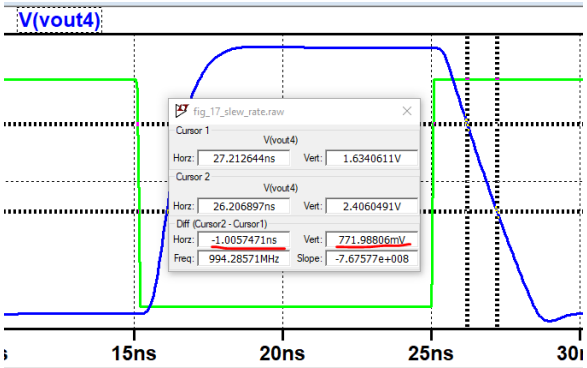

Figure 19 slew rate close-up

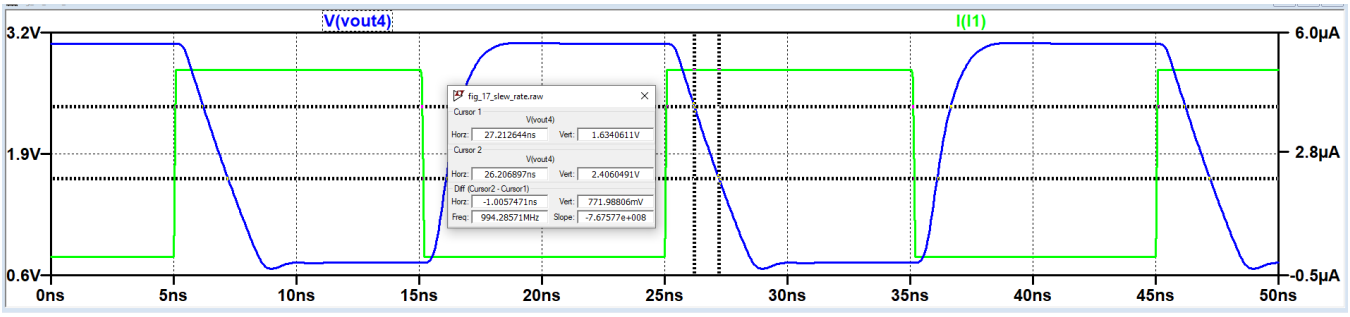

Figure 20 simulation of slew rate, fall, 1pF load

Before parasitic capacitance is added a simulation for the output voltage made with input current of 5u to make sure that the minimum output voltage swing of 1.5V is achieved.

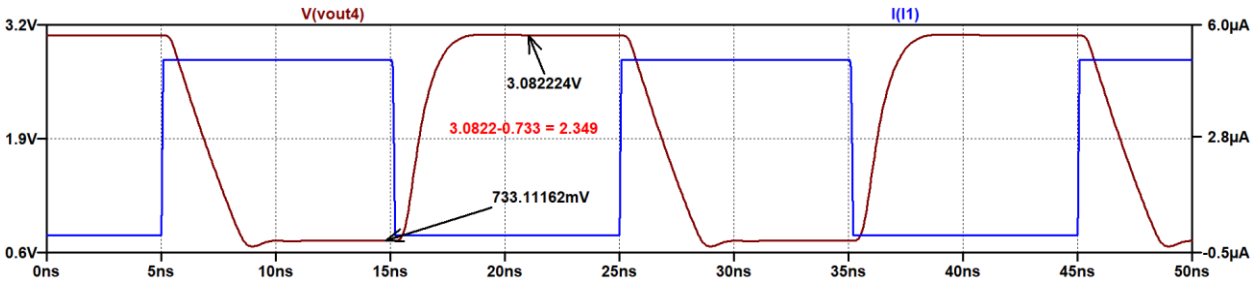

Figure 21 simulation to inspect minimum output voltage with 5u input current, 1pF load

Simulations with APD Added Parasitic Capacitance

First AC analysis is performed with different loads (1pF-5pF) to see the change in gain and bandwidth. The figure below shows those changes and for the gain there are no changes, it stays at 110dB. However, for the bandwidth it changed from 256MHz at 1pF to 110MHz at 5pF

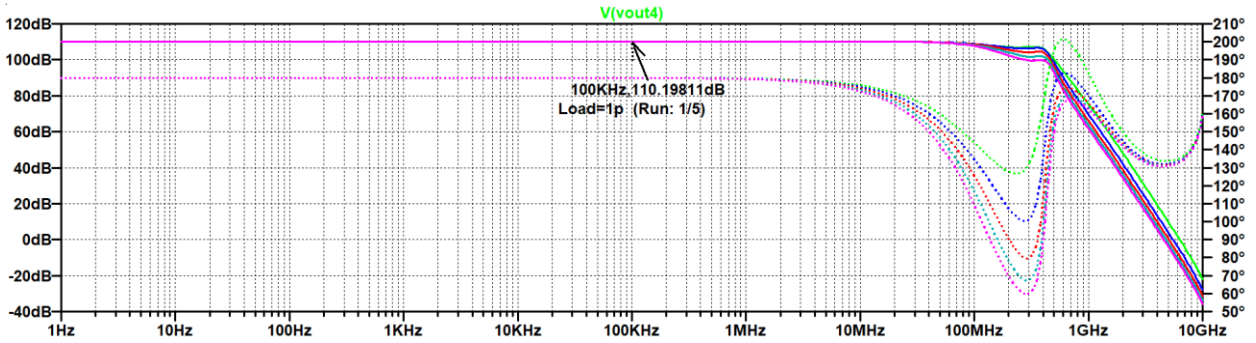

Figure 22 simulation of gain and bandwidth changes as the load increases from 1pF to 5pF

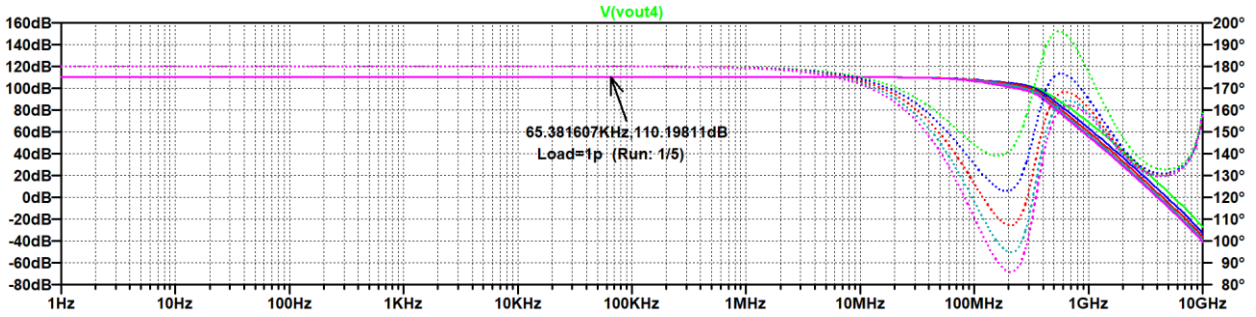

Figure 23 simulation of gain and bandwidth changes as the load increases from 1pF to 5pF, 200f parasitic

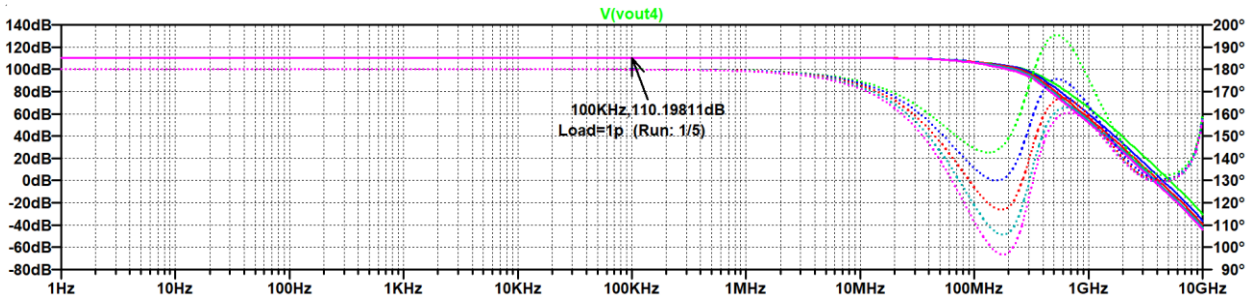

Figure 24 simulation of gain and bandwidth changes as the load increases from 1pF to 5pF, 300f parasitic

Noise Performance

The next few simulations the output noise is being divided by the gain to obtain the input referred noise.

The first simulation is 100f parasitic capacitance and 1pF load. The maximum noise of 1.88pV/Hz^2 comes at 372MHZ

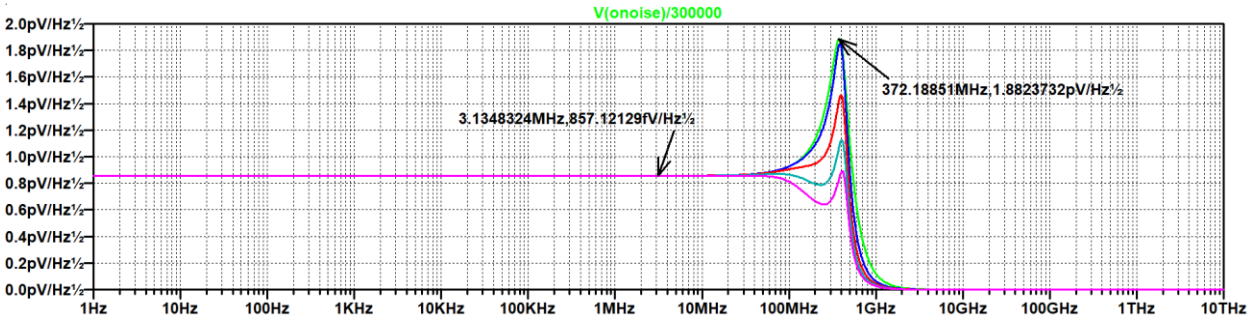

Figure 25 input referred noise, 100f parasitic and load (1p-5p)

The second simulation is adding noise to fig. 23 to see how the noise behaves with 200f parasitic and changes in load from 1p-5p.

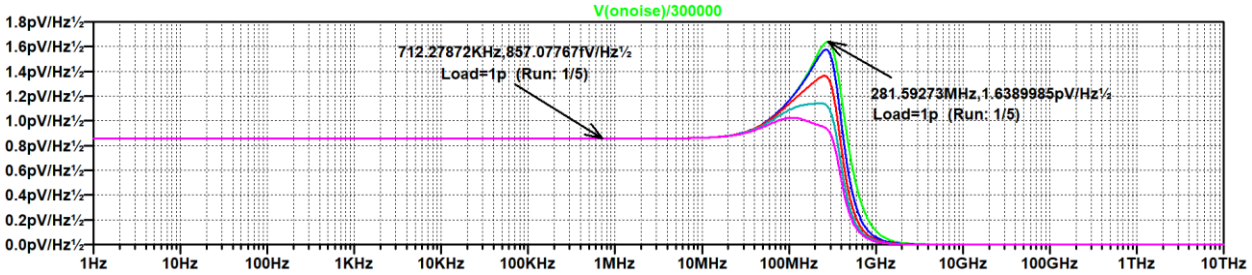

Figure 26 input referred noise, 200f parasitic and load (1p-5p)

The third simulation is adding noise to fig. 24 to see how the noise behaves with 300f parasitic and changes in load from 1p-5p.

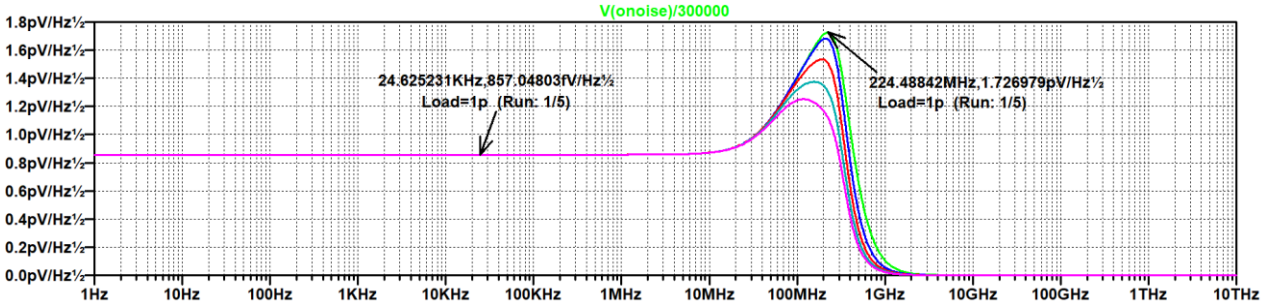

Figure 27 input referred noise, 300f parasitic and load (1p-5p)

The fourth simulation the same as the previous before except no APD parasitic capacitance.

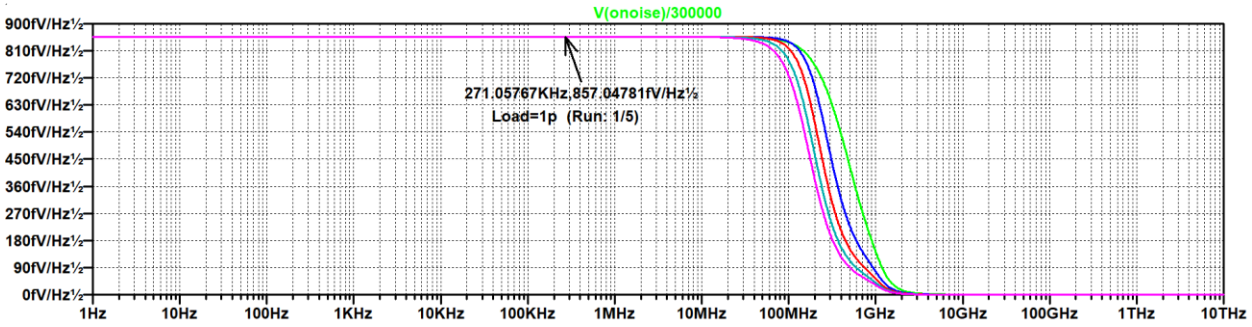

Figure 28 input referred noise, no APD parasitic capacitance and load (1p-5p)

Current Consumption (Quiescent current)

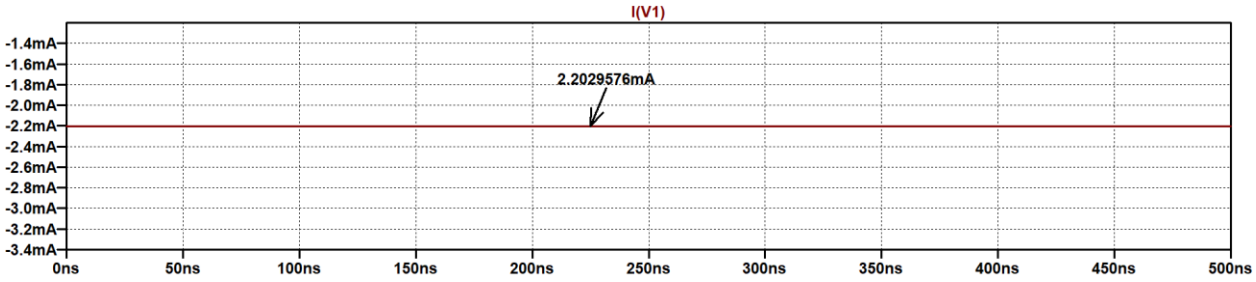

Figure 29 simulation showing quiescent current

Note: The transient analysis simulations were performed earlier without the parasitic capacitance, but now several of those values were added to see the difference. These are re-simulations from fig. 15 to see how the output behaves with APD capacitance

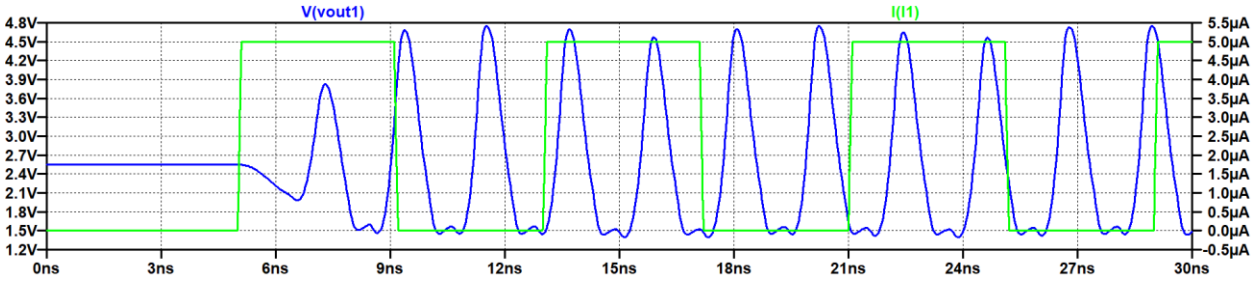

Figure 30 re-simulations from fig. 15 to see how the output behaves with 100f added capacitance

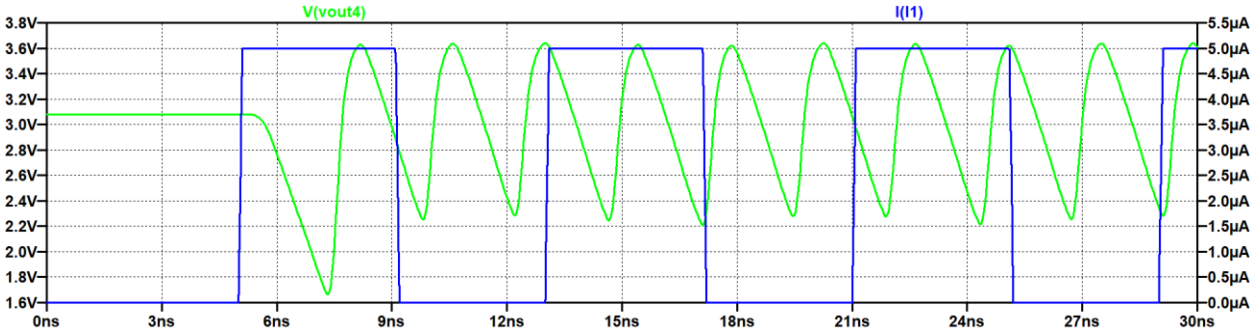

Figure 31 re-simulations from fig. 15 to see how the output behaves with 200f added capacitance

This shows that this is perhaps not the best design and probably not working as desired, even though the AC analysis seemed to show that.

The Study for the Need of the Second Stage

In this case a second stage is needed because of the gain and bandwidth requirement. Even if we can get a 300k to 600k gain from the first stage diff-amp amplifier, the bandwidth would be minimal, unless the desired bandwidth is small.

Conclusion

In conclusion the complete design provides for a gain of 300k and a bandwidth of 250MHz. A diff-amp TIA used as a first stage, a diff-amp voltage amplifier as second stage, and a source follower at the output of the second stage to drive the load. The output swing is above 1.5V. The quiescent current is 2.23mA. And the slew rate is between 700mV and 1V per nanosecond. However, adding parasitic capacitance to the current source (APD) with different values, it seems to break it. Thus perhaps this is not the best design. And spending too much time on the first topology which did not work was not the best option.