Low Voltage Op – Amp

On Semiconductor's 500nm process, C5 with two polysilicon layers and 3 levels of metal with a lambda of 300nm.

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May 2019

The following report details the design and simulation of a low voltage op amp that operates with VDD from 2V - 5V while driving 100pF maximum and 1k minimum load.

The requirements followed are DC open-loop gain > 66 dB under all load and VDD condition, Gain-bandwidth product should be > 1 MHz, CMRR > 90 dB at 100 kHz, PSRR > 60 dB at 1 kHz, Slew-rate with maximum load > 1V/microsecond.

The op-amp design goals were to have as high of a gain as possible, while maintaining a phase margin of 90 degrees for optimal stability and a first order step response mirroring that of an RC circuit. The design aimed to use smaller device sizes for a faster and more concise design and layout, minimal power dissipation and a minimum current.

Result Tables

DC Open Loop Gain

Power Supply Voltage (V)	Normal Load: 1k & 100pF	Larger Load: 100k & 100p
2	72 dB	78 dB
3	68.4 dB	74 dB
4	66 dB	71 dB
5	64 dB	68 dB

Gain Bandwidth Product

Power Supply Voltage (V)	Normal Load: 1k & 100pF	Larger Load: 100k & 100p
2	4.967MHz	4.72MHz
3	4.48MHz	4.37MHz
4	4.48MHz	4.37MHz
5	4.429MHz	4.37MHz

Common Mode Rejection Ratio (CMRR) at 100kHz

Power Supply Voltage (V)	No load (in units of dB)	Normal Load: 1k & 100pF (in units of dB)
2	93.412	95.494
3	109.512	95.629
4	94.84	104.84
5	87.169	93.47

Power Supply Rejection Ratio (PSSR) Plus at 1kHz

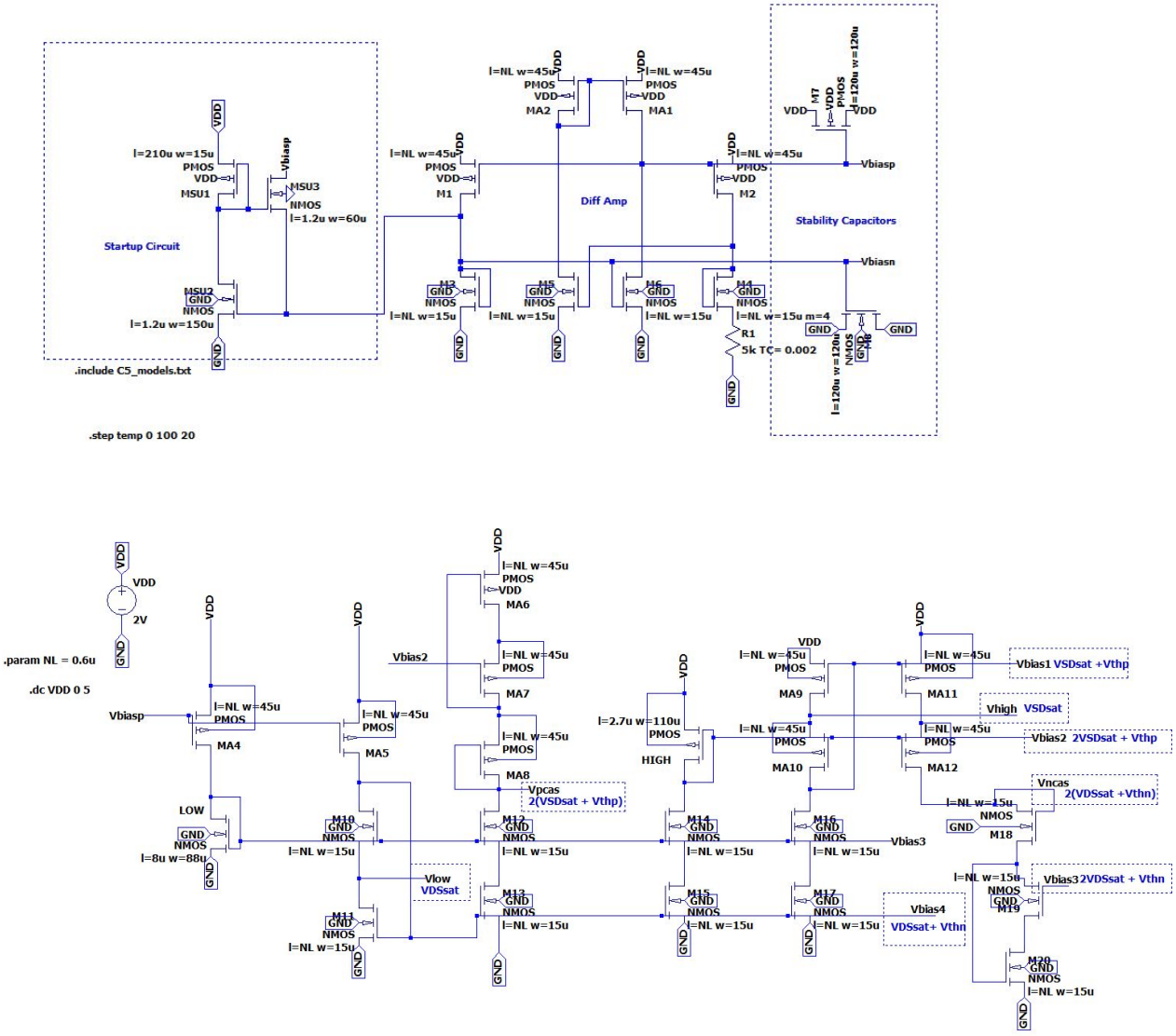
Power Supply Voltage (V)	Normal Load: 1k & 100pF	Larger Load: 100k & 100pF
2	87.86dB	77.11dB
3	79.38dB	75.6dB
4	76.1489dB	72.7dB
5	72.761dB	69.9dB

Power Supply Rejection Ratio (PSSR) Minus at 1kHz

Power Supply Voltage (V)	Normal Load: 1k & 100pF	Larger Load: 100k & 100pF
2	58.3dB	59.0dB
3	53.8dB	54.6dB
4	50.64dB	51.57dB
5	47.85dB	48.9dB

Part 1: Biasing Circuit

The Biasing Circuit topology I choose is below:



Folded Cascode Topology: This topology is best when generating bias voltages. This is because the method of diode-connecting the NMOS devices allows the PMOS current source to set the gate potentials of the NMOS current source that is diode connected beneath the two PMOS devices. This way, we can connect the currents and allow them to be at the same potential between the two sources. Current stealing is used with these connections.

I designed this circuit to follow a VDSsat voltage of 5% of the lowest VDD, to follow 5% of 2V, at 100mV. The voltages on the biasing circuit that correspond to VDSsat are Vhigh and Vlow.

Since VDSsat is related to the other voltages, perfecting those values should give the accurate biasing voltages in the rest of the circuit. I changed the sizes of two transistors in the biasing circuit to change Vhigh and Vlow to 100mV, and those changes led the other voltages to align with my calculations. In order to increase VDSsat, the length should be increased since the length is directly proportional to VDSsat and the width is inversely proportional to VDSsat. Increasing the width will decrease the value. This is based on the VGS equation and its relation to VDSsat.

$$V\,DSsat = V\,GS - V\,thn$$

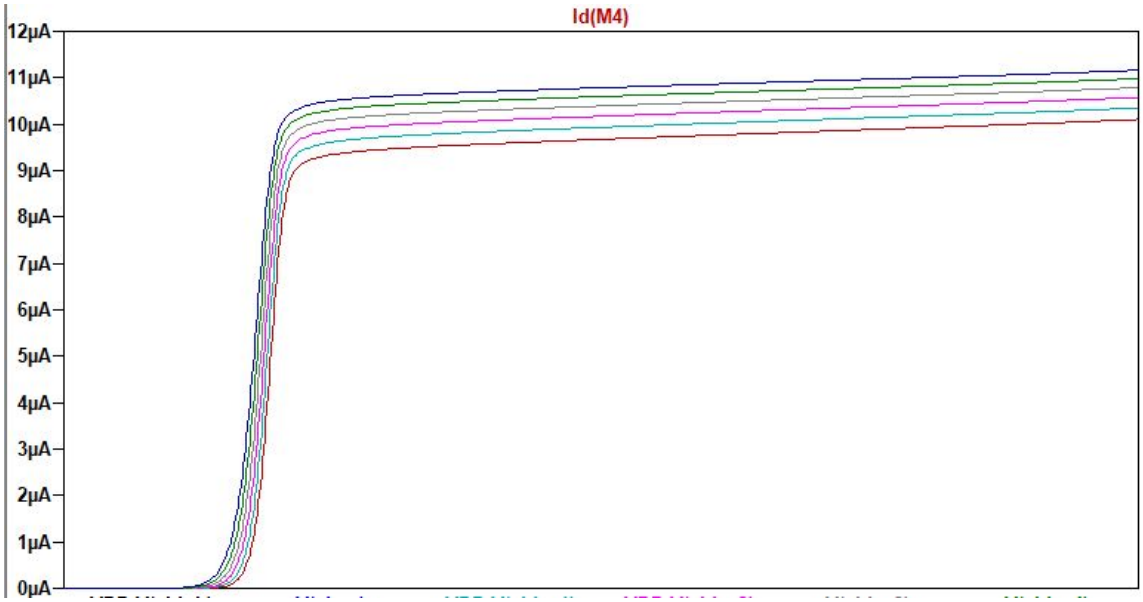
$$V\,DSsat = \frac{\sqrt{2ID}}{\sqrt{KP\frac{W}{L}}} + V\,thn - V\,thn$$

$$V\,DSsat = \sqrt{\frac{2*ID*L}{KP*W}}$$

From this equation, it is deduced that the length of the MOSFET is directly proportional to the VDSsat value and the width of the MOSFET is inversely proportional.

Vlow corresponds to VDSsat and Vhigh corresponds to VSDsat.

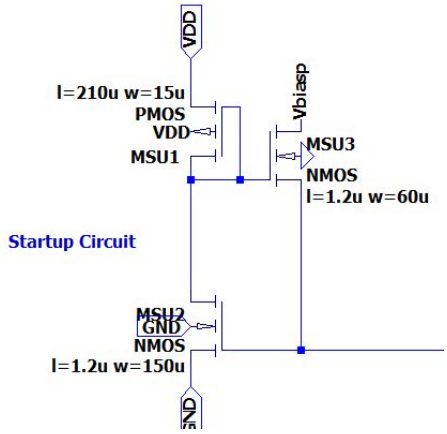
Current over Varying Temperature: 10uA



The current used in my biasing circuit ranges from 9.93uA to 10.4uA from 2V-5V. I was able to flatten the current and make it constant over a range of voltage by increasing the width on the NMOS of my startup circuit. The current value I chose was 10uA. Increasing the current gives a better gain, however, it increases the power and the benefits do not outweigh the negative effects of a high power dissipation. Decreasing the current creates a skewed step response, even if the phase margin is accurate. A current as high as 30uA, or as low as 5uA can give off a gain that

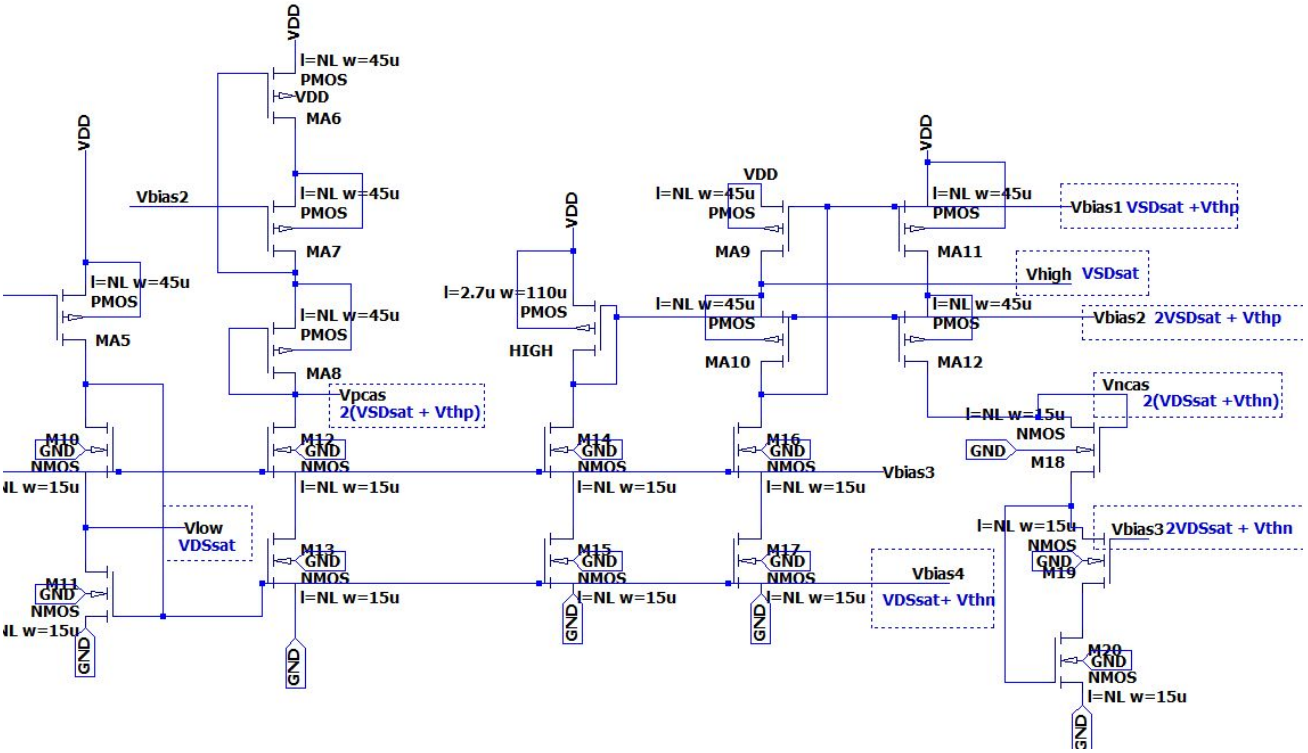
meets requirements in this project, however, they either consume excessive power, or reduce the functionality of the circuit in a transient response. The current can be easily increased and decreased by changing the resistor value in the Beta Multiplier Circuit. Increasing the resistance decreases the current while decreasing the resistor increases the current.

Startup Circuit: The three transistors in the startup circuit are used to turn the circuit on, and act as a switch. These transistors work with the gate voltages of the transistors in the circuit, and when some of them are at VDD, and MSU1 turns off, the other two transistors will be on, and send current into the gates of the transistors that have gone to ground and turn them back on. Once the current is stable, MSU3 turns on.



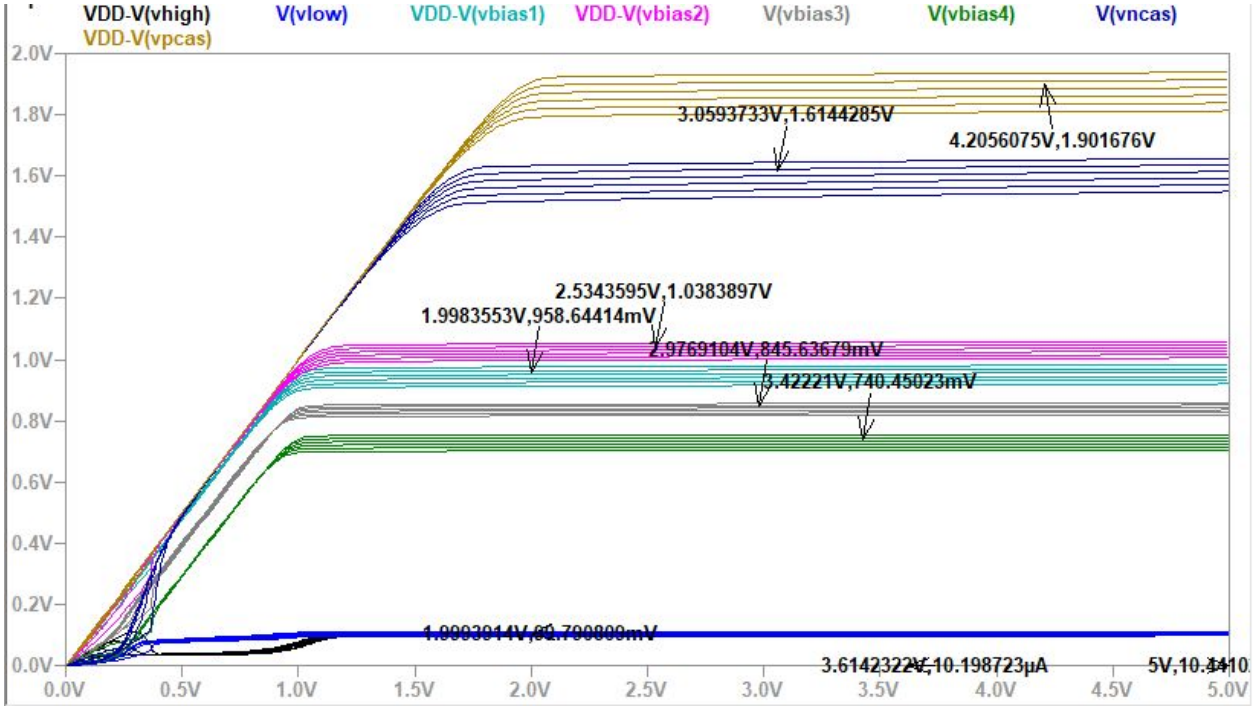
The current can be easily increased and decreased by changing the resistor value in the Beta Multiplier Circuit. Increasing the resistance decreases the current while decreasing the resistor increases the current.

I designed the biasing circuit to follow the calculations of what the voltages should be in the circuit. Below is a photo showing the values of the biasing voltages.



Below are the voltages simulated from the current reference.

Biasing voltages over varying temperatures from 0- 100 degrees Celsius with increments of 20 degrees, showing that the circuit works under all temperature conditions.



Vthn = 0.667

Vthp = 0.9214

Vhigh = VDSsat is set to 99.8mV in my biasing circuit, which is about 100mV, at 5% of 2V.

Vlow = VSDsat is set to 99.9mV in my biasing circuit, which is about 100mV, at 5% of 2V.

The calculations used are below:

Vbias1 = VSDsat + Vthp = 0.098V + 0.9214V = **1.02 V**

Vbias2 = 2VSDsat + Vthp =2*0.098 + 0.9214 = **1.121 V**

Vbias3= 2VDSsat + Vthn = 2 * 0.098 + 0.667 = **0.863V**

Vbias4 = VDSsat + Vthn = 0.0998 + 0.667 = **0.7668V**

Vncas = 2(VDSsat + Vthn) = 2 * (0.099 + 0.667) = **1.532V**

Vpcas = 2(VSDsat + Vthp) = 2 * (0.0999 + 0.9214) = **2.04V**

Vlow = VDSsat = **0.0998 V**

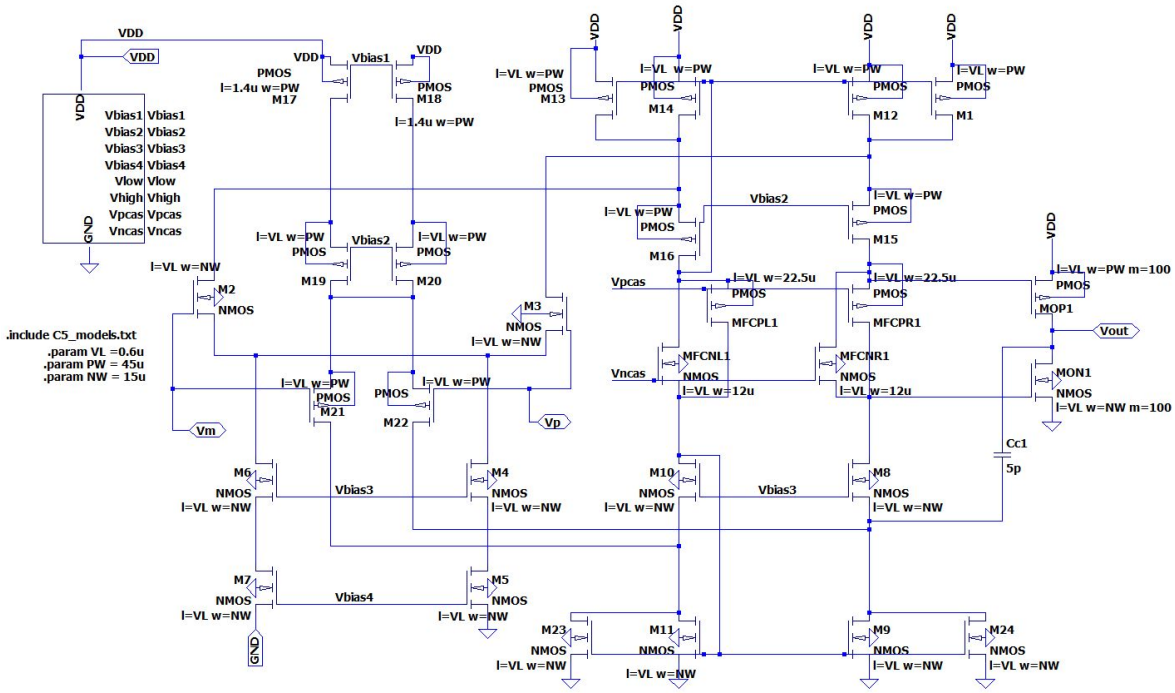
Vhigh = VSDsat = **0.099V**

The biasing voltages from LTSpice compared to calculations:

Voltage Name	From LTSpice (V)	From Calculations (V)
Vbias1	0.960	1.02
Vbias2	1.04	1.121
Vbias3	0.845	0.863
Vbias4	0.739	0.7668
Vncas	1.60	1.532
Vpcas	1.89	2.04
Vlow	0.100	0.0998
Vhigh	0.100	0.099

The voltages from my circuit are very similar to the calculated voltages.

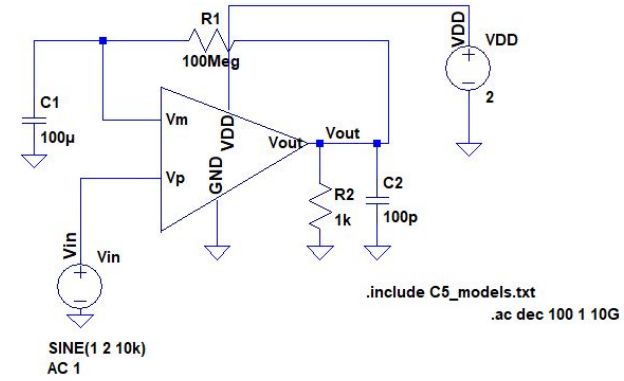
Part 2: Op-Amp Design

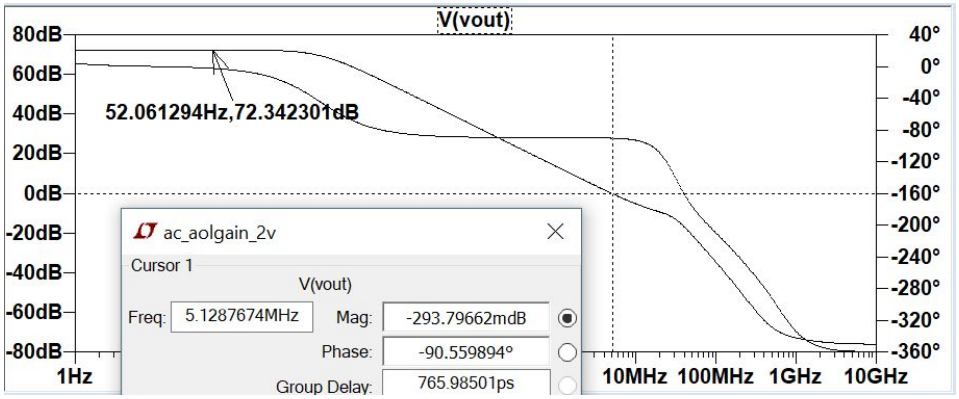


The op amp design I chose is a wide swing, folded cascode op amp with a class AB output buffer and a PMOS differential amplifier stage. I choose a wide swing topology in order to increase the input common mode voltage with the PMOS diff amp addition, and the NMOS additions to sink the larger current supplied by the PMOS This topology is very useful because the floating current sources minimize offset from the input. Using this topology allows us to increase the unity frequency and gain bandwidth product by decreasing the compensation capacitor cc. In this case, I increased the compensation capacitor in order to create a more stable circuit. The two output transistors creating the output stage are large in order to stabilize the circuit as well. They are not too large in order to create practicality when laying out a circuit on a chip.

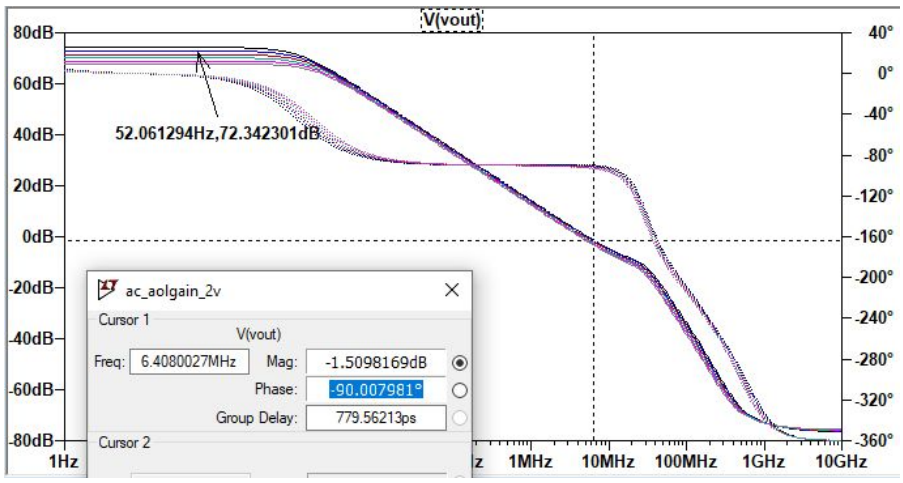
My goal when designing the circuit was to minimize sizes as much as possible to create the most efficient and concise layout. The sizes I used are the same as the ones in the current reference and biasing circuit, lengths of 0.6u (minimum length) and PMOS widths of 45u, and NMOS widths of 15u. The purpose of this circuit is to have as large of a gain as possible while the stability is optimal by giving a phase margin of 90 degrees, since the phase shift at unity gain is -90. The step response is thus a first order response. I wanted to reduce the current and power as much as possible while having an optimal phase margin and gain. Once those conditions were set, I worked on improving the CMRR and PSRR, however, my goal is a large gain, a very stable circuit, low power dissipation and lower current input.

Project Condition 1: DC open loop gain of > 66dB





Gain of 72dB with a phase margin of 90 degrees. The gain and phase margin also stay the same at varying temperature.



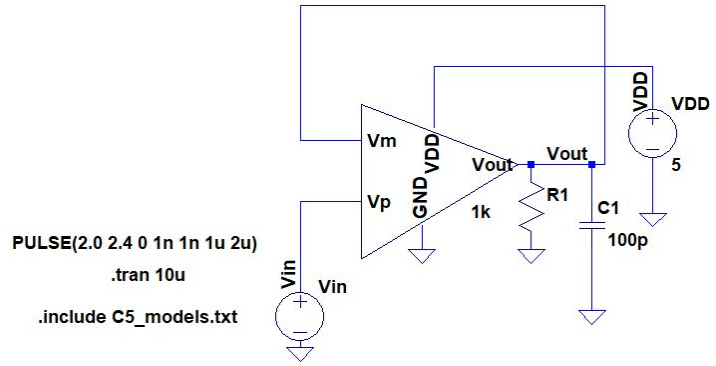
Project Condition 2: Gain Bandwidth Product > 1MHz at 5.12MHz.

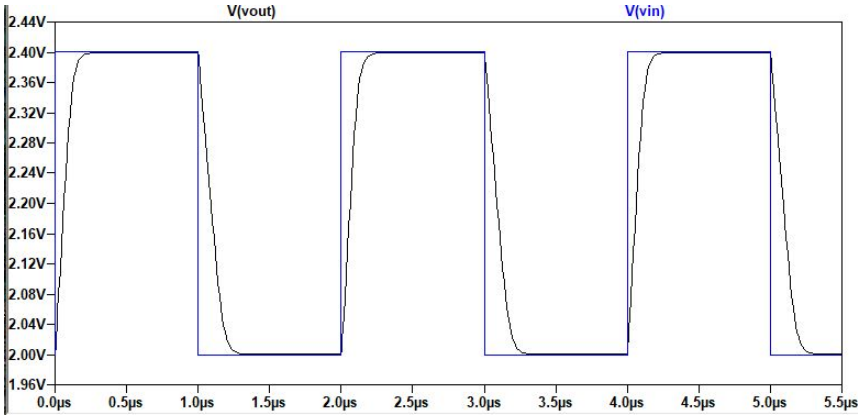
Two specifications are satisfied here, a gain over 66dB and a gain bandwidth product over 1MHz, at 5.12MHz.

Phase Margin

The ideal phase margin in this case is 90 degrees in order to create an optimal step response that acts as an RC circuit, giving off a first order response.

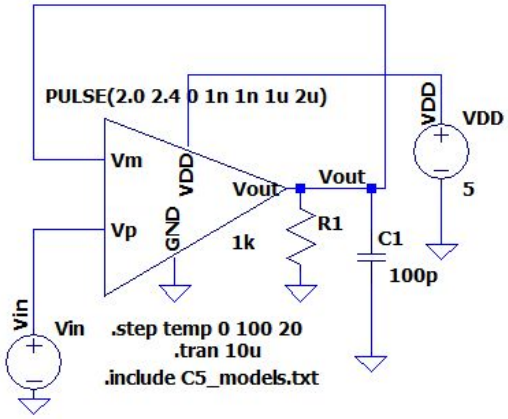
Step Response: since the phase margin is 90 degrees, the step response is a first order response, like an RC circuit.

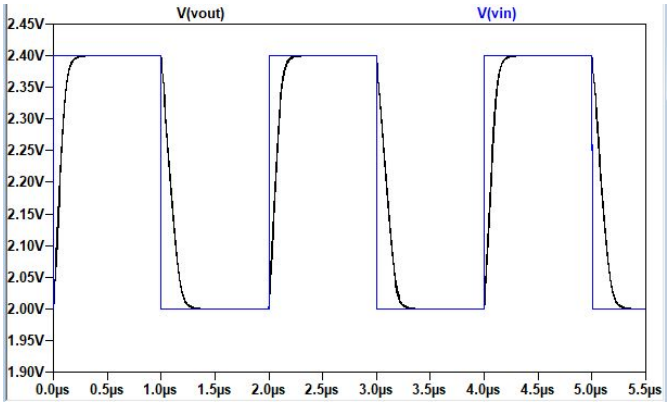




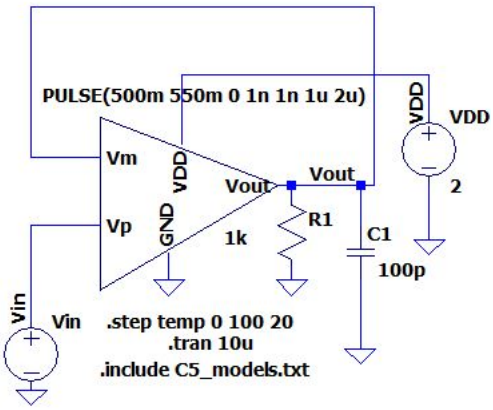
Step Response at Varying Temperature of 0-100 degrees Celsius

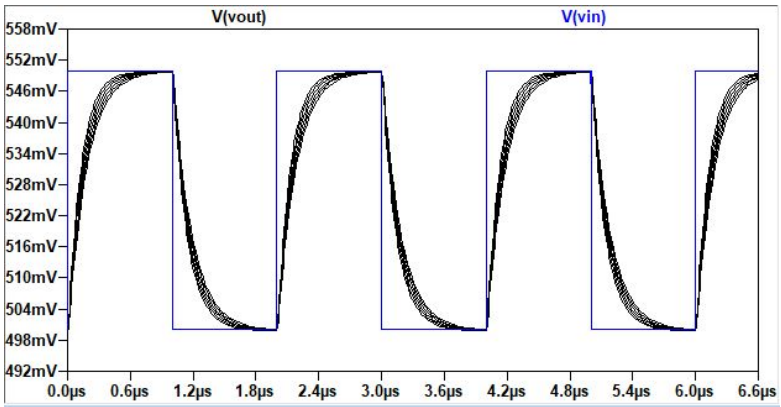
VDD of 5V





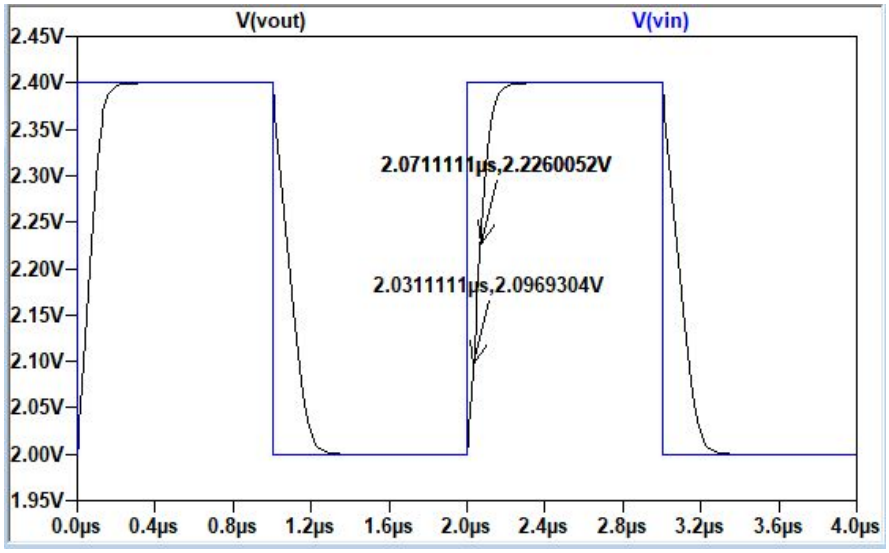
VDD of 2V





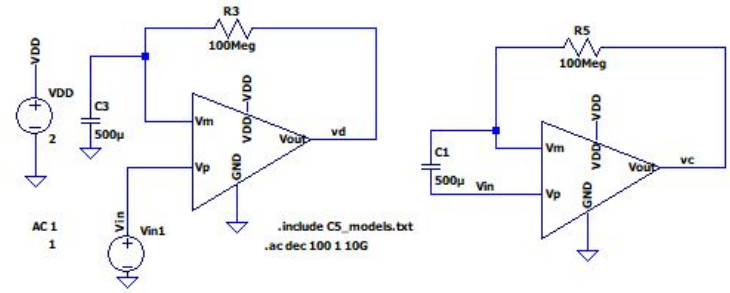
Project Condition 3: Slew Rate with maximum load > 1V/ microsecond at 3.22V/us

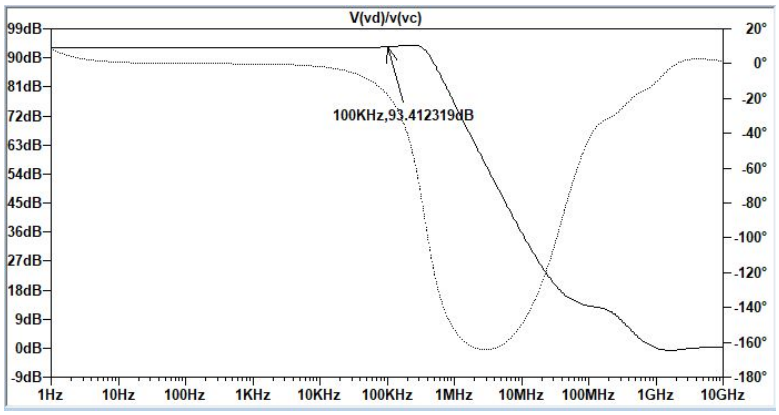
Using the same step response circuit from above.



Slew Rate = $\frac{change\ in\ voltage}{change\ in\ time} = \frac{2.226V - 2.0969\ V}{2.0711us - 2.0311us} = \frac{0.1291V}{0.04us} = 3.2275\frac{V}{us}$

Project Condition 4: CMRR > 90dB at 100kHz, CMRR is 93.4dB





The CMRR was 93.41dB which was above the requirement. At first, I had a lower CMRR of about 70dB. The common mode signal is just noise, so the common mode rejection ratio is how well the circuit's differential amplifier rejects noise. The noise affects the positive and negative terminal's voltages to vary so increasing the CMRR is crucial for a good circuit. By understanding the CMRR equation, I deduced that increasing the length of the PMOS differential amplifiers current biasing source would **decrease gm** and in turn **increase the output resistance.** Increasing the output resistances increases the CMRR.

$$\text{The equation for gm} = \sqrt{(2 * Kpn * \frac{W}{L} * ID}$$

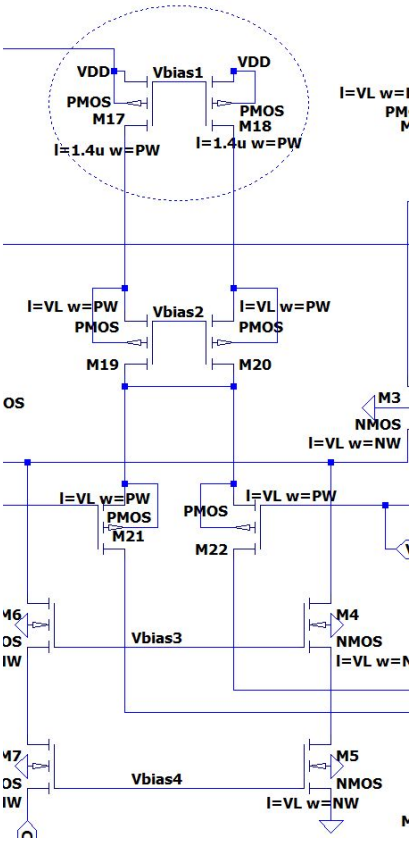
Increasing the length decreases the gm because the length is inversely proportional to the gm.

$$ro = \frac{1}{gm}$$

Once gm goes down, the r0 goes up and the CMRR increases based on the equation for CMRR below.

$$Common\ Mode\ Gain = Ac = \frac{Vout}{Vc} = \frac{\frac{-1}{gm}}{2*Ro} = \frac{-1}{2*gm*Ro}$$

$$CMRR = 20 * \log log \left|\frac{Ad}{Ac}\right| = 20 * log(gm\,(ro17||ro18) * 2(gmRo)$$



The usual length was 0.6u and was increased to 1.4u.

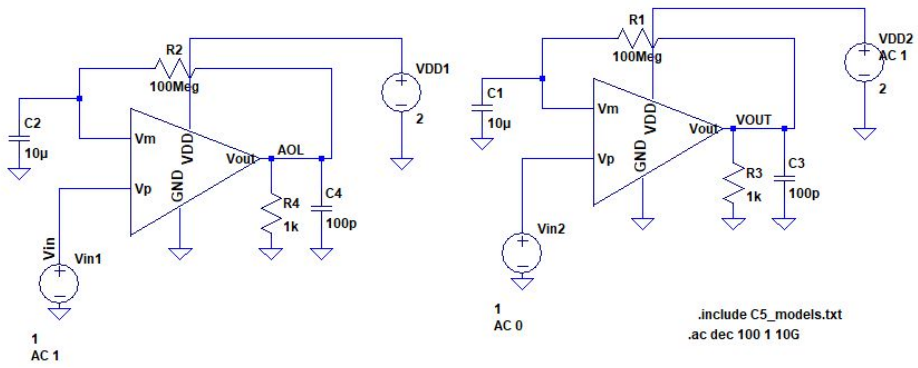
Project Condition 6: PSRR > 60dB at 1kHz

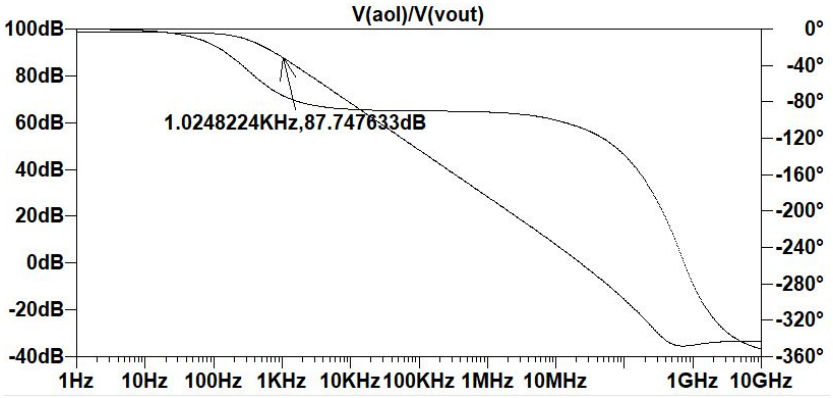
PSSR PLUS at 87.74dB at 1kHz.

The power supply rejection ratio measures how well the op amp rejects noise on the power supply voltages, VDD and GND, where the CMRR checks the voltages on VP and VM.

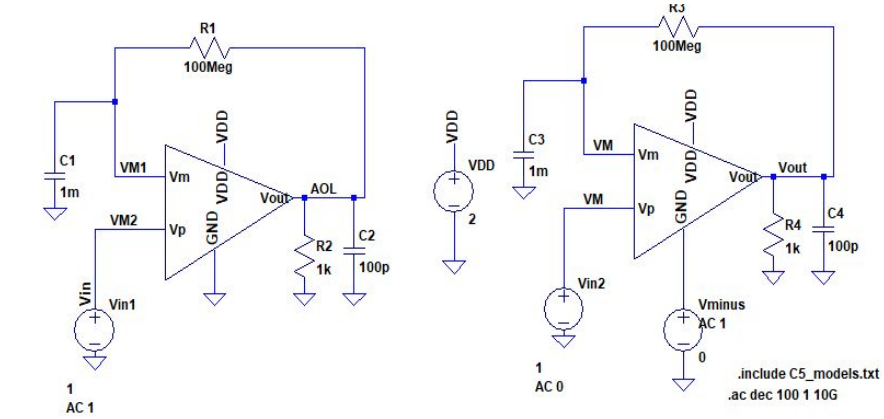
The compensation capacitor has a lot to do with PSRR since at higher frequencies, the compensation capacitor has a transistor gate and drain short together which sends the noise from VDD to the output. The ground noise does not affect the op amp ideally, but it does show up in practical circuits at the output. At high frequencies the compensation capacitor, ground noise does not appear.

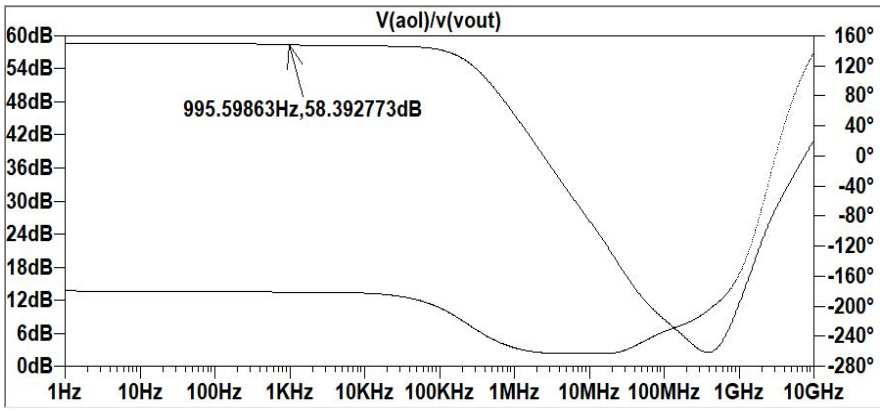
$$PSRR+ = \frac{Aol(f)}{\frac{Vout}{V+}}$$





PSRR Minus: Slightly below 60dB at 1kHz, at 58.4dB



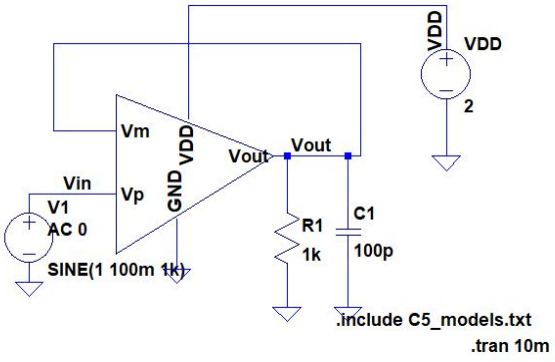


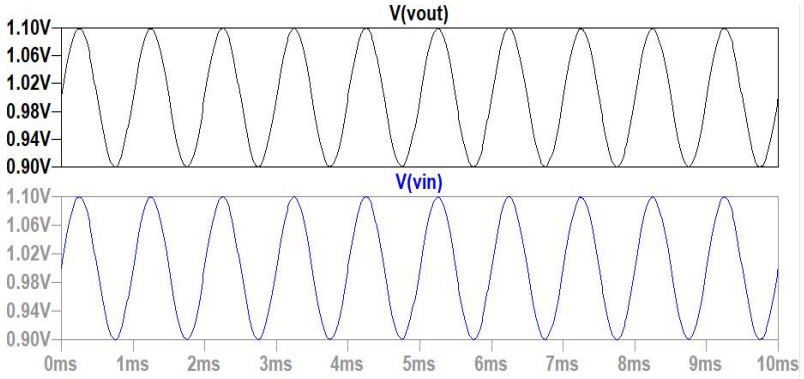
At higher frequencies, the PSRR is still at 58dB before dropping, whereas for the PSRR plus, the signal falls earlier, before 1kHz. Because of the compensation capacitor, at higher frequencies the ground noise contributions to the output signal decrease.

The PSRR minus is slightly below the requirement, because of a tradeoff I choose in this design. Increasing the gain will increase the PSRR, however the stability of the circuit decreases. My priority in this design is to have a stable circuit, with an ample gain, that dissipates less power and needs a minimal current.

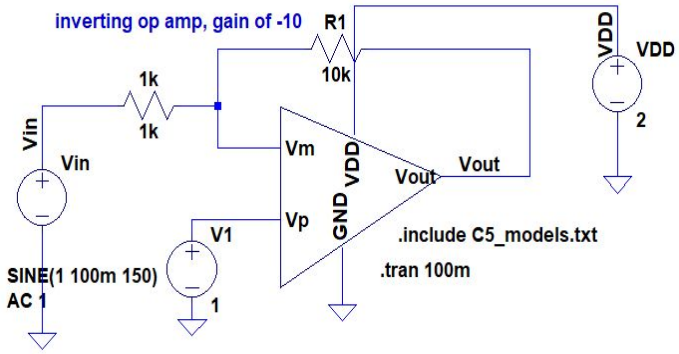
Testing Closed Loop Gain using a Voltage Follower

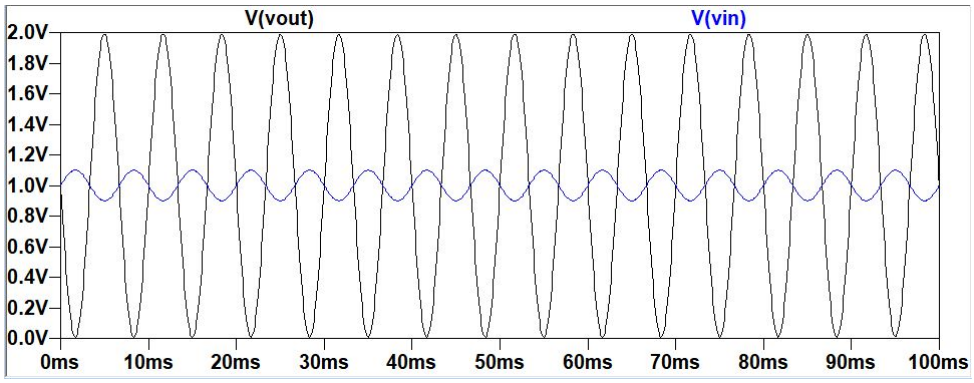
The closed loop gain of a voltage follower is 1. A voltage follower is actually very unstable and testing it with a feedback increases the stability when testing the open loop gain. Testing it with a load of 1k and 100pF shows the gain to be 1.





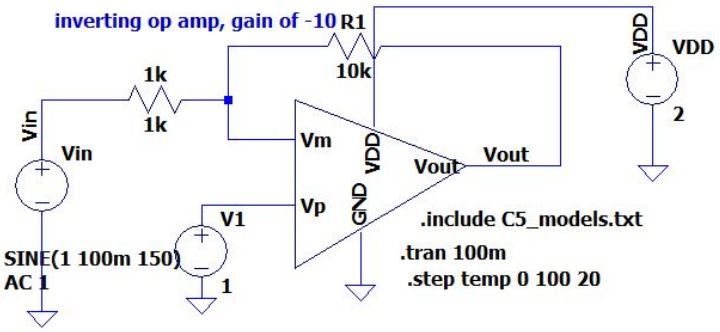
Testing Closed Loop gain using an Inverting Op-Amp

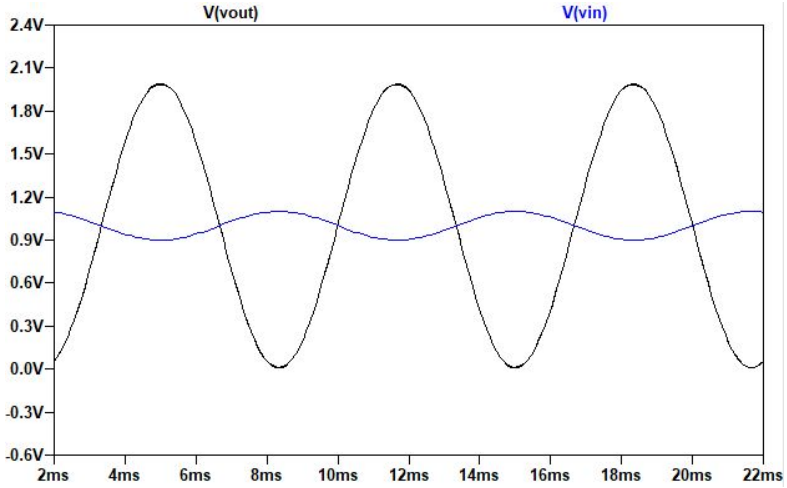




Closed Loop Gain Over Varying Temperatures

Gain remains the same

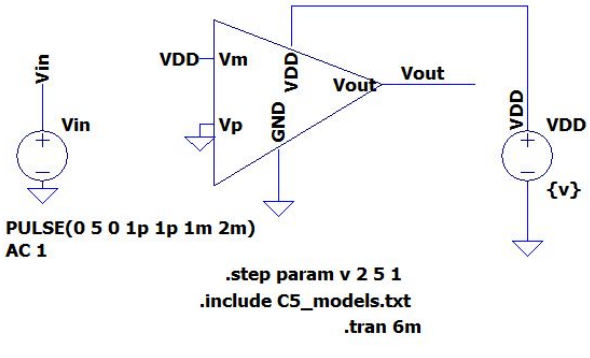


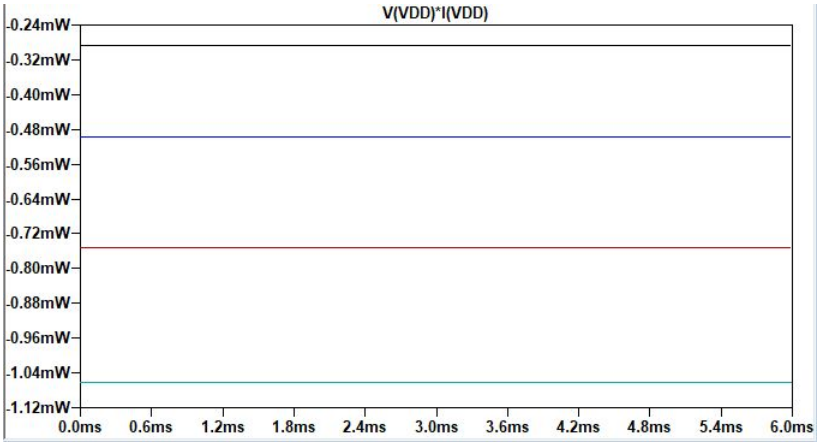


Power Dissipation

One of the goals of this op amp design is to dissipate as little power as possible while operating properly. The current was reduced in order to find the power. To find the power dissipation, all the currents were added through each branch and multiplied by the VDD value.

The power ranges from 287.85uW at 2V to 1.06mW at 5V. The power dissipation is not optimal, however, for such a large gain, the power dissipation of the circuit is sufficient. Increasing the PSRR would also increase the power, however, since reducing the power was a goal in this project, the PSRR was slightly less in the PSRR minus.





Input CMR as a Function of VDD

The common mode range (CMR) is the range at which the inputs of the op amp can operate, since the inputs are forced through feedback to be similar values. If the voltages on VP and VM go outside of the CMR, the gain can fall. The common mode voltage is the average of the voltages on the inputs of the op-amp. In order to maintain that range we must know the minimum and maximum input voltages. We can find those values using the VCMmax and VCMmin equations.

$$VDS >= VGS - Vthn$$

$$VD >= VG - Vthn$$

$$VD = VDD$$

$$VD >= VG - Vthn$$

Let VG = Vcmmax

$$Vcmmax = VDD + Vthn = 2V + 0.667 = 2.667V$$

The VCMmax equation shows that the input can be 667mV larger than the power supply voltage.

Find VCMmin

$$Vcmmin = VGS + 2 * VDSsat$$

$$VSD >= VSG - Vthp$$

$$VD <= VG + Vthp$$

$$Let\ VG = VCMmin$$

$$VCMmin = VD - Vthp$$

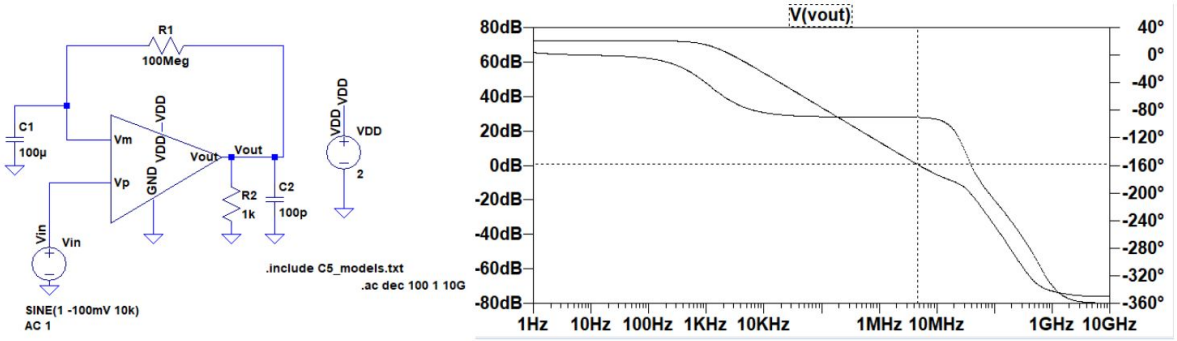
$$VD = VDSsat$$

$$VCmmin = VDSsat - Vthp = 0.100V - 0.9214V = -0.8214V$$

The VCMmin equation shows that the input can drift 821mV below power supply voltage. The common mode range is the range between these two voltages with respect to VDD.

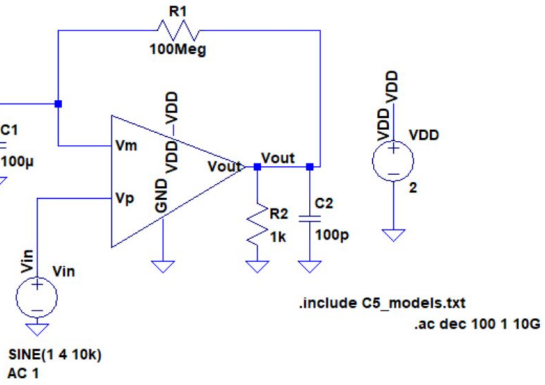
VCM Min Simulation

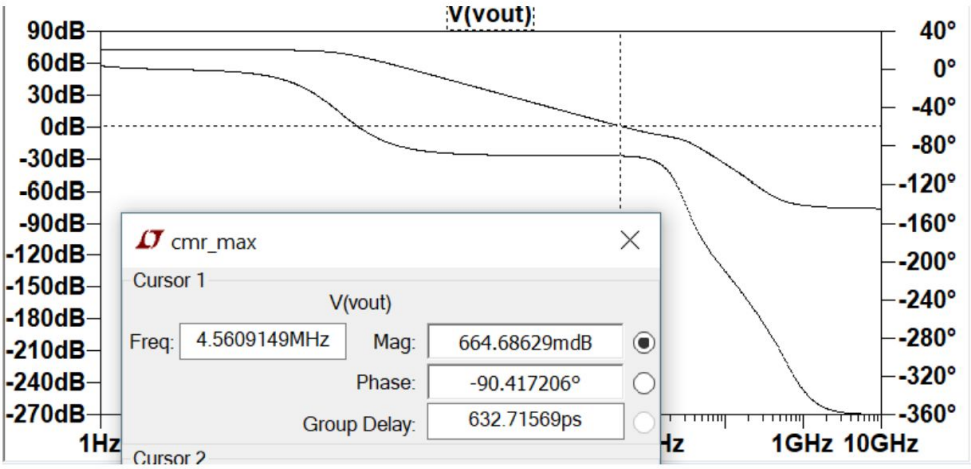
This simulation shows that when the input voltage in the positive terminal is more than 800mV below VDD, the circuit still operates correctly. I tested it with a negative voltage to show the full operation. The gain is still above 66dB and the phase margin is still 90 degrees.



VCM Max Simulation

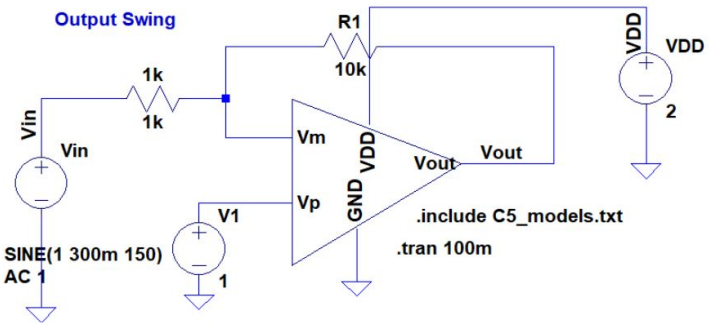
CMR max tested with an input voltage double the power supply voltage.

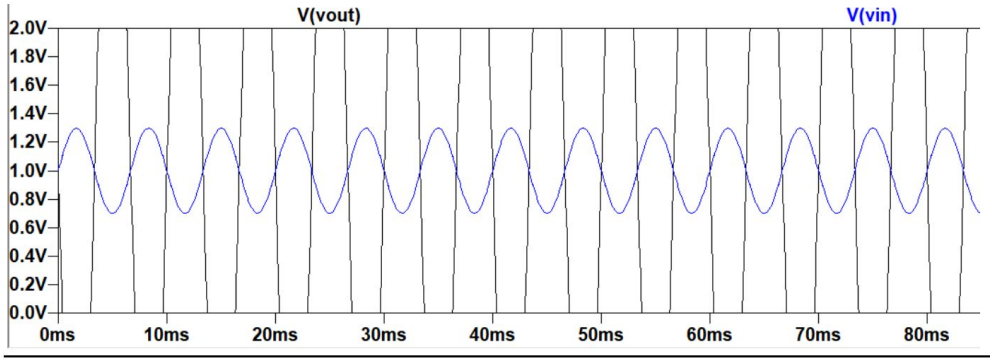




Output Swing

In order to measure the output swing, a sine wave with a large amplitude is sent into the op-amp in order to find where the output clips. The amplitude I choose was 300mV and the output was 2V again, showing that the output swing is from 0-2V.





Conclusion

Some trade-offs made in this design to preserve the design goals were the reduction in PSRR in order to reduce power dissipation and the gain. Decreasing the current increases the gain and in turn, the PSRR, however it makes the circuit unstable. The only way to decrease the current without reducing stability is to also reduce device sizes throughout the biasing circuit and the op-amp. The CMRR value was not as high as possible, as explained in the next paragraph. Due to time constraints, I was not able to redesign the entire circuit properly and improve stability.

If I had more time to improve my design, I would aim to reduce device sizes even more, and reduce the amount of current from the biasing circuit because that would reduce power dissipation. Reducing the current will reduce the power since current is added up by each branch and multiplied by the VDD value. I would also increase the output resistance of the PMOS differential amplifier in order to increase the common mode rejection ratio and increase the performance of the differential amplifier. The CMRR value of my circuit met requirements, however, I was able to increase it even more by increasing the output resistance of the PMOS differential amplifier but choose not to in order to preserve the stability of the circuit (due to time constraints). Reducing the sizes and increasing the current will improve the gain of the circuit and improve the PSRR. The reduction in sizes is optimal for circuit layout on Cadence as well and changing the circuit in that regard would make it most optimal.