HIGH DYNAMIC RANGE ACTIVELY QUENCHED SILICON-GERMANIUM SINGLE-PHOTON AVALANCHE DIODES

By

Abraham Castaneda

Bachelor of Science in Engineering – Electrical Engineering
University of Nevada, Las Vegas
2023

A thesis submitted in partial fulfillment
of the requirements for the

Master of Science in Engineering – Electrical Engineering

Department of Electrical and Computer Engineering
Howard R. Hughes College of Engineering
The Graduate College

University of Nevada, Las Vegas
May 2025

ABSTRACT

Single-photon avalanche diodes (SPADs) are solid-state devices capable of providing large current pulses in the milliampere range in response to incident photons. The large gain inherent to SPADs makes them a popular technology for photon counting applications, but their operation can be hindered by long recharge times, which necessitates the use of active quenching to reduce dead times and increase detection rates. For the prompt gamma/neutron radiation experiments conducted at the Nevada National Security Site, photomultiplier tubes (PMTs) have been the primary photodetector of choice, but their continued use is expected to dwindle as it becomes increasingly difficult to source quality PMTs due to aging of the technology. As a result, alternative means of photodetection are currently being researched, with SPADs being one of the devices of interest.

This thesis details the development of high dynamic range, actively quenched silicon-germanium (SiGe) SPADs capable of meeting the performance targets set by the NNSS for the intended application, which requires reset times of 1-2ns maximum and full-width-half-max output pulses in the 100-500ps range or less. The beginning of this process involved testing a multitude of SiGe SPADs previously developed by the lab using the Austriamicrosystems 0.35μm SiGe BiCMOS process and determining which device structure and size yielded the shortest pulse widths (an indicator of a small junction capacitance, a desired parameter for the aforementioned metrics). Once the ideal SPAD structure was identified, a 5μm-by-5μm square structure without guard rings, the device was further tested to characterize its current response to varying degrees of reverse biasing. Using this information, an LTspice model was developed to emulate the SPAD's behavior to facilitate more accurate simulations of the final two active quenching integrated circuit designs, which were developed using TSMC's 180nm process. The

variable-load active quenching design was able to achieve a nominal reset time of 738ps with a 103ps FWHM output while the latching active quenching design provided a nominal reset time of 735ps with a 73ps FWHM output, indicating that both designs can theoretically resolve 1Gcps (gigacounts per second) reliably. Preliminary layouts of the actively quenched SPAD pixels with integrated analog counting were created using TowerJazz's 180nm SiGe BiCMOS process, the process in which the final chip will ultimately be manufactured.

ACKNOWLEDGEMENTS

First and foremost, I wish to express how immensely grateful I am for all of the learning experiences I have been granted throughout my academic journey and for the amazing individuals I have had the great fortune of meeting, all of whom have contributed to where I am now. I want to especially thank my parents for their unwavering support and encouragement throughout my career. You have always motivated me to pursue my dreams with faith and integrity regardless of the circumstances and challenges I face, and you have engrained in me the belief that having a strong passion for what you do must always be accompanied by an equally strong work ethic to achieve one's goals.

To my professor, mentor and committee chair Dr. Baker, I extend my sincerest gratitude for the significant role you have played in my professional development and for granting me innumerable opportunities to expand my horizons through your insightful courses and cutting-edge research. Your amazing ability to practically convey the most complicated concepts in a way that can be captured, understood, and used by students is what fueled my desire to learn, and your prowess as an engineer inspires me to challenge myself to be the best engineer I can be. Thank you for giving me a chance, it has been a privilege learning and working under your guidance. To Dr. Harris and Dr. Morris, I give my utmost appreciation for also introducing me to the world of research so early on in my academic career. Your REU program showed me what it takes to be a good, thorough researcher and how to ask the right questions when confronted with obstacles during the research process. Thank you for your mentorship and for dedicating your time to participate in my thesis committee. To Dr. Barzilov, thank you for being willing to serve as the graduate college representative for my thesis. Your background in radiation detector research is vast and I truly appreciate your contribution to my committee.

I also want to thank Angsuman Roy for his knowledgeable contributions and for always being available to provide his unique perspectives on this project. Your extensive experience in photonics is undeniable and I appreciate you helping me to grasp the more technical aspects of chip design. From the NNSS, I am very thankful to James Mellott and Robert Buckles for their continued support of this project and for allowing students like myself to participate in such interesting work. I have learned so much from our meetings and hope I can continue to learn from your expertise. From Dr. Baker's lab, I would like to recognize and thank Andrew Kerstetter for his assistance in collecting the batch testing data and his redesigning of the TO-8 testing boards used for testing in this thesis. I also want to acknowledge all of the previous lab members whose work helped to lay the foundation that this thesis is built upon, thank you.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1: INTRODUCTION

On September 23, 1992, the very last underground nuclear explosive test, code named "Divider", was conducted at the Nevada National Security Site (formerly the Nevada Test Site). That same year, the United States would enter into a moratorium prohibiting all nuclear weapons testing, which saw several extensions in the following years and culminated in the signing of the Comprehensive Nuclear Test Ban Treaty in 1996 [1]. With a strong need to ensure the reliability of the U.S. nuclear arsenal without full scale explosive testing, the Stockpile Stewardship Program was born, which today leverages subcritical experimentation as well as a wide range of novel scientific and engineering diagnostic techniques to monitor and maintain the nuclear stockpile.

Prompt radiation detection through the use of scintillation is one such technique that has been utilized to support stockpile experimentation and operations. It is conducted by exposing a scintillator (a material that emits light when exposed to ionizing radiation) to a radioactive sample and using a photodetector to convert the light into a measurable electrical signal. Photomultiplier tubes (PMTs) have been the standard photodetector of choice used to perform these tests, but due to aging of the technology and lack of market demand, procuring PMTs that fit the needs of such applications has become increasingly difficult, which calls for new photodetector technologies [2]. Single-photon avalanche diodes (SPADs) are solid-state devices that conduct an amplified current when exposed to incident photons and are one of the technologies being explored as a possible substitute. However, the commercial SPAD products currently on the market are simply too slow for the intended use, which calls for more novel design techniques involving quenching and digital read-out. Quenching is a method commonly used to quickly reset SPADs by lowering the voltage bias across the device to stop the amplified

current flow and then immediately increasing the bias to its original state so that the device can be ready for subsequent photon detections.

The goal of this thesis is to present a set of active quenching circuits (AQCs) designed using TSMC's 180nm process capable of being used with SPADs in an application specific integrated circuit (ASIC) to meet the required performance targets in terms of speed and dynamic range. Although the final designs will be incorporated into TowerJazz's 180nm SiGe BiCMOS process for the final tape-out, previous design simulations indicated that the TSMC LTspice models were identical enough to the TowerJazz models to create the preliminary designs, which allowed for much faster drafting, modeling, simulation, and debugging using LTspice. With the knowledge gained from previous ASICs designed by Dr. Baker's research group, various CMOS quenching techniques will be explored. The transient behavior of multiple existing SPAD structures from testing will be covered as well, with the fastest device being chosen for the final design. In order to improve the accuracy of the system level simulations, a behavioral SPICE model for the SPAD of interest will also be proposed as a substitute for the ideal current sources available in LTspice.

CHAPTER 2: THEORY AND APPLICATION

2.1 Fundamentals of Photon Counting

Visible light exists as a wave similar to any other wave on the electromagnetic spectrum, but it can also be represented as quantized particle known as a photon with an energy equal to Planck's constant times the frequency ($E = hv$). When an experiment calls for the detection of light signals from an optical event of very short duration, photon counting is often used due to its higher dynamic range and sensitivity as opposed to other methods of light detection that simply measure optical intensity. Photon counting especially allows for precise measurements of low-intensity light signals that may only generate a relatively low number of photons at a time. Devices that operate as photon counters will usually provide a series of pulses coinciding with the arrival of photons or, in more advanced devices with read-out circuitry, a digital output corresponding to the total number of photons detected, typically accomplished using transistor-transistor logic.

There are a variety of specifications that determine the performance of a photon counting device including dark count rate, dead time, and quantum efficiency [3]. The dark count rate (DCR) is the rate at which a photon counting device registers a count without a light source present, which most often occurs due to thermally generated charge carriers. For photon counting experiments where the dark count rate cannot be minimized any further, the nominal dark count for the given time-frame is normally subtracted from the final output count to provide the best estimate of the actual number of photons detected.

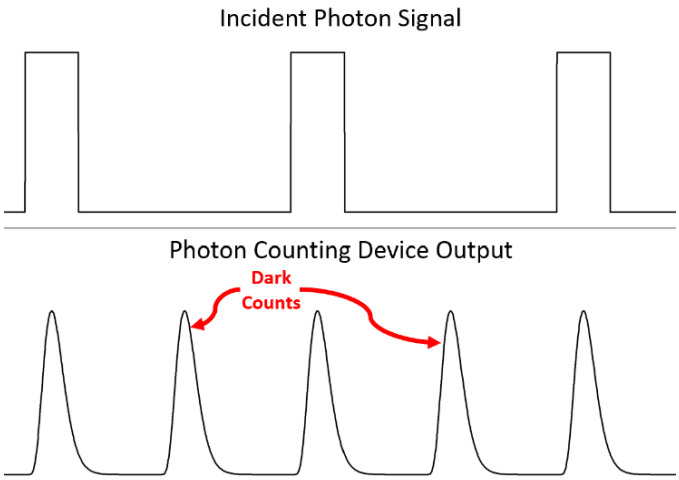


Figure 1: Illustrated example of dark counts

The dead time of a photon counter is the amount of time that must pass after a photon is initially detected for the device to be in a state capable of detecting a photon again, with shorter dead times yielding larger bandwidths. In the case of SPADs, this dead time is heavily influenced by the quenching method used as well as the structure of the device. The quantum efficiency refers to the ratio of the number of electron-hole pairs generated by the absorption of photons to the total number of incident photons. If the quantum efficiency is too low, the device risks missing a significant number of photons, thus impacting the final count.

In practice, when a light signal's intensity needs to be recorded over a period of time, a specific photon counting method known as time-correlated single photon counting (TCSPC) is used. TCSPC involves time-tagging single photon arrivals after repeated excitations and using the data to reconstruct the light emission event in the form of a time-resolved histogram. In experiments using TCSPC, the probability of the photodetector detecting more than one photon per cycle must be low and can be accomplished by using an optical attenuator [4]. In order to accurately reconstruct the light emission event, the event must be recreated enough times for the statistical variation of the photon arrival times to yield valuable information.

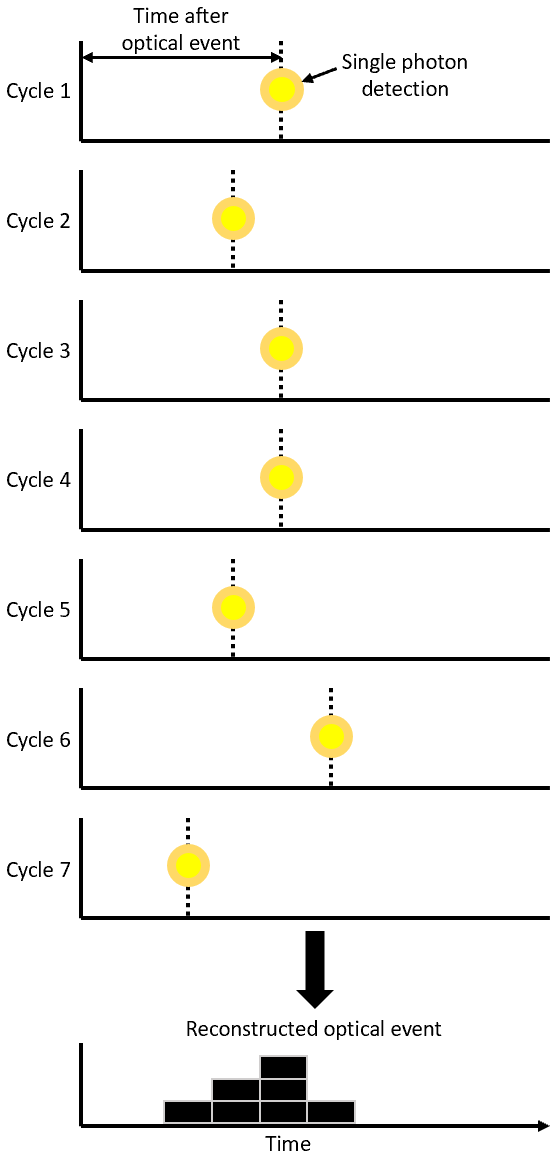


Figure 2: TCSPC operating principle

This method offers very high temporal resolution due to the extreme sensitivity of the photodetectors used and is commonly utilized in time-resolved fluorescence spectroscopy [4]. The drawback of traditional TCSPC however, is the lack of scalability when it comes to recording photon detections from a large number of devices as is commonly seen in SPAD arrays on chips, which would require a large transfer bandwidth and significant memory allocation to store the arrival times of all the photons detected by each cell. In such cases, it becomes more

practical to incorporate time-gating, where photon arrivals are not individually time tagged with an on-chip timer, but rather all counted at once in a series of short time windows over a single optical event cycle [5]. In a time-gating configuration, a higher count rate per detector is desired, so unlike traditional TCSPC, the restriction of one photon detection per cycle is not applied.

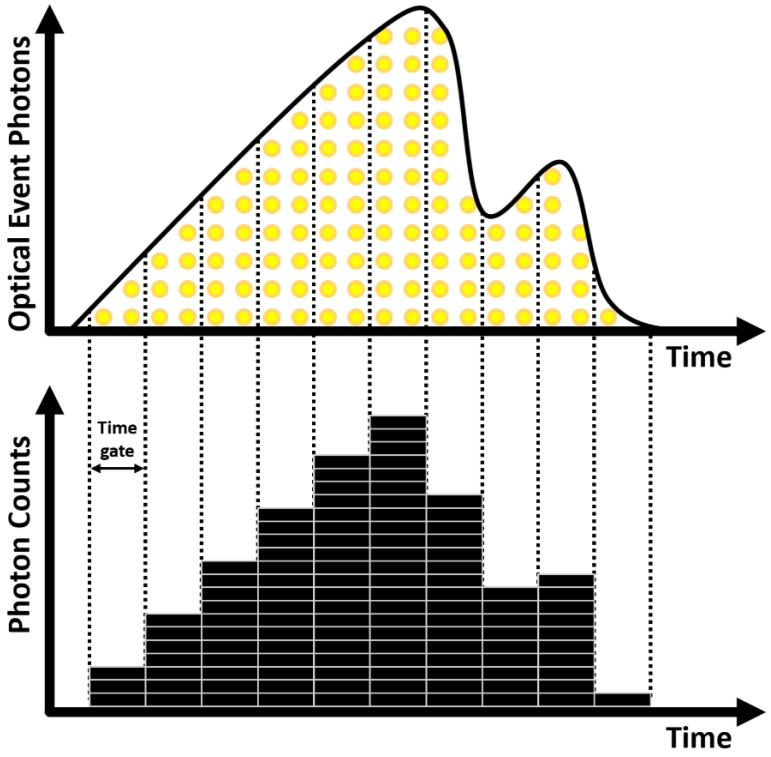


Figure 3: Time-gated photon counting operation

2.2 Basic Semiconductor and Photodetector Theory

Many of the photodetectors that enable photon counting are based on semiconductor technology, which involves the use of materials that can have their conductivity altered through the manipulation of charge concentrations. Intrinsic silicon, for example, on its own is not a good conductor due to the low number of mobile charges, but it can be doped so that the material

carries a majority mobile charge carrier that is either positive or negative, making it more conductive. A P-doped material is a material that has had a certain quantity of acceptor atoms (atoms with less valence electrons than the surrounding atoms in the crystal lattice) implanted into it so that there is an abundance of mobile electron "holes" or positive charge carriers. An N-doped material is created by the same principle only that the implanted element is a donor atom (extra valence electrons) and results in an abundance of mobile electrons or negative charge carriers.

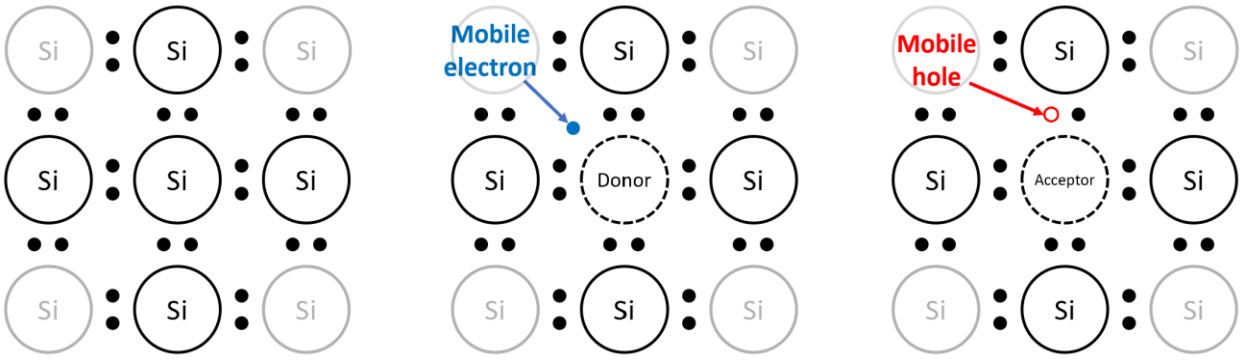


Figure 4: Electron configurations for lattice of intrinsic silicon (left), N-doped silicon (center) and P-doped silicon (right)

When an N-doped and a P-doped material are joined together as a PN junction, a diode is formed, with the N-doped section acting as the cathode and the P-doped section acting as the anode (see figure 6). The conjoining of the doped materials results in the partial recombination of the mobile charge carriers of opposite polarity where the two sections meet (i.e. mobile electrons from the N-region combine with mobile holes from the P-region). As the mobile charges recombine, the acceptor/donor atoms that were implanted into the semiconductor material will acquire a charge due to the loss of the hole/electron they originally carried in their neutral state. The result of this recombination is a region located in the center of the PN junction that is

depleted of mobile charges and instead contains immobile ionized donor and acceptor atoms, creating a localized electric field. This region is known as the depletion region and its electric field prevents the rest of the mobile charges within the device from recombining. One important aspect to note is that the creation of the depletion region gives rise to a depletion or junction capacitance resulting from the proximity of the mobile charge carriers on either side of the junction [6]. This internal capacitance will be an important parameter to consider in SPADs, as will be covered in the following section.

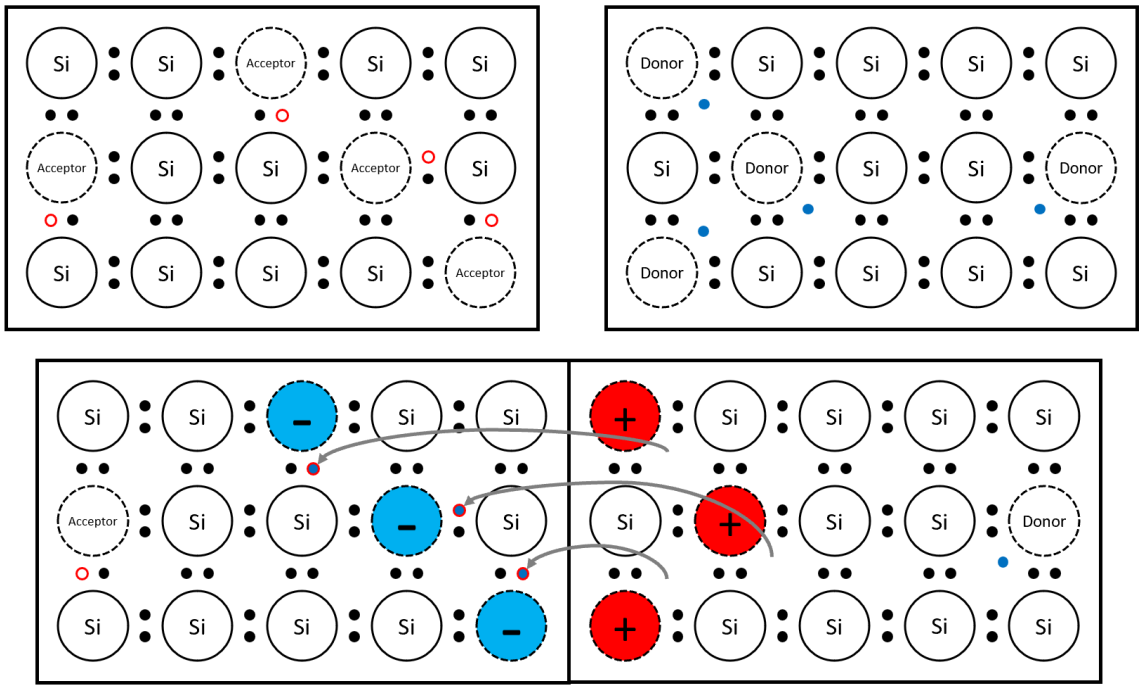


Figure 5: PN junction formation

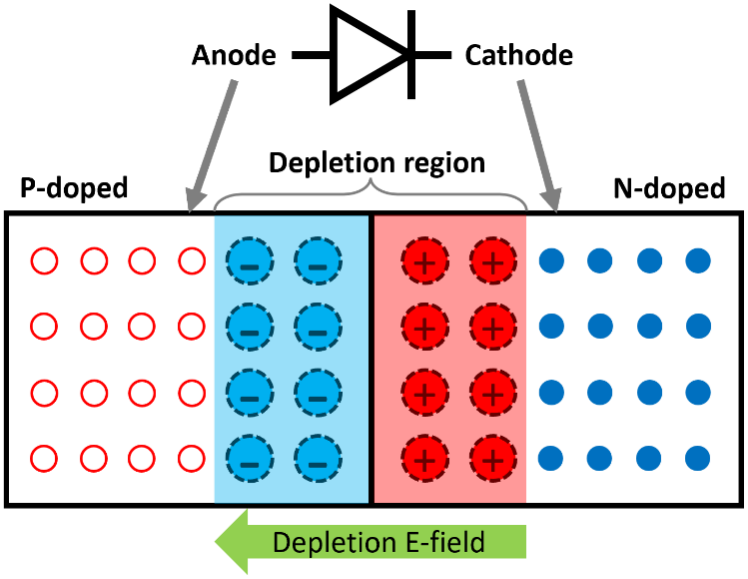


Figure 6: Diode shown with depletion region

The behavior of mobile charge carriers can be best described using energy band diagrams and the Fermi energy level, the energy level at which the probability of an electron being present is 50% [6]. In the context of conductivity, the two main energy bands an electron can reside in are the valence band and the conduction band. The valence band encompasses energies where electrons are bound to the valance shell of an atom (forming the covalent bonds that make up the lattice) while the conduction band makes up the energy levels where the electrons are not bound to an atom and thus free to move throughout the material. In a metal such as copper, the valence and conduction bands overlap while in an insulator, such as rubber, the bands are separated by an energy difference known as the bandgap energy, which is the energy needed for an electron in the valence band to make the transition up to the conduction band. A traditional insulator will exhibit a very large bandgap energy while a semiconductor's bandgap energy will be significantly smaller, making it suitable for photodetection.

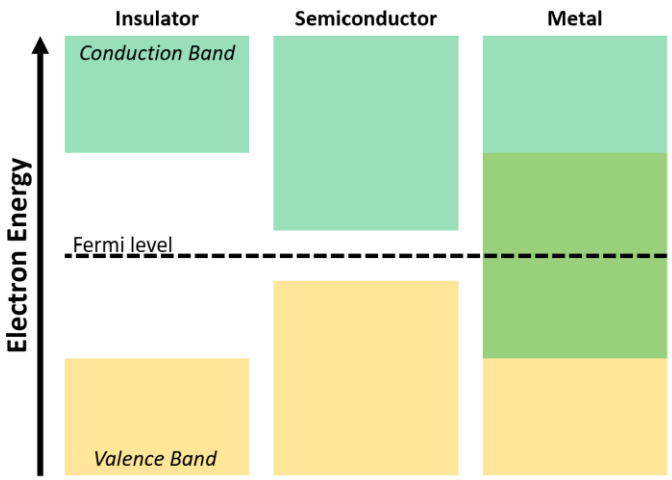


Figure 7: Energy band diagrams for insulator (left), semiconductor (center) and metal (right)

Photodetector devices fall into two main categories: thermal detectors, which rely on the conversion of photonic energy into heat, and photoelectric detectors, which utilize the photoelectric effect to generate charges from light [7] and are the focus of this thesis. The photoelectric effect is the phenomenon that describes how electrons, when exposed to a photon of sufficient energy, can transition from a lower energy level to a higher energy level through photon absorption (enables the transfer of a photon's energy to an electron). When exposed to light of sufficient energy, these electrons can either escape the device material entirely and travel into free space (external photoelectric effect), as is done in PMTs, or remain within the material (internal photoelectric effect). The latter applies to solid-state photodetectors such as photodiodes, which are further categorized as photoconductive devices [7].

The operation of the photodiode, the basic structure of which is derivative of the regular diode structure illustrated in figure 6, is facilitated by the photoconductive properties of semiconductor materials. When a photon that possesses an energy meeting or exceeding the bandgap energy of the medium reaches the photodiode and is absorbed, an electron has the potential to successfully make the transition from the valence band to the conduction band. Since

the process of an electron leaving the valence band results in an atom having one less electron, an electron "hole" is left behind and a positive mobile charge carrier is effectively created. The result is that for every photon that is absorbed by the material, an electron-hole pair is generated.

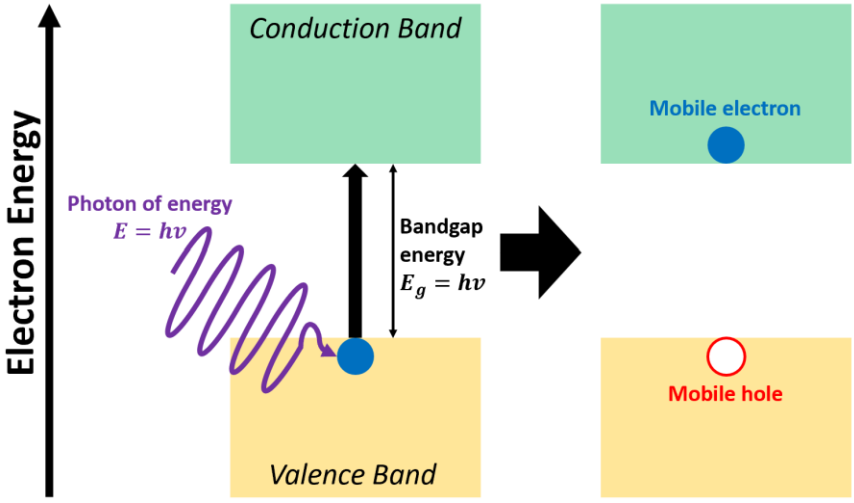


Figure 8: The internal photoelectric effect

These new charge carriers, if generated inside the depletion region, can then be accelerated by the localized electric field towards the terminals of the device (holes are accelerated towards the P-region, the anode, and electrons are accelerated towards the N-region, the cathode) [8]. If enough electron-hole pairs are generated and the terminals of the photodiode are connected to an external circuit, a photocurrent can be observed from the movement of charges. It is in this manner that a measurable current can be induced in the device through exposure to light. Although electron-hole pairs can be generated outside of the depletion region, the movement of such pairs is too slow (without the depletion electric field to provide a means of acceleration, charges need to be transported via diffusion) and the recombination rates too high (e.g. electrons generated in the P-region tend to recombine with holes before diffusing over to the

N-region) to grant them any significant consideration. It is for this reason that larger depletion regions are desired in photodiodes, hence the purposeful design of devices with larger intrinsic regions between the P-regions and N-regions known as PIN (P-Intrinsic-N) diodes and the use of reverse biasing, which increases the depletion region width in the diode by pulling the mobile carriers away from the junction area, creating more immobile acceptor/donor ions (yields a stronger depletion electric field) [9].

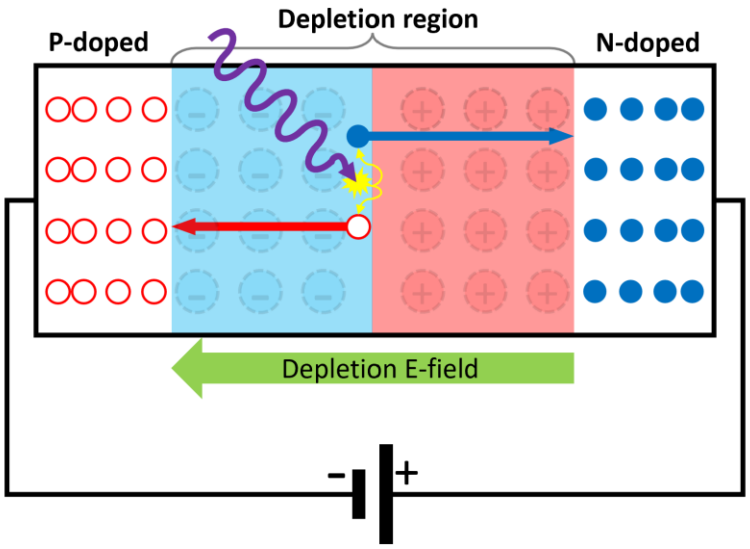


Figure 9: Typical PN photodiode operation

2.3 APDs, SPADs and Quenching Basics

Regular photodiode operation is technically capable of detecting light, but it still requires a fair amount of illumination before it can generate enough charges to produce a significant current signal, making it an inappropriate choice for photodetection when dealing with low-intensity light sources. A device that attempts to address this concern is the avalanche photodiode, a photodiode variant that leverages charge multiplication to incorporate an internal

gain mechanism by generating an “avalanche” of charges rather than just one electron-hole pair per photon. Charge multiplication in an APD is enabled by impact ionization [9], a process by which an electron imparts enough kinetic energy via direct collision with an atom’s valence electron for it to transition to the conduction band, ionizing the atom in the process.

When the reverse bias across a photodiode approaches its breakdown voltage, it will exhibit avalanche photodiode behavior due to the increased width of its depletion region and significant increase in its electric field. This electric field becomes capable of accelerating photogenerated electron-hole pairs to the point of colliding with other electrons in the lattice to create new pairs, which in turn are also accelerated thus repeating the process until all of the generated carriers have left the device, causing the avalanche to die out on its own. It is worth noting that although holes are not physical particles themselves, they can still induce impact ionization by causing a neighboring valence electron to “fall into” the hole, creating a proxy electron that, now possessing the kinetic energy of the original hole, can collide with another electron.

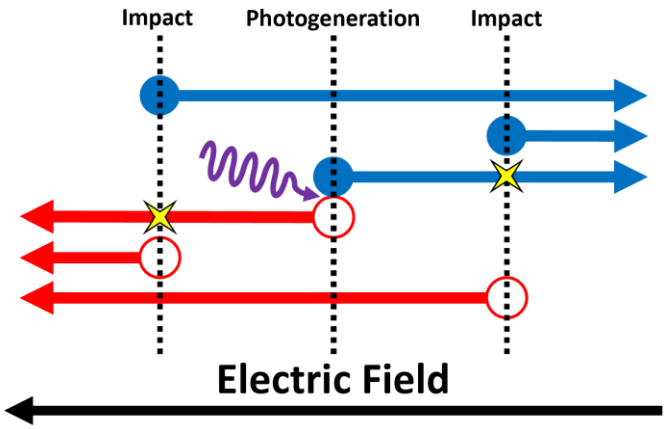


Figure 10: Avalanching process

Although APDs used in this manner can exhibit gains ranging from 10 to 1000 [5], they still do not quite offer the necessary gain to provide a prominent signal alerting to the arrival of a single photon. For those applications, the photodiode must instead be biased beyond the breakdown voltage and operated in Geiger mode as a single-photon avalanche diode, the functionality of which is akin to how Geiger counters detect radiation [7]. Unlike APDs, where the charge multiplication events are finite, controlled and of limited gain, SPAD avalanches are self-sustaining and thus ideally of infinite gain, which is owed to the extreme overvoltage biasing that gives rise to a much stronger electric field and a significantly wider depletion region. At such a level of biasing, a great majority of the electron-hole pairs undergo impact ionization, and the rate at which new charges are created meets or exceeds the rate at which charges leave the device. As a result, SPADs have the unique ability to convert a single photon absorption event into a complete avalanche breakdown of the device capable of supplying a current pulse in the milliampere range in less than a nanosecond [10]. Figure 11 illustrates the various operating regions of photodiodes and how each device variant responds to increasing light intensity.

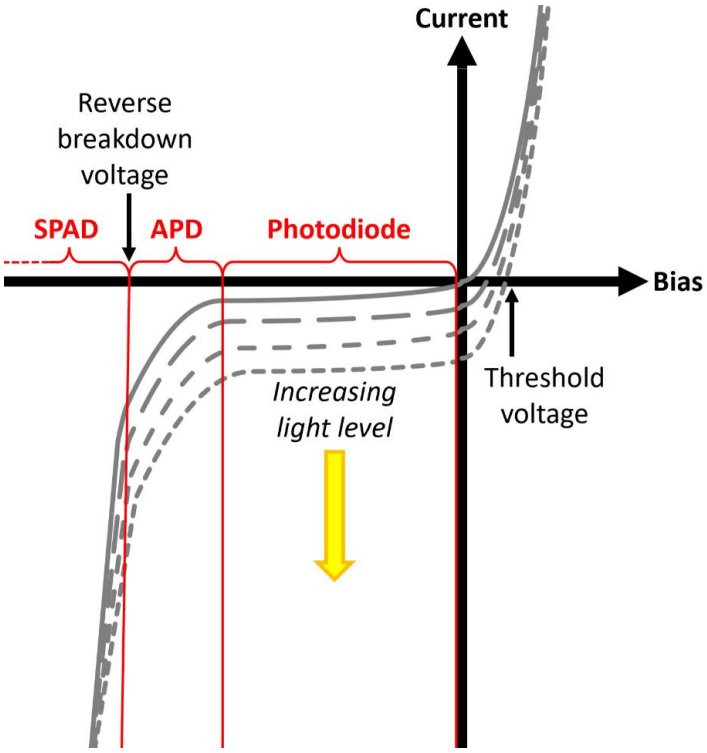


Figure 11: IV curves of photodiode modes of operation

Contrary to the other photodiode variants, the photocurrent of a SPAD does not vary with the light level and instead operates in a binary on/off fashion contingent on a photon's arrival. Taking this into consideration, the merits of the photon counting methods discussed in section 2.1 become clear, as they provide the means by which SPADs can be used to discriminate between varying light intensities. Because of the uncontrolled nature of SPAD breakdown events, special measures must be taken to limit the intensity and duration of the current pulses that result. In order for the avalanche of a SPAD to be halted, its bias must be reduced to a voltage below the breakdown voltage, a process known as quenching. Possible consequences of failing to effectively quench a SPAD during an avalanche include prolonged dead times, overvoltage damage to connected circuitry and, in the worst case, thermal destruction of the

device itself due to excessive current flow. Quenching techniques for SPADs fall into two main categories: passive and active quenching [5].

Passive quenching relies on a resistive load connected in series with the SPAD to reduce the bias as the avalanche current creates a voltage difference across the load. It is the easiest method to implement with the disadvantage being that the time it takes for the SPAD to recharge back up to a bias greater than the breakdown voltage is heavily dependent on the resistance used and the internal junction capacitance of the SPAD. In many cases, the resulting RC time constant inherent to passive quenching can make the dead time too long for the desired application. Active quenching, on the other hand, performs a hard reset on one of the SPAD terminals through active circuitry (transistors) by directly forcing a high (or low) voltage on the anode (or cathode). This method allows for much faster performance at the expense of layout area, power consumption and circuit complexity. In some cases, passive and active quenching can be combined to reduce the complexity of the circuit. In these hybrid active schemes, passive quenching is used to start the initial stage of the quench (starts reducing the bias across the SPAD) until active quenching can take over and conclude the quenching process. In this manner, the simplicity offered by the passive technique can be taken advantage of for the beginning of a quench while still yielding the fast reset times offered by active methods.

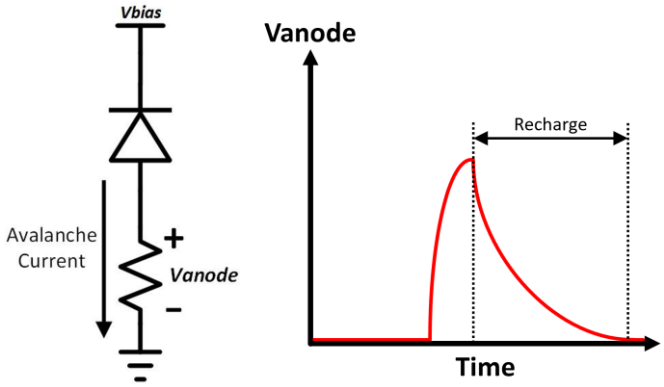


Figure 12: Passive quenching operation

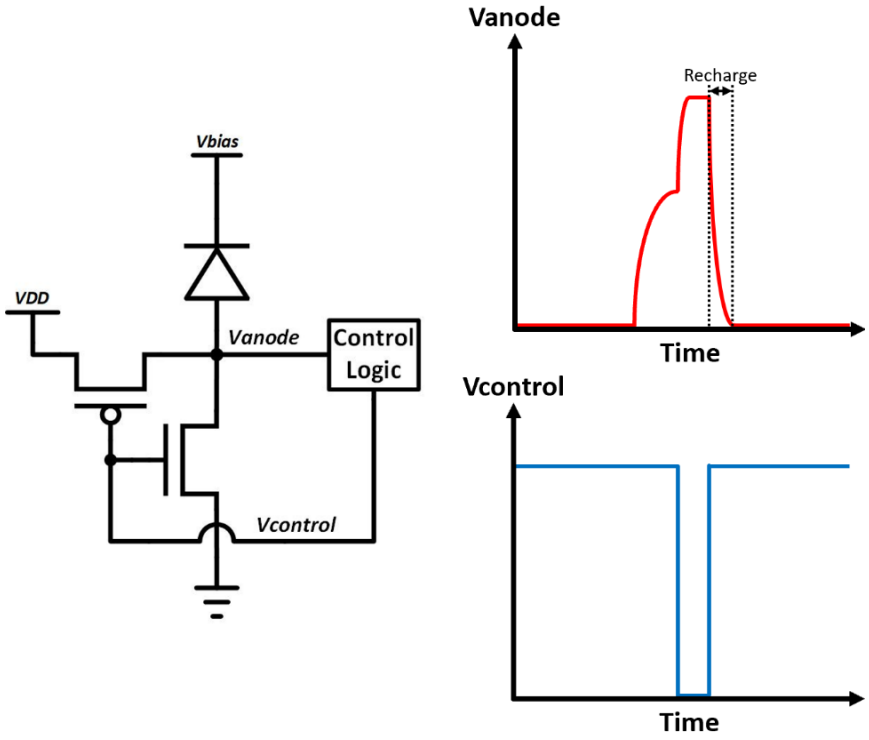


Figure 13: Active quenching operation

Additional characteristics that are important to consider in a SPAD besides the dead time are dark counts, after-pulsing, leakage current, crosstalk, time delay, jitter, and photon detection efficiency (PDE) [10]. Dark counts, as mentioned in section 2.1, are a byproduct of thermally generated electron-hole pairs that, when exposed to the high electric fields in a SPAD's depletion

region, can cause unintended avalanche events despite the absence of light. Common dark count countermeasures include subtracting the estimated dark count from the final output count and operating the device at lower temperatures to reduce thermal excitation of electrons. After-pulsing is a similar phenomenon where residual charges from an earlier avalanche event are “trapped”, or slowed down, in the depletion region due to defects in the semiconductor lattice and then subsequently accelerated to the point of causing extra avalanches later in time [11]. The most practical mitigation technique for these extra pulses is to incorporate fast quenching that prevents the SPAD from avalanching any more than it needs to, meaning that the residual charges then have less time to undergo acceleration through the electric field.

Leakage current is the small, but constant current that is conducted due to the reverse biasing of a SPAD and in an ideal device this parameter would be zero amps. However, due to imperfections in the diode structure outside of the depletion region, at the semiconductor/oxide interface for example [11], leakage currents can develop and cause issues such as premature quenching (as will be observed in chapter 5). Unlike thermally generated and trapped charges, charge carriers from the leakage current do not undergo charge multiplication because their conduction path does not pass through the depletion region. The previous statement is better understood by considering that real SPADs are not literally shaped as portrayed in figures 6 and 9. Chapter 3 sheds some light on the actual structures commonly used to implement these detectors.

Crosstalk is another unwanted effect that causes extra photon detections and is specific to detectors where multiple SPADs are fabricated in close proximity to one another. During a charge multiplication event, there are instances where an electron can recombine with a hole. If such an electron were to possess enough energy immediately prior to transitioning from the

conduction band to the valence band, radiative recombination can occur, which results in the spontaneous emission of a photon with an energy equivalent to that which was lost by the electron [7]. The emission of this photon can then optically trigger any SPAD that happens to be within the vicinity. The severity of crosstalk in a detector can be reduced by increasing the distance between the SPADs in the array and, if the manufacturing process allows, the inclusion of optical barriers between pixels [11].

Time delay and jitter are closely related factors that heavily influence the temporal accuracy with which a SPAD can resolve a photon signal. The time delay, as the name would suggest, is the time that typically elapses between the arrival of a photon and the resultant output pulse peak [12]. It is dependent on the nominal amount of time it takes for an avalanche current pulse to be initiated and reach the terminals of the device, which in turn is heavily influenced by the structure of the SPAD itself [10]. Jitter, also referred to as the timing resolution, describes the level of uncertainty surrounding this time delay and is typically quantified by observing the time variation in the leading edge of the output pulse [12]. In an ideal detector, every signal generated by each photon would produce an output with the exact same delay, but due to the stochastic nature of avalanche events, this does not hold true. Specific factors that contribute to jitter include the SPAD's structure type, the wavelength of the incident light and the specific location within the depletion region where the photogenerated charges are initially created [12].

Lastly, the photon detection efficiency (PDE) describes the probability that a SPAD can successfully detect an incident photon. The PDE is calculated by taking the product of the photon detection probability (PDP), which is the product of the quantum efficiency (QE) and the avalanche triggering probability (ATP) [13], and the fill factor (FF), the latter being a metric that

describes the ratio between the photosensitive active area and the space taken up by the rest of the SPAD or pixel [5].

$$\mathrm{PDE} = \mathrm{PDP} \cdot \mathrm{FF} = \mathrm{QE} \cdot \mathrm{ATP} \cdot \mathrm{FF} \quad (1)$$

While a majority of a SPAD's PDE is determined by its physical layout, the fill factor of a SPAD pixel can be maximized by minimizing the surface area occupied by the circuitry connected to the device. Improvements in the fill factor are one of the reasons for transitioning from a 350nm process to a 180nm process (in addition to speed) for this thesis.

2.4 High-Energy Physics Application

Subcritical experiments involve the testing of nuclear materials without the formation of a critical mass and without the creation of a self-sustaining nuclear reaction [1]. By using gamma/neutron diagnostics, information about a radioactive source's underlying characteristics can be determined. At the most basic level, a radiation detector will typically operate by generating a certain amount of charge through a current that is linearly related to the quantity of radioactive interactions taking place within the detector (the mechanism for current generation will vary depending on the detector type) [13].

There are three main methods of radiation detection: pulse mode, current mode, and mean square voltage (MSV) mode. Pulse mode measurements are intended for applications where the detection of singular radiation quanta is required, and provides an output of current pulses corresponding to the arrival of each radioactive particle. Current mode measurements will instead generate a current that follows the time-averaged amount of charge generated by all of

the radiation events combined and are more tailored for high event rates. MSV mode is similar to current mode, with the exception that only the variance, or mean square value, of the average current is considered and is commonly used in mixed radiation environments to distinguish between higher and lower energy nuclear emissions [13]. For the prompt gamma/neutron signatures being considered, pulse mode cannot be employed due to the extensive overlapping of radiation arrival times nor can MSV mode be used since the diagnostic being performed is more concerned about the total energy generated by the high radiation flux source, which is why current mode is used.

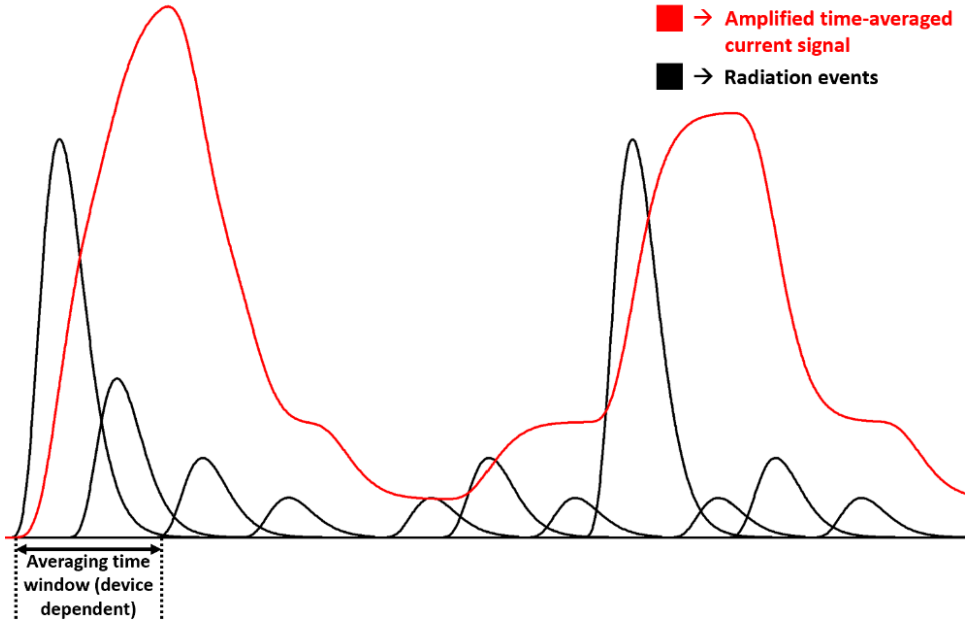


Figure 14: Simplified current mode operation (averaging window is determined by the response time of the measuring device)

A typical prompt radiation experiment will usually involve the exposure of a fast-scintillating material to a radioactive sample, with a photomultiplier coupled to the scintillator to convert any light into an amplified current signal. This analog signal is then processed by

external instruments to digitize the information into data that can be more easily interpreted and analyzed. The SPAD devices and circuitry discussed in this thesis will be considered for the design of a silicon-germanium photomultiplier geared for these same kinds of experiments. The replacement of traditional photomultipliers with solid-state photon counting devices would provide a number of benefits including significantly smaller size, lower operating voltages, better durability, higher resolution, and the ability to be integrated with additional on-chip read-out circuitry capable of providing photon counts in real time, supplanting the need of an external digitizer [7].

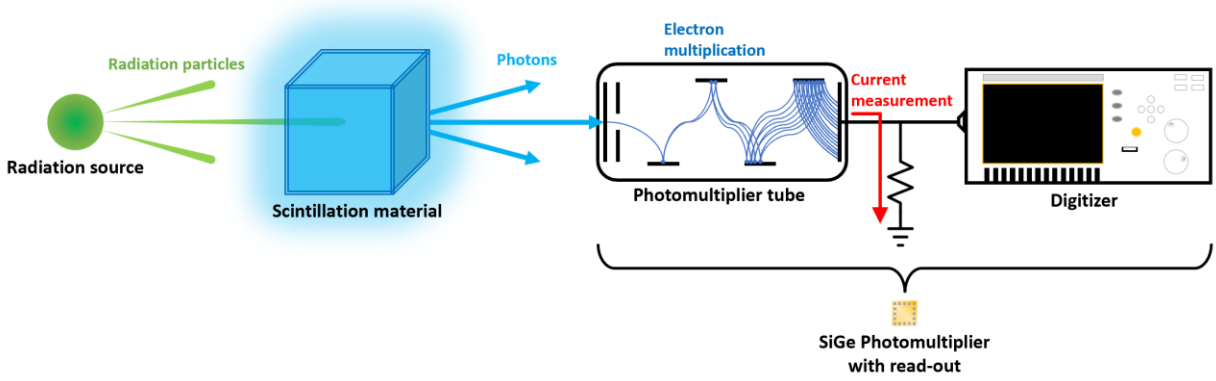


Figure 15: Proposed application

A device of this nature necessitates the use of an array of SPADs to minimize the loss of information about the optical event concerned. The rationale behind this is best understood by recalling that SPADs can only detect one photon at a time until quenched and reset. Assuming that each SPAD is small enough to ideally have a low probability of being struck by a single photon, one can increase the number of cells so that the number of avalanches from incident photons becomes increasingly proportional to the light level being exposed to the chip [13]. This design approach, combined with the bandwidth improvements offered by active quenching

techniques, results in a device with very reasonable photon count resolving capabilities for low-intensity light signals. The timing metrics that the designs will aim to satisfy include a full-width-half-max (FWHM) impulse response of 100-500ps (or faster) and a reset time of 1-2ns maximum. Meeting these performance targets would yield the foundation needed to design a photodetector with high dynamic range appropriate for the application.

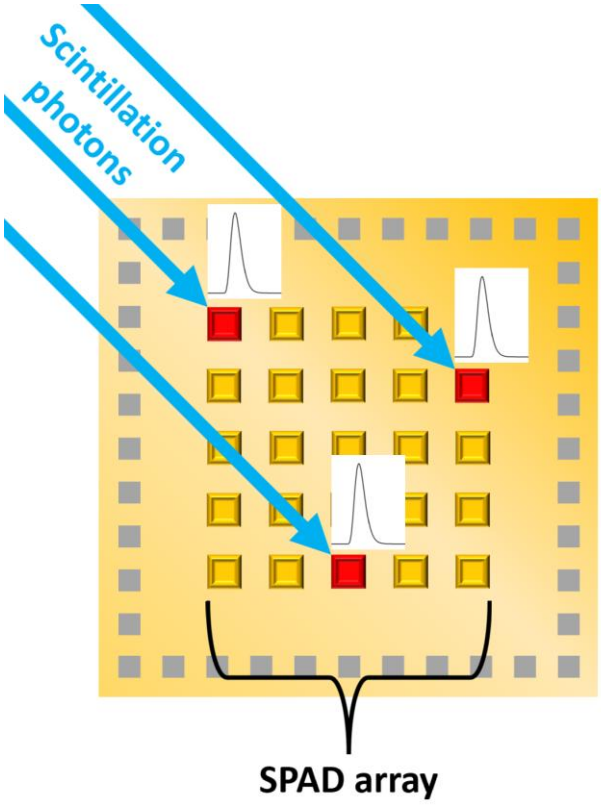


Figure 16: The use of SPAD arrays for photon counting

CHAPTER 3: SIGE SPADS

3.1 Basic SPAD Structures

In the previous chapter, the electric field of the depletion region was described as the primary mechanism that enables avalanche multiplication in APDs and SPADs. What was not discussed however, is how different device structures can play a role in the localization and intensity of the electric field that develops. The conceptualized PN structure of the diode, and by extension the SPAD, was discussed in section 2.2, but in reality, the size, doping concentrations and distribution of the doped regions can vary depending on the intended application and device type. The SPADs discussed in this thesis, for example, will be integrated into TowerJazz's BiCMOS process, a technology not necessarily meant for SPAD design. In such cases, process layers provided by the process design kit (PDK) are usually repurposed and used in ways that can violate the design rules that would normally apply to CMOS devices. Alternatively, if a dedicated technology process meant specifically for SPAD design were used instead (much more costly), the process layers available would lend themselves better to taking full advantage of the underlying physics needed to achieve efficient absorption and charge multiplication. The drawback to these dedicated processes however is that they are not nearly as compatible with interfacing with electronics as those designed with commercial CMOS/BiCMOS processes, mostly due to their much higher operating voltages [10].

The two main categories of SPAD structures are thick and thin SPADs. Thick SPADs, which are common in dedicated and PIN diode processes [14], are devices that have depletion layers tens of micrometers long [10], and will often separate the zones where photon absorption and charge multiplication take place. These devices are commonly referred to as separate absorption and multiplication (SAM) SPADs. The segmentation of the two regions helps ensure

that only one of the two mobile charge carriers (electrons or holes) ionizes appreciably, which provides more control over the avalanche gain in cases where the APD mode of operation is preferred [7]. This is commonly achieved by using a combination of thick P-epitaxial layers, which are lightly doped and form the depletion layer, and more heavily doped P and N layers that form the anode and the cathode. In addition to considerable control over charge multiplication dynamics, thick SPADs boast high photon detection efficiencies, a benefit owed to the width of their depletion regions that provide larger photosensitive areas. Larger depletion areas also allow for better detection of light with longer wavelengths [11], but have the disadvantage of introducing longer time delays and increased jitter compared to their thin SPAD counterparts due to the longer distance carriers need to travel before reaching the avalanche zone. Figure 17 shows an example of a thick SPAD structure along with a simplified cross-section to illustrate the charge densities that give rise to the device's electric fields.

Thin SPADs on the other hand, have depletion layers of only a few micrometers, use fewer complex layers and usually have much lower breakdown voltages [10]. The simplicity of their structure thus makes them popular to implement in standard CMOS/BiCMOS processes. The structures of most thin SPADs are more reminiscent of typical diodes and can be formed by using a deep N-well for the cathode, with N-doped regions added for contacts, and a P-doped area as the anode. Without a thick, lightly doped epitaxial layer to extend the depletion region, what develops is a small but intense localized electric field where both absorption and avalanching takes place. Because of this shallower photosensitive area, thin SPAD photodetection efficiencies for long wavelengths of light pale in comparison to thick devices, but they perform reasonably well for shorter wavelengths such as blue light (common for scintillators). Thin structures also offer shorter carrier transit times, which improves transient

performance. Figure 18 depicts an example of a thin SPAD structure in a similar fashion to figure 17.

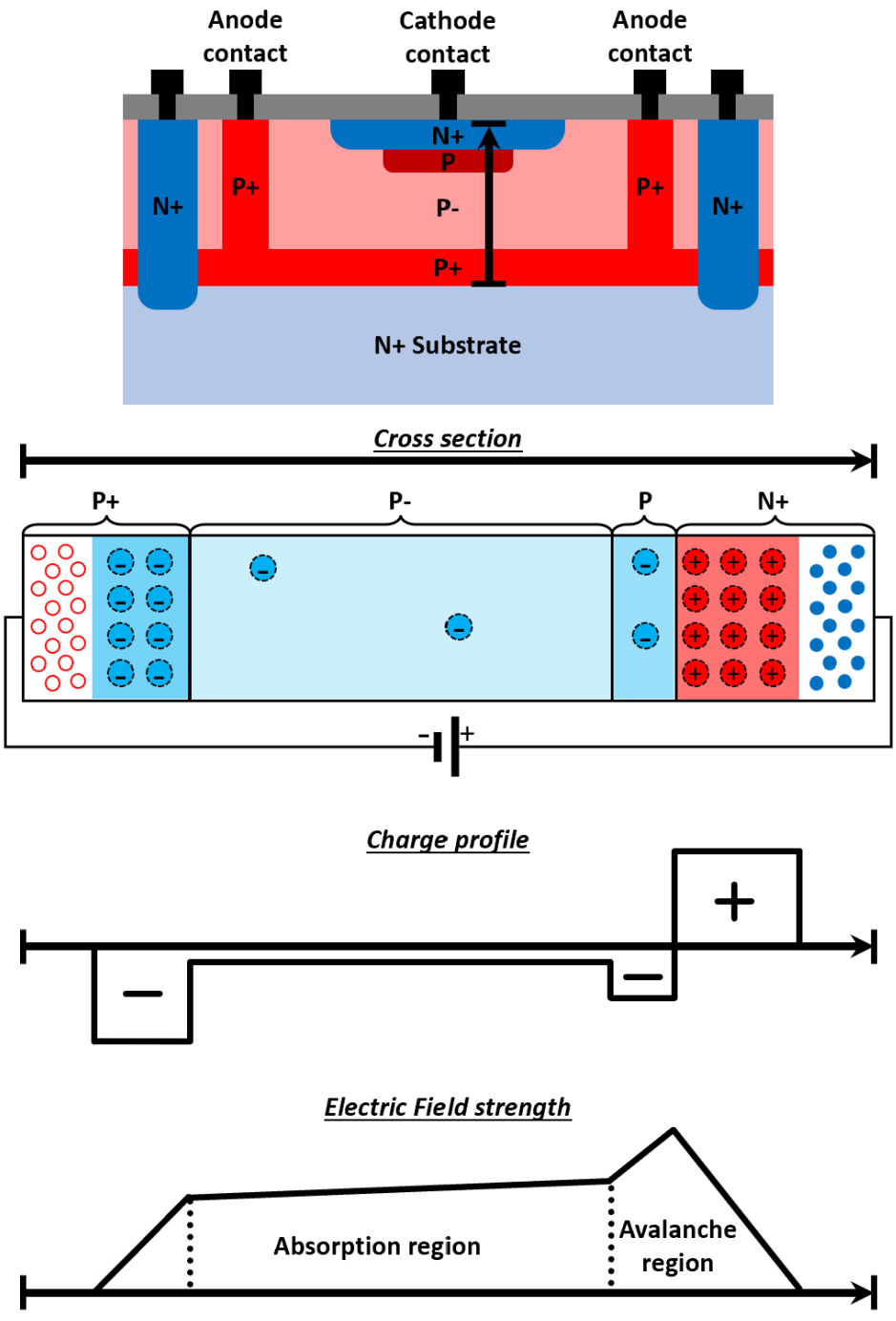


Figure 17: Thick SPAD structure and properties

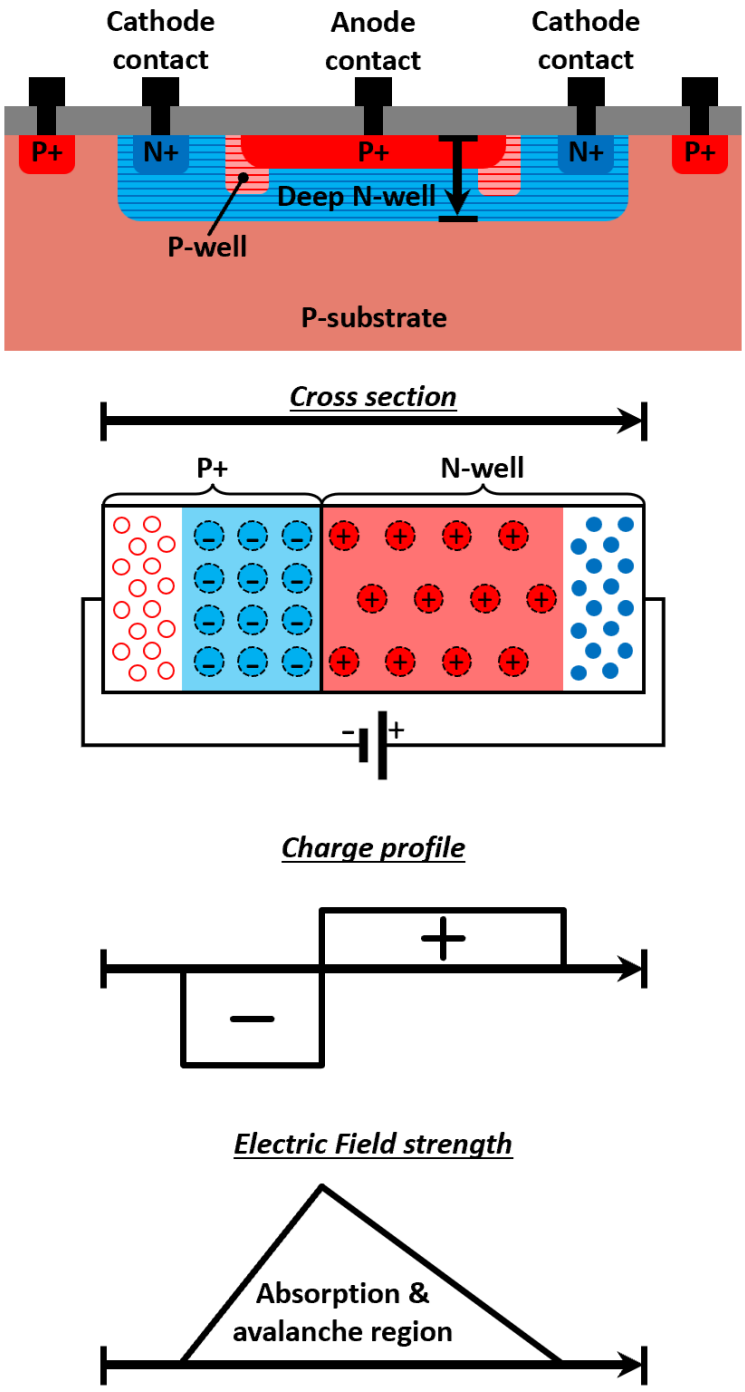


Figure 18: Thin SPAD structure and properties

Note the inclusion of the P-wells in figure 18. The placement of lightly doped guard ring implants around the anode of a SPAD is a common measure taken to prevent premature edge

breakdown of the device due to electric field crowding effects that can arise from the curved junctions between the P+ and N-well. It is worth reiterating that the structure of thin SPADs will be heavily dependent on the design layers available in the PDK being used, so the effectiveness and feasibility of features like guard rings and device-substrate isolation will vary from process to process.

3.2 350nm SiGe AMS Designs

The decision to utilize silicon-germanium thin SPADs for this project was made based on the need to detect light in the blue region spectrum of 405nm-460nm. The use of silicon-germanium yields lower bandgap energies than silicon alone, which improves the photon detection efficiency for the specified wavelengths. Furthermore, a thin SPAD structure increases the probability of short wavelength photons generating charge carriers within the depletion layer of the diode because of its proximity to the surface (the shorter the wavelength is, the less distance the photon can penetrate into the material). Another benefit to using SiGe for SPAD design is that it is an indirect bandgap material, meaning that the minimum energy of its conduction band and the maximum energy of its valence band have different electron momentum values within the material's structure, so in order for an electron in the conduction band to fall into the valence band it must first undergo a significant change in momentum (in a direct bandgap material the momentums would be the same for both) [7]. The benefit to this is that radiative recombination of charge carriers becomes much less likely to occur, meaning that the risk of crosstalk is effectively reduced.

The original SPADs developed by Dr. Baker's research group were designed using the Austriamicrosystems (AMS) 0.35µm SiGe BiCMOS (S35) process, a technology that features

layers allowing for the design of SiGe heterojunction bipolar transistors (HBTs), which are a special type of improved performance bipolar junction transistor where different semiconductor materials are combined as opposed to using the same material for all three sections (base, collector, and emitter) of the device. The HBTs in the S35 process use silicon-germanium for the base and silicon for the collector and emitter. A diagram showing a cross-section of the layers available in this process is shown in figure 19.

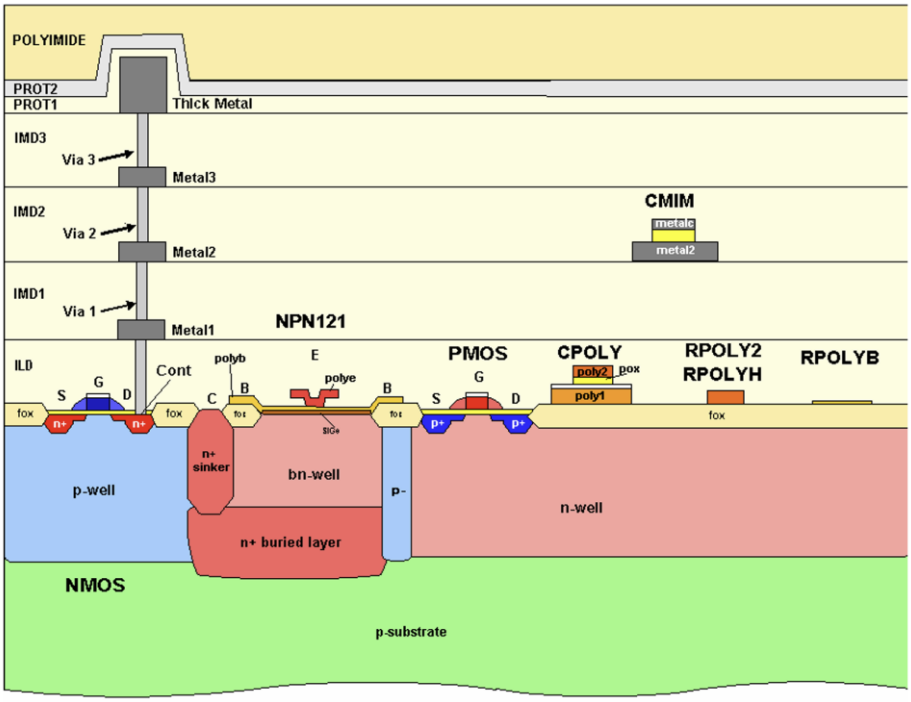


Figure 19: AMS S35 process cross-section [15]

To acquire a PN junction with this process, the NPN HBT structures were modified by deleting the N-doped polysilicon emitter layer, leaving only the P-doped SiGe base and the N-doped collector behind. Figure 20 shows a basic illustration of the device that results from this approach. A large number of different SPAD structures were designed in this manner with varying shapes, sizes, n-epitaxial/N-well types, and other configurations from a prior research

endeavor of Dr. Baker's lab [16]. In these designs, the buried N+ layer provides effective isolation from the substrate and by extension nearby SPADs.

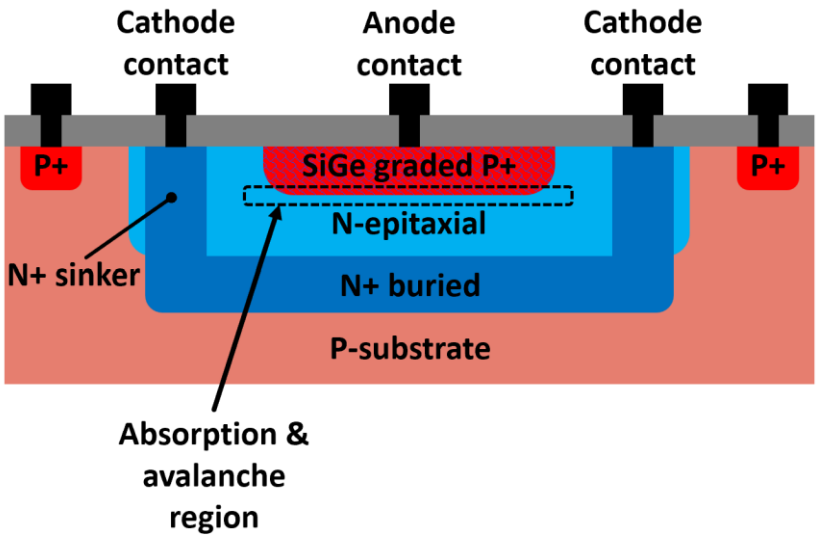


Figure 20: Simplified AMS S35 process SiGe SPAD structure

3.3 Batch testing of SiGe SPAD Variants

Before any active quenching circuitry could be designed, it was necessary to experimentally determine the behavior of the SiGe SPAD structures in order to determine how much current they actually supply during avalanche events. This is an important parameter to establish because every transistor that connects to the SPAD contributes additional oxide capacitance that can attenuate the current pulse. If too many transistors are added, or the transistors made too large, the avalanche signal can become too small or slow to trigger the circuit, so a careful compromise between transistor responsivity and pulse size/speed must be reached. Another purpose behind testing the variants available was to determine what structures yielded the fastest pulse widths and reset times, with the best performing device to be tested

more thoroughly and considered as a strong candidate for integration into the final chip design. The results of these experiments helped lay the foundation for the SPICE modeling efforts covered in chapter 4.

SPAD-connected transistor size/quantity	Small ⟷ Large
Transistor responsivity	
SPAD pulse size/speed	

Table 1: Effects of transistor size/quantity in active quenching circuits

A trio of dies (hereafter referred to as chips 1, 2 and 3) developed by prior researchers contained all of the experimental SPAD structures, with many copies having been manufactured, wirebonded to TO-8 packages, and soldered to printed circuit boards (PCBs) previously designed by James Skelly for testing. Each board can accommodate a maximum of three SPAD structures at a time using three SMA connectors (one per anode) and three BNC connectors (one per cathode). Footprints added for the population of resistors for both the anode and cathode terminals were also available on the PCBs. To simplify the tracking of testing data, all of the boards were assigned a unique number and each SPAD structure defined by a two-character alphanumeric identifier consisting of the chip number and the letter pertaining to the structure type. Tables 2, 3 and 4 list the identifiers created for all of the structures available. Only devices that were previously wirebonded to a useable package were tested.

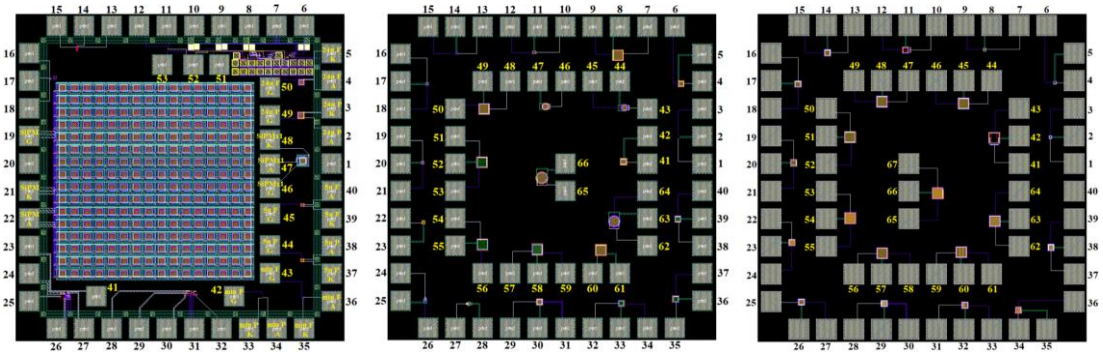


Figure 21: From left to right, chips 1, 2 and 3

ID	SPAD type
1A	Min-P
1B	Min-F
1C	5µ-P
1D	5µ-F
1E	24µ-P
1F	24µ-F
1G	SiPM Pixel
1H	SiPM Array

Table 2: SPAD identifier list for chip 1

ID	SPAD type
2A	5µ Elementary
2B	24µ Elementary
2C	50µ Elementary
2D	5µ Standard
2E	5µ BPOLY/PPLUS Smaller
2F	5µ BPOLY/PPLUS
2G	5µ No EMITT
2H	5µ No Sub
2I	5µ Circle
2J	5µ Circle No Sub
2K	24µ Standard
2L	24µ BPOLY/PPLUS Smaller
2M	24µ BPOLY/PPLUS
2N	24µ No EMITT
2O	24µ No Sub
2P	24µ Circle
2Q	24µ Circle No Sub
2R	50µ Standard
2S	50µ BPOLY/PPLUS Smaller
2T	50µ BPOLY/PPLUS
2U	50µ No EMITT
2V	50µ No Sub
2W	50µ Circle
2X	50µ Circle No Sub

Table 3: SPAD identifier list for chip 2

ID	SPAD type
3A	5µ TUBBUR
3B	5µ TUB
3C	5µ noBNTUB2
3D	24µ Cyl
3E	24µ TUBBUR
3F	24µ TUB
3G	24µ noBNTUB2
3H	24µ Striped BNTUB2
3I	24µ Striped BUR hTUB
3J	24µ Striped BUR Half TUB
3K	24µ Striped TUBBUR
3L	24µ Striped Half BNTUB2
3M	24µ Striped Half TUB hBUR
3N	50µ Cyl
3O	50µ TUBBUR
3P	50µ TUB
3Q	50µ noBNTUB2
3R	50µ Striped BNTUB2
3S	50µ Striped BUR hTUB
3T	50µ Striped BUR Half TUB
3U	50µ Striped TUBBUR
3V	50µ Striped Half BNTUB2

Table 4: SPAD identifier list for chip 3

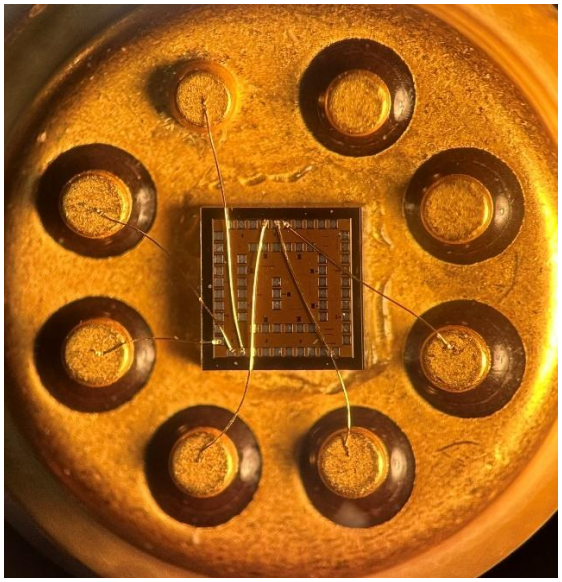


Figure 22: Chip 3 from board 14 with SPADs 3I and 3D wirebonded

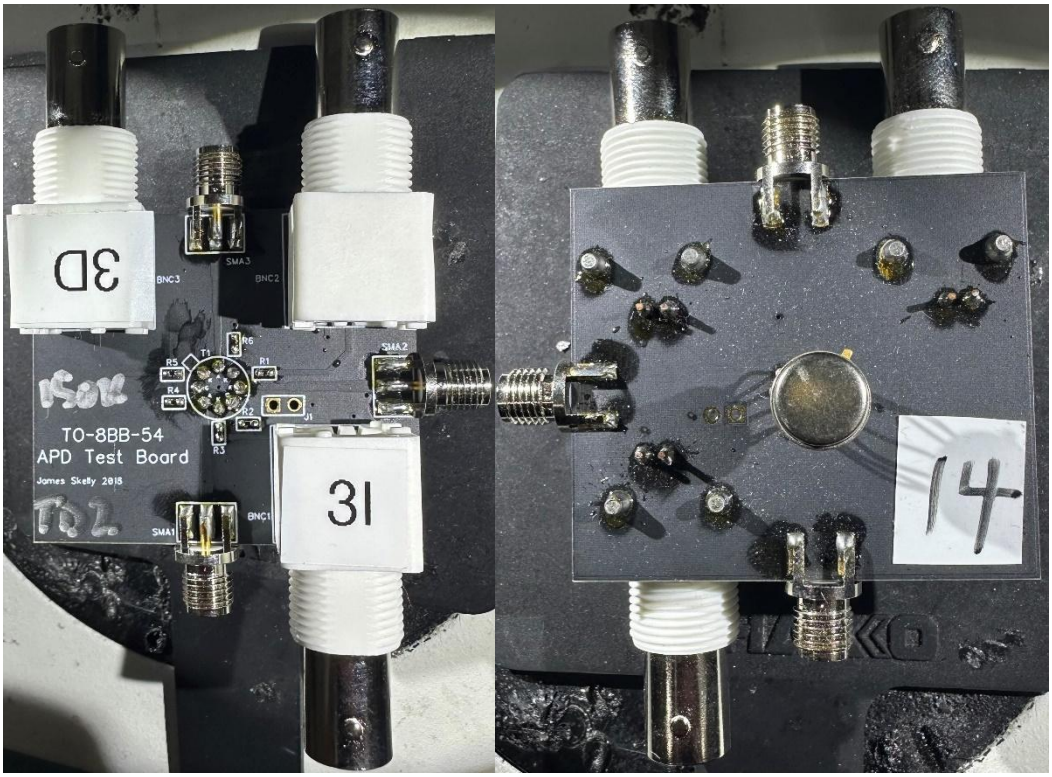


Figure 23: Board 14 front (left) and back (right)

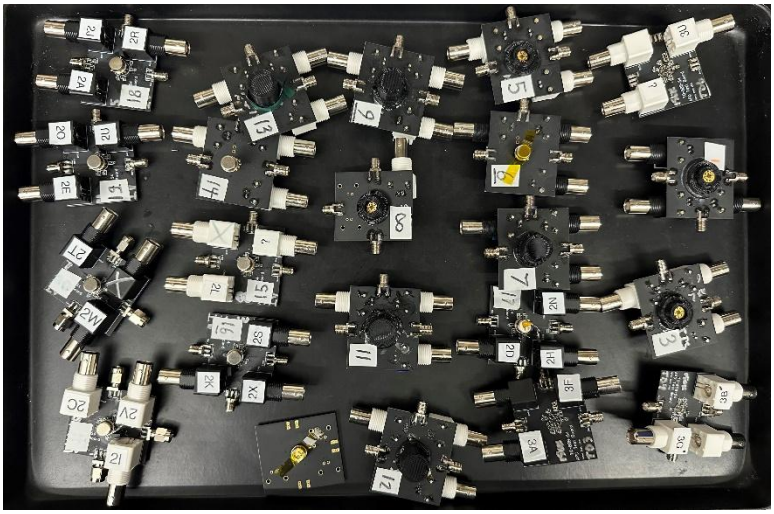


Figure 24: Assortment of SPAD testing boards

There are two main measurement methods that can be used to test SPAD devices: current mode (not to be confused with the current mode radiation detection method discussed in section 2.4) and voltage mode [17]. In current mode testing, a large quenching resistor, Rq, is placed on either the anode or the cathode to quench the SPAD while a small series resistance, Rs, is placed on the opposite terminal to capture the avalanche current pulse in the form of a voltage drop. If Rs is small enough, it is assumed that it does very little to quench the SPAD and thus provides a reasonable estimate of how much current is generated by the device during the avalanche process and for how long. As discussed in chapter 2, since the current of a SPAD continues flowing until its bias is reduced below breakdown, the settling time of current mode-generated signals can be interpreted as how long it takes for the SPAD under test to be quenched. In most cases, a 50Ω value is used for resistor Rs in order to allow impedance matching with coaxial cabling for measurements conducted with an oscilloscope.

Voltage mode testing, on the other hand, does not capture the fast current pulse through the SPAD but instead allows the user to see how the bias across the device changes over time,

particularly in the recharging phase, through an attenuated version of the diode voltage pulse. This is achieved by connecting Rs (again, usually 50Ω) in series with Rq on either the anode or the cathode. Like before, it is assumed that Rs is small enough that its contribution to the quenching of the SPAD is minimal, which allows the SPAD quenching behavior to be observed without the measurement itself interfering with its operation. While voltage mode offers a better visualization of how larger quenching resistors yield longer recharge times, the voltage divider formed by Rq and Rs results in significant attenuation of the signal and requires amplification. Current mode does not suffer from this attenuation factor and as a result is easier to implement and interpret in most cases. Figure 25 illustrates both modes of testing in anode measurement configurations.

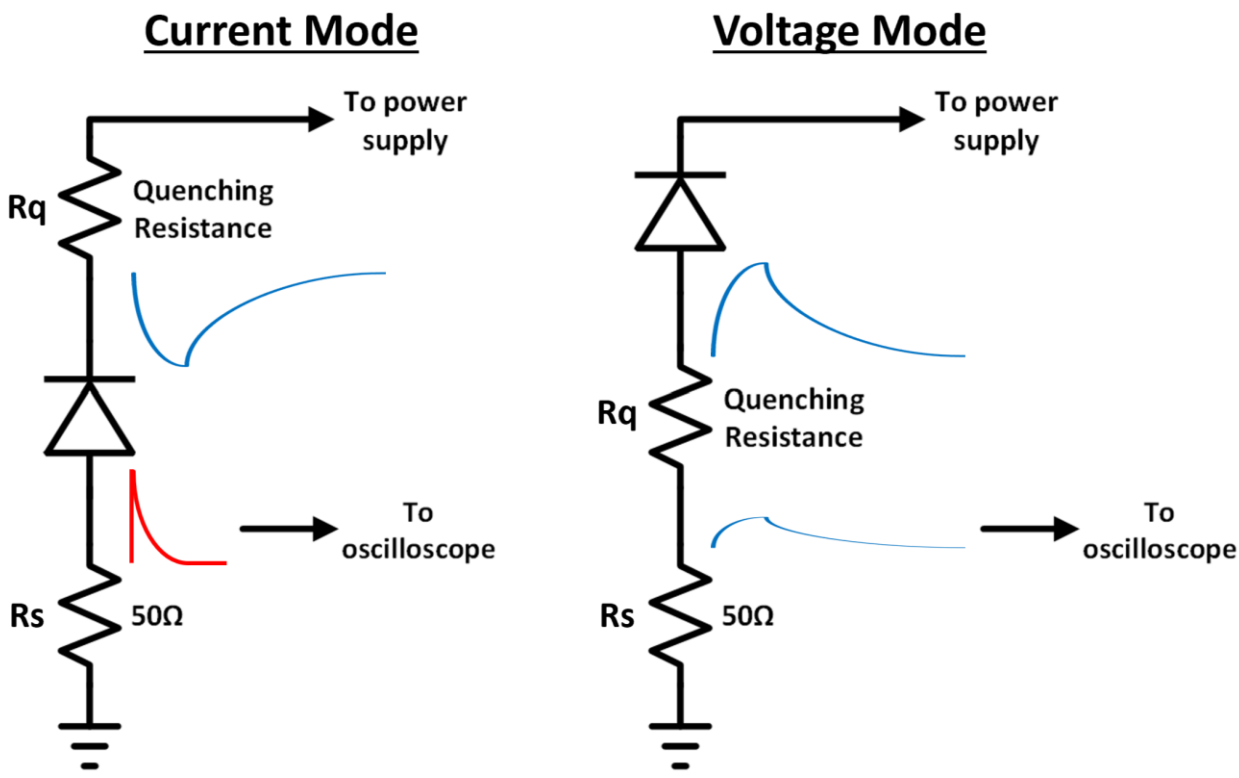


Figure 25: Current mode vs voltage mode SPAD testing

The batch of SPADs shown in figure 24 were tested using the current mode method with the Agilent Infiniium 54855A DSO oscilloscope, which has a 6GHz resolution and a sample rate of 20 gigasamples per second. Since dark counts are nearly indistinguishable from photon counts, each device was operated with a cover placed on top of the chip to reduce the density of avalanche occurrences due to incident light, allowing for better visualization of individual pulses. To conduct the tests, the bias across each SPAD was slowly increased until a notable increase in the number of voltage pulses of reasonable size was observed, at which point statistics would be run on the waveform to determine the average rise time, fall time, pulse width, and peak-to-peak voltage. For most structures, a biasing of approximately 12.5V to 13.5V was sufficient.

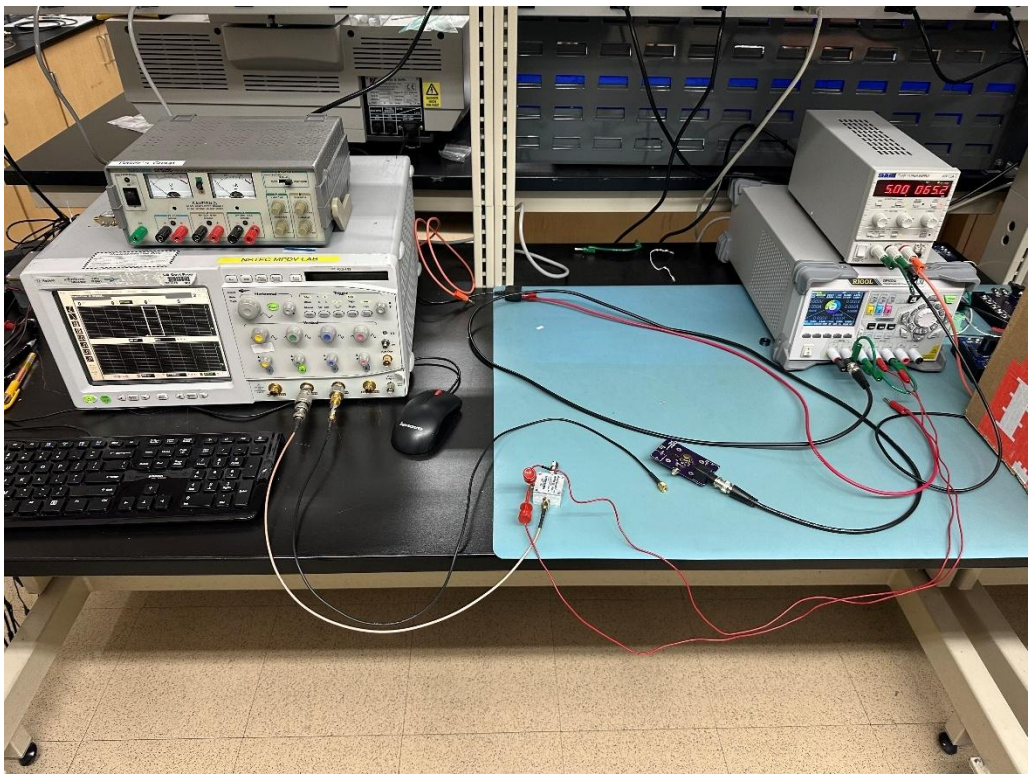


Figure 26: SiGe SPAD testing setup

For the first phase of testing, all of the structures were tested with their original cathode quenching resistor values, which varied from 0Ω to 230kΩ and was dependent on the state the boards were left in by previous users. Any devices that were deemed functional (i.e. able to generate pulses) or were not yet tested with a large enough quenching resistor from phase one were then introduced to the second phase of testing, which replaced all cathode resistors with 953kΩ or 976kΩ values. The reasoning behind using much larger values was to introduce more intense passive quenching in an attempt to mimic the speeds of active quenching in terms of the quenching time. The testing data from testing phases one and two can be reviewed in Appendix A. The result of testing phase two indicated that the fastest responding structure from the batch was SPAD 2H, a 5µm-by-5µm square SPAD without a substrate guard ring, as it exhibited a pulse width of about 171ps with a pulse amplitude of 140mV (see table 76 and figure 196 for test results).

3.4 SPAD 2H Specific Testing

With the fastest device having been identified, a series of additional tests were conducted to better determine SPAD 2H's behavior at biases no larger than 13V (to increase the longevity of the design). Initially, voltage mode testing was performed in an attempt to estimate the capacitance exhibited by the device. This was done by measuring the amount of time it would take for the anode voltage to settle after a passively quenched pulse, with the experiment being repeated with various quenching resistor values. An important factor to keep in mind when conducting such tests is that there exists a lower limit on the quenching resistance value that will allow for proper quenching operation. If the resistance is too low, the bias across the SPAD will not be reduced enough to stop the current, which will result in a continuous avalanche current

and a DC output that scales with the bias instead of the expected pulse signals (see figures 29 and 30 for examples of these DC outputs).

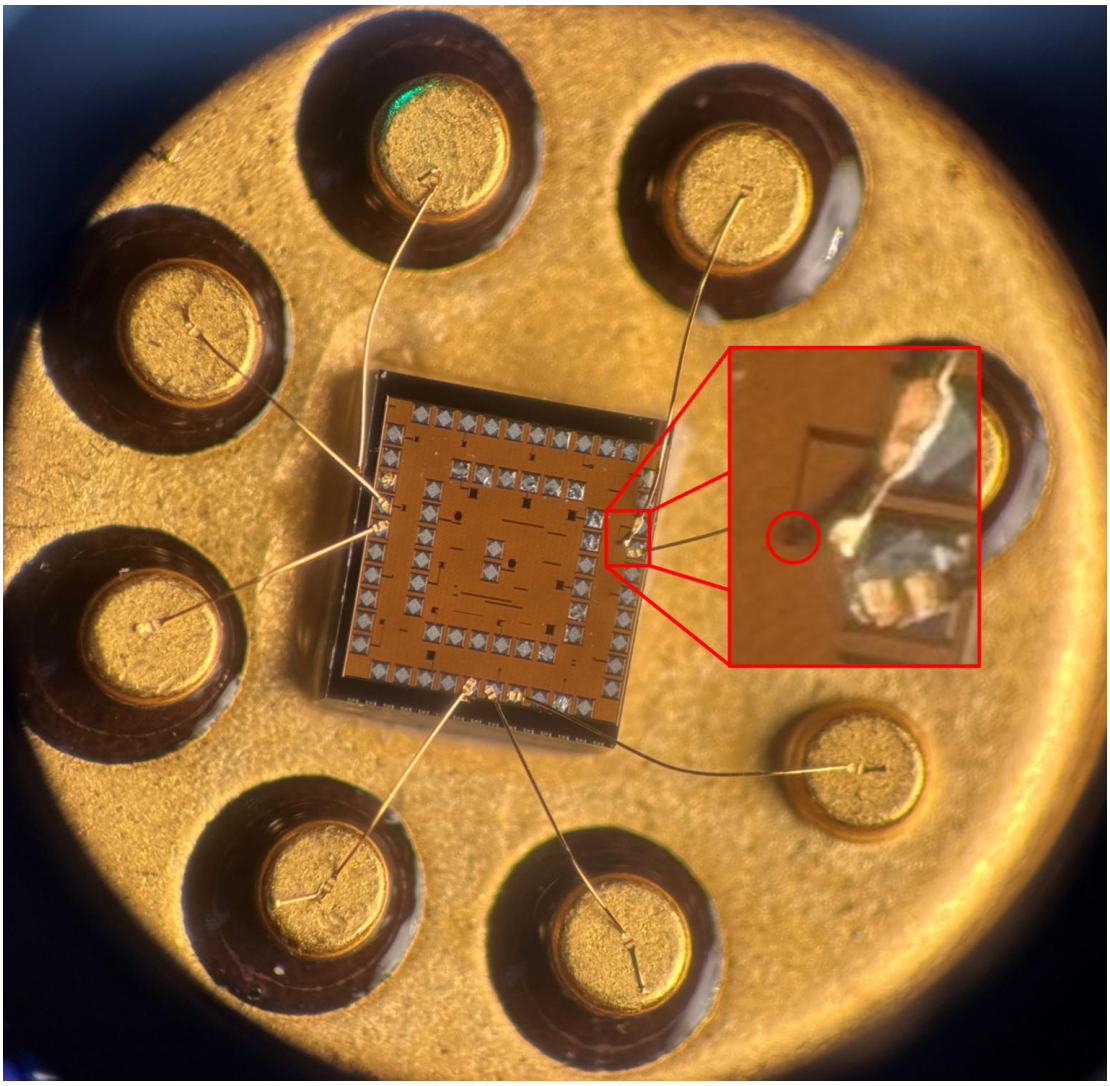


Figure 27: SPAD 2H photo

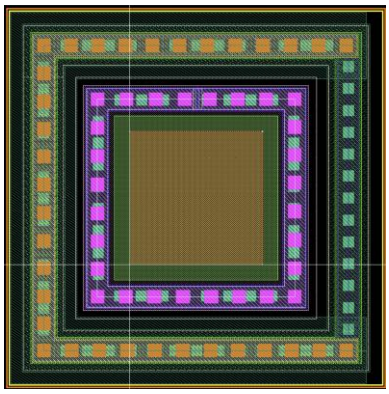


Figure 28: 5µm-by-5µm no-sub SPAD AMS layout

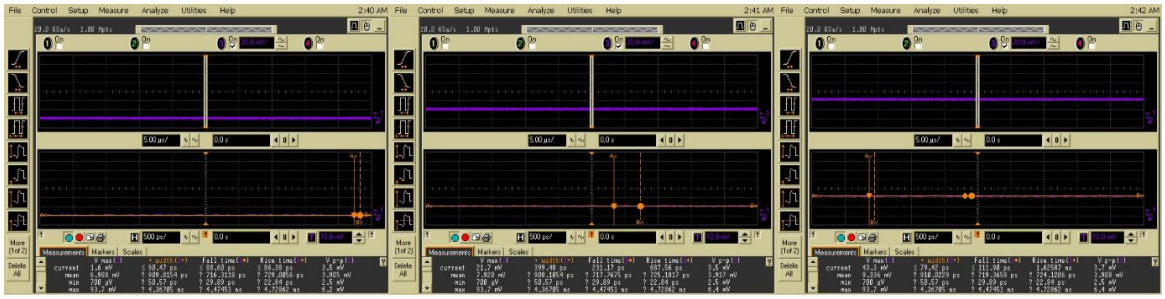


Figure 29: Voltage mode tests showing DC outputs for a 1kΩ quenching resistor with (from left to right) 10V, 12V, and 13V biasing

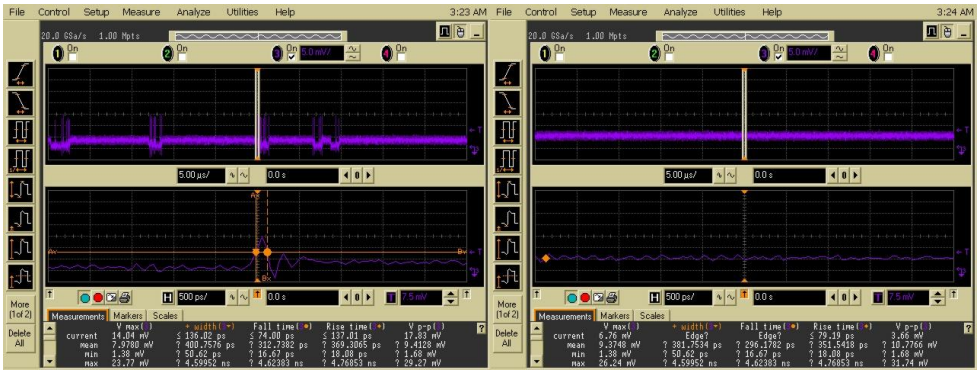


Figure 30: Voltage mode tests showing outputs for an 11kΩ quenching resistor at 12V (left) and 13V (right)

After increasing the resistance by 5kΩ increments starting from 10kΩ, it was determined that the minimum quenching resistance with which the SPAD can generate quenched pulses

reliably was around 30kΩ. Recalling the previous section, voltage mode testing inherently introduces a significant reduction in signal amplitude that requires amplification to adequately observe the recharge time of the voltage signal. To satisfy this requirement, a low noise, 0.05MHz to 500MHz bandwidth, Mini-Circuits ZFL-500+ model RF amplifier was used, and in cases where amplification alone was not enough to discern the recharge time due to noise, the Agilent oscilloscope's math functions were used to low-pass filter and magnify the signal as needed. During testing, the SPAD was measured with resistances of 30.1kΩ, 60.4kΩ, and 121kΩ, with the values being approximately doubled with each subsequent test to make it easier to detect the change in the recharge time. Due to the limited bandwidth of the amplifier itself, higher resistance values could not be tested (larger Rq values yielded faster rising-edge pulses, which increased the effective frequency beyond the RF amp bandwidth). The waveforms from voltage mode testing can be observed in figures 32-35. To calculate the capacitance acting on the device, the recharge time was assumed to be five time constants long, allowing the capacitance to be derived using the following formula:

$$C = \frac{t_{recharge}}{5 \cdot R_q} \tag{2}$$

Figure 31: RF amp used for voltage mode testing

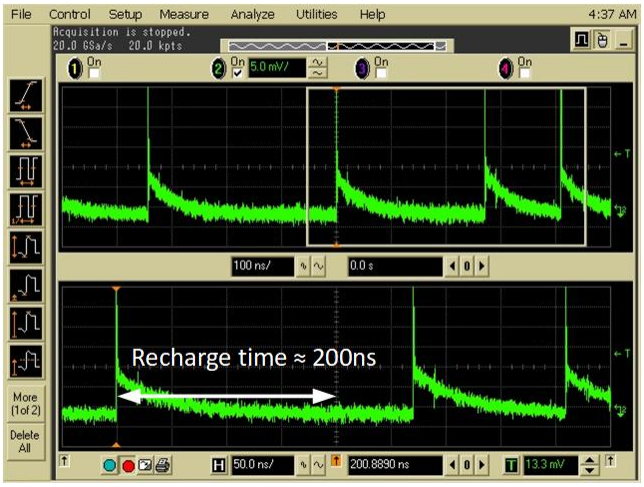


Figure 32: 2H voltage mode test with Rq = 30.1kΩ

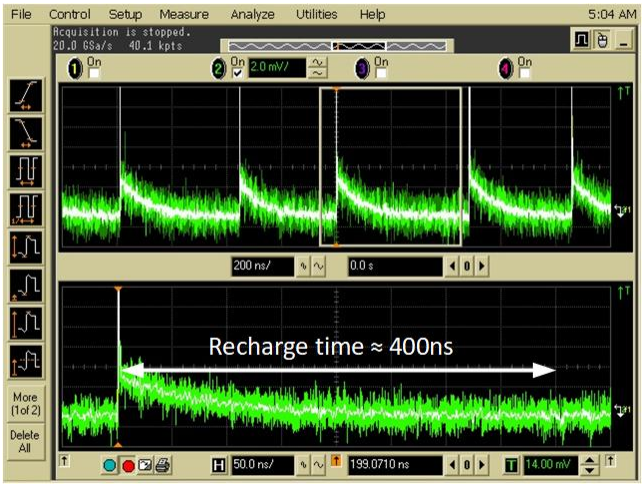


Figure 33: 2H voltage mode test with Rq = 60.4kΩ

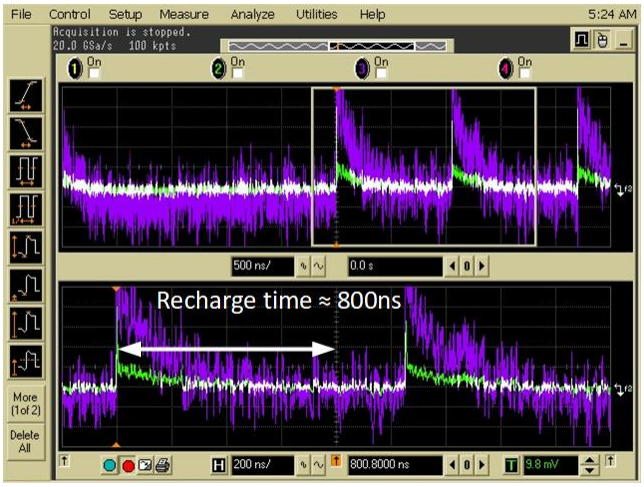


Figure 34: 2H voltage mode test with Rq = 121kΩ

Resistance	Recharge time	Inferred capacitance
30.1k	200ns	1.329pF
60.4k	400ns	1.325pF
121k	800ns	1.322pF

Table 5: 2H voltage mode testing results

The average capacitance attached to the device was calculated to be about 1.325pF, which was particularly large considering the size of the SPAD. The likely cause of this discrepancy was stray capacitance, an unintended parasitic that is introduced by the interface between the chip and the circuit board it is being tested on, which can add significant amounts of capacitance through the coupling between traces and ground planes. Furthermore, there were significant alterations that needed to be made to the PCB to allow for a voltage mode configuration that included using longer connection paths, severing and shorting traces (the boards were originally designed for current mode testing only). These alterations very likely contributed significant amounts of stray capacitance that were affecting the measurement.

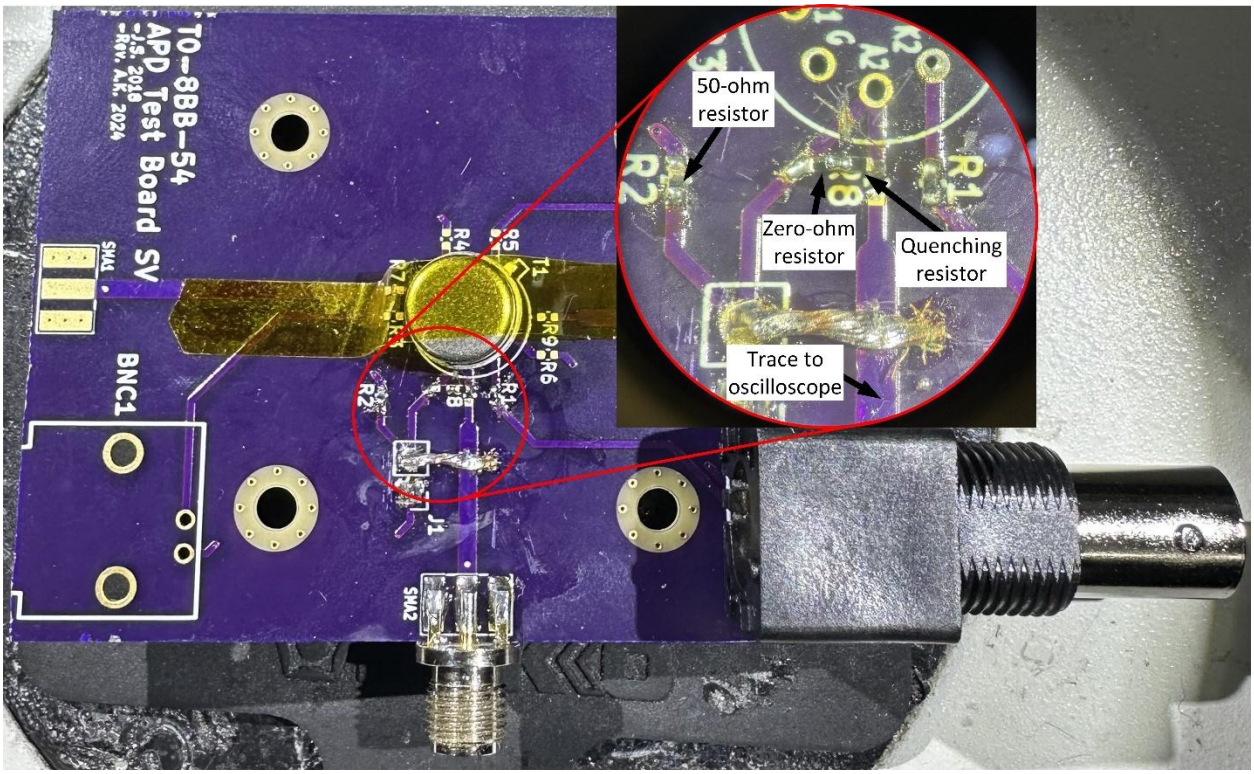


Figure 35: SPAD current mode testing board with voltage mode alterations, PCB design by Andrew Kerstetter

To circumvent this, current mode was once again settled upon to ascertain more information about the SPAD, only this time the amplitude of the current signal was observed across multiple values of Rq and various biasing levels. The specifics behind the alternative calculation of the internal capacitance of the 2H device will be discussed in chapter 4, as the derivation required assumptions that stem from the equivalent circuit SPAD model that was used.

For SPAD 2H current mode testing, the effective dark count rate (in megacounts per second) was also determined by measuring the average frequency of detected pulses of roughly the same size (the real dark count rate was much higher in reality, but consisted of pulses of all sizes). The assumption was that for every increase in the quenching resistance, the effective dark count rate should reduce in a linear manner since larger values of Rq yield longer recharge times (5RC), which would in theory increase the time elapsed between large pulses. The results are

shown in tables 6 through 11 and seem to corroborate this assumption, with the effective DCR reducing by close to half for every doubling of the quenching resistance. The current pulse magnitudes provided by the SPAD were also observed to decrease as larger resistors were used and increase with the reverse voltage bias. Furthermore, the breakdown voltage appeared to increase with resistor value by a small amount. The inferred current pulse magnitudes were calculated by dividing the voltage pulse amplitudes by the series resistance value (50Ω).

Rq = 30.1k (Measured breakdown voltage = 10.858V)			
Bias	Pulse Vmax	Inferred current pulse size	DCR*
10.858V	4.15mV	0.083mA	-
10.9V	6.35mV	0.127mA	-
11V	13.73mV	0.2746mA	2.8Mcps
11.1V	23.79mV	0.4758mA	3.5Mcps
11.2V	34.67mV	0.6934mA	3.1Mcps
11.3V	47.77mV	0.9554mA	3.2Mcps
11.4V	57.88mV	1.1576mA	3.2Mcps
11.5V	70.98mV	1.4196mA	3.2Mcps
11.6V	85.38mV	1.7076mA	3.3Mcps
11.7V	100.9mV	2.018mA	3.3Mcps
11.8V	115.8mV	2.316mA	3.2Mcps
11.9V	129.3mV	2.586mA	3.4Mcps
12V	143.6mV	2.872mA	3.6Mcps
12.1V	157.6mV	3.152mA	3.7Mcps
12.2V	168.4mV	3.368mA	3.9Mcps
12.3V	186.8mV	3.736mA	3.9Mcps
12.4V	199.2mV	3.984mA	4.1Mcps
12.5V	211.5mV	4.23mA	4.1Mcps
12.6V	222.1mV	4.442mA	4.3Mcps
12.7V	226.6mV	4.532mA	4.6Mcps
12.8V	238.4mV	4.768mA	4.8Mcps
12.9V	250.8mV	5.016mA	4.9Mcps
13V	252mV	5.04mA	4.8Mcps

Table 6: 2H current mode tests with Rq = 30.1kΩ

Rq = 60.4k (Measured breakdown voltage = 10.894V)			
Bias	Pulse Vmax	Inferred current pulse size	DCR*
10.894V	4.73mV	0.0946mA	-
10.9V	4.88mV	0.0976mA	-
11V	11.80mV	0.236mA	2.2Mcps
11.1V	19.11mV	0.3822mA	2.7Mcps
11.2V	32.07mV	0.6414mA	2.6Mcps
11.3V	43.95mV	0.879mA	2.5Mcps
11.4V	57.01mV	1.1402mA	2.6Mcps
11.5V	66.92mV	1.3384mA	2.5Mcps
11.6V	83.20mV	1.664mA	2.5Mcps
11.7V	97.16mV	1.9432mA	2.5Mcps
11.8V	114.0mV	2.28mA	2.6Mcps
11.9V	122.6mV	2.452mA	2.6Mcps
12V	136.3mV	2.726mA	2.7Mcps
12.1V	148.8mV	2.976mA	2.8Mcps
12.2V	165.1mV	3.302mA	2.8Mcps
12.3V	176.8mV	3.536mA	3Mcps
12.4V	185.8mV	3.716mA	3.2Mcps
12.5V	193.2mV	3.864mA	3.3Mcps
12.6V	199.6mV	3.992mA	3.4Mcps
12.7V	207.3mV	4.146mA	3.6Mcps
12.8V	215.2mV	4.304mA	3.7Mcps
12.9V	227.5mV	4.55mA	3.8Mcps
13V	239.1mV	4.782mA	3.9Mcps

Table 7: 2H current mode tests with Rq = 60.4kΩ

Rq = 121k (Measured breakdown voltage = 10.939V)			
Bias	Pulse Vmax	Inferred current pulse size	DCR*
10.939V	4.75mV	0.095mA	-
11V	8.83mV	0.1766mA	-
11.1V	16.46mV	0.3292mA	1.3Mcps
11.2V	26.06mV	0.5212mA	1.4Mcps
11.3V	38.10mV	0.762mA	1.3Mcps
11.4V	48.50mV	0.97mA	1.3Mcps
11.5V	59.44mV	1.1888mA	1.3Mcps
11.6V	68.70mV	1.374mA	1.4Mcps
11.7V	83.92mV	1.6784mA	1.4Mcps
11.8V	96.43mV	1.9286mA	1.5Mcps
11.9V	113.1mV	2.262mA	1.5Mcps
12V	118.83mV	2.3766mA	1.6Mcps
12.1V	130.5mV	2.61mA	1.7Mcps
12.2V	141.9mV	2.838mA	1.7Mcps
12.3V	157.8mV	3.156mA	1.8Mcps
12.4V	160.9mV	3.218mA	1.8Mcps
12.5V	163.1mV	3.262mA	1.9Mcps
12.6V	179.1mV	3.582mA	1.9Mcps
12.7V	179.8mV	3.596mA	2.1Mcps
12.8V	195.0mV	3.9mA	2Mcps
12.9V	198.3mV	3.966mA	1.9Mcps
13V	206.3mV	4.126mA	2.1Mcps

Table 8: 2H current mode tests with Rq = 121kΩ

Rq = 243k (Measured breakdown voltage = 11.047V)			
Bias	Pulse Vmax	Inferred current pulse size	DCR*
11.047V	4.75mV	0.095mA	-
11.1V	7.36mV	0.1472mA	-
11.2V	14.26mV	0.2852mA	0.6Mcps
11.3V	23.16mV	0.4632mA	0.6Mcps
11.4V	32.93mV	0.6586mA	0.6Mcps
11.5V	39.93mV	0.7986mA	0.7Mcps
11.6V	52.07mV	1.0414mA	0.6Mcps
11.7V	64.10mV	1.282mA	0.7Mcps
11.8V	73.32mV	1.4664mA	0.7Mcps
11.9V	86.80mV	1.736mA	0.7Mcps
12V	98.02mV	1.9604mA	0.7Mcps
12.1V	108.9mV	2.178mA	0.7Mcps
12.2V	104.5mV	2.09mA	0.9Mcps
12.3V	112.6mV	2.252mA	0.9Mcps
12.4V	118.6mV	2.372mA	0.8Mcps
12.5V	130.6mV	2.612mA	0.9Mcps
12.6V	149.6mV	2.992mA	0.9Mcps
12.7V	157.6mV	3.152mA	0.9Mcps
12.8V	160.8mV	3.216mA	1Mcps
12.9V	161.0mV	3.22mA	1Mcps
13V	172.1mV	3.442mA	1Mcps

Table 9: 2H current mode tests with Rq = 243kΩ

Rq = 475k (Measured breakdown voltage = 11.222V)			
Bias	Pulse Vmax	Inferred current pulse size	DCR*
11.222V	4.75mV	0.095mA	-
11.3V	8.82mV	0.1764mA	-
11.4V	14.04mV	0.2808mA	0.3Mcps
11.5V	23.70mV	0.474mA	0.3Mcps
11.6V	29.52mV	0.5904mA	0.4Mcps
11.7V	34.75mV	0.695mA	0.4Mcps
11.8V	48.09mV	0.9618mA	0.4Mcps
11.9V	57.09mV	1.1418mA	0.4Mcps
12V	66.54mV	1.3308mA	0.4Mcps
12.1V	68.90mV	1.378mA	0.4Mcps
12.2V	80.80mV	1.616mA	0.4Mcps
12.3V	90.09mV	1.8018mA	0.4Mcps
12.4V	97.54mV	1.9508mA	0.4Mcps
12.5V	104.0mV	2.08mA	0.4Mcps
12.6V	112.5mV	2.25mA	0.5Mcps
12.7V	117.7mV	2.354mA	0.4Mcps
12.8V	120.5mV	2.41mA	0.4Mcps
12.9V	128.3mV	2.566mA	0.5Mcps
13V	133.8mV	2.676mA	0.5Mcps

Table 10: 2H current mode tests with Rq = 475kΩ

Rq = 953k (Measured breakdown voltage = 11.623V)			
Bias	Pulse Vmax	Inferred current pulse size	DCR*
11.623V	4.79mV	0.0958mA	-
11.7V	7.95mV	0.159mA	-
11.8V	10.99mV	0.2198mA	-
11.9V	16.63mV	0.3326mA	-
12V	24.42mV	0.4884mA	-
12.1V	30.28mV	0.6056mA	-
12.2V	35.46mV	0.7092mA	-
12.3V	42.47mV	0.8494mA	-
12.4V	51.10mV	1.022mA	-
12.5V	56.73mV	1.1346mA	-
12.6V	63.45mV	1.269mA	-
12.7V	68.82mV	1.3764mA	-
12.8V	73.51mV	1.4702mA	-
12.9V	79.82mV	1.5964mA	-
13V	85.88mV	1.7176mA	-

Table 11: 2H current mode tests with Rq = 953kΩ, effective DCR too small to measure

CHAPTER 4: SIGE SPAD SPICE MODEL

4.1 Purpose

Unlike typical circuit designs, quenching circuits possess an added layer of complexity due to the SPAD devices they connect to, the characteristics of which can vary from device to device as was revealed by the batch testing conducted. This means that a quenching circuit that works well with one type of SPAD may not necessarily work for another. For this reason, simulations that reflect the behavior of the SPAD to be used can be a great asset, but the reality is that SPICE models for SPADs are hard to come by and simply do not exist for custom designs such as the ones developed by the lab. While it would theoretically be possible to develop simulation tools using physics modeling, doing so would require detailed, in-depth information on the doping concentrations and layer properties of the chip foundry's processes, all of which is proprietary information and not available for public use.

A half-solution that can be easily employed in these cases is to settle for the use of the linear current pulse sources common in circuit simulators. By adjusting the rise time, fall time, on time, and period of the pulse signal, SPAD avalanche current pulses can be rudimentarily generated. Use of this method, however, severely neglects to account for the reduction of current that takes place when the bias across the SPAD falls below breakdown levels, a phenomenon that is integral to the principle of quenching. This calls for the development of a model that can not only provide current pulses of a specified amplitude, but is also capable of adjusting the state of current flow depending on the voltage bias in real time.

4.2 SPAD Modeling in Literature

Recalling the principles covered in chapter 2, a photodiode can only operate as a SPAD when biased beyond the breakdown voltage, Vbd. The specific voltage amount by which the SPAD bias exceeds breakdown is commonly referred to as the excess voltage, Vex, with larger excess voltages yielding larger avalanche currents. As will be shown by the current mode data collected from SPAD 2H, the relationship between a SPAD's avalanche current and excess voltage is typically linear by nature, or marginally close to linear.

Building on this, in order for a SPICE circuit model to act as a SPAD, it must adhere to a specific set of behaviors. Before being triggered, the circuit must conduct little to no current, but upon triggering (only if biased beyond breakdown) the circuit will need to produce a current linearly related to the excess voltage. If the current produced results in a drop in the bias across the model, the current must decrease accordingly until the bias falls below breakdown, at which point the current must revert to its off-state (if there is no sufficient bias drop, the current should continue). After being quenched, the circuit would then need to exhibit a less-than-instantaneous recharging process that would be controlled by some form of capacitance within the model. Once the bias is brought back above breakdown, the circuit should then be able to be triggered once more. Figure 36 illustrates the described avalanche, quenching, and recharging processes in the form of an IV curve.

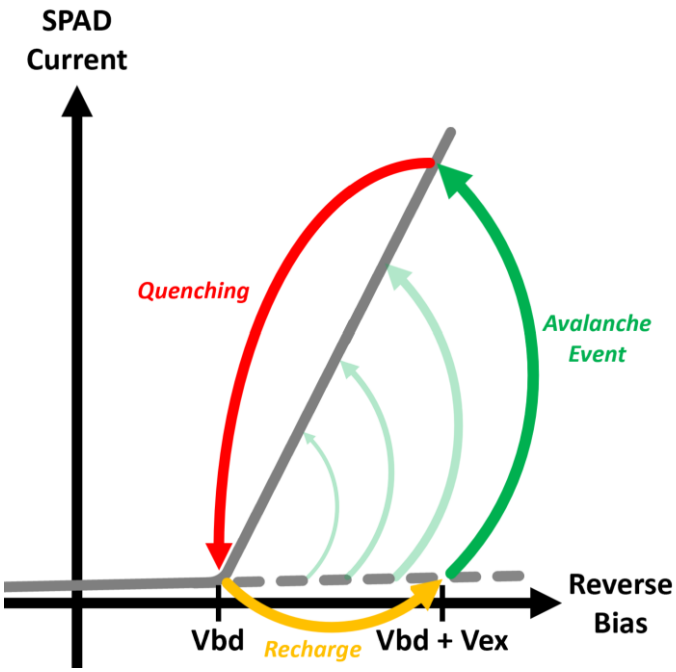


Figure 36: SPAD operation IV curve

In 1965, Roland H. Haitz published a paper that included one of the earliest equivalent circuit models for the avalanche diode that abides by these requirements, which primarily consists of an ideal switch, a voltage source equal to the breakdown voltage, a capacitor acting as the internal capacitance of the diode, Cd, and an internal resistor element, Rd, that determines how much current flows during an avalanche event [18]. The model also accounts for stray capacitance, Cstray, from sources external to the device, although the specific node that Cstray connects to is determined by where it creates the most impact in terms of transient performance. For instance, if the cathode is shorted to the bias voltage while the anode is passively quenched with a resistor, the stray capacitance at the cathode would not matter while it would matter much more at the anode since it affects the recharge time. In such a case, Cstray would connect from the anode to ground. It is worth noting that Cstray may not be constant for every SPAD configuration and will depend on how the chip is interfaced with external electronics. This

equivalent circuit has proven effective and has been used and modified in many forms throughout literature, so it was ultimately chosen to serve as the framework for the model to be developed for this thesis. Since the intended application of the SPADs to be used in the final chip will always have them biased beyond breakdown, the other photodiode regions of operation shown in figure 11 did not need to be simulated, so they are not accounted for in this model.

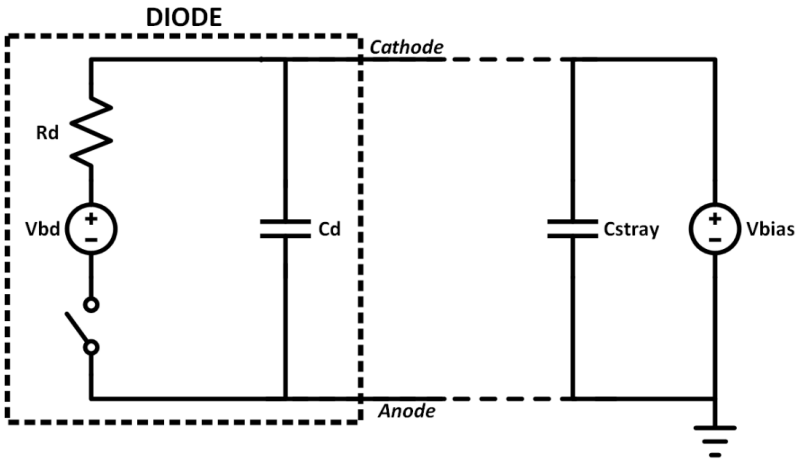


Figure 37: Heitz's equivalent circuit for the SPAD

For normal operation, the basic equivalent circuit assumes that the switch is closed by the arrival of a photon if the diode's voltage exceeds Vbd, and that the switch is opened whenever the diode's voltage falls below Vbd. Furthermore, the resistive quenching element, Rq, is assumed to be significantly larger than the internal resistance Rd. With the circuit's switch opened and at steady state, the voltage across the diode is at Vbias, with no current flowing through the circuit. At this stage, the voltage across Rd is zero. When the switch closes, a voltage equal to $Vex = Vbias - Vbd$ immediately develops across Rd, creating a current that either pulls the anode up to Vex (in an anode quenched SPAD) or pulls the cathode down to Vbd (in a cathode quenched SPAD) before the switch opens again. Since $Rq \gg Rs$, very little of the initial

current travels through Rq, so the current primarily serves to discharge capacitor Cd, which results in the reduction of the bias across the SPAD with a time constant of:

$$\tau_{\text{quench}} = \mathrm{R_d} \cdot \left(\mathrm{C_d} + \mathrm{C_{stray}}\right) \tag{3}$$

When the switch opens due to the bias reduction below Vbd, the SPAD's internal capacitor is then allowed to recharge for subsequent avalanche events. This recharge period has a larger time constant of:

$$\tau_{\text{recharge}} = \mathrm{R_q} \cdot \left(\mathrm{C_d} + \mathrm{C_{stray}}\right) \tag{4}$$

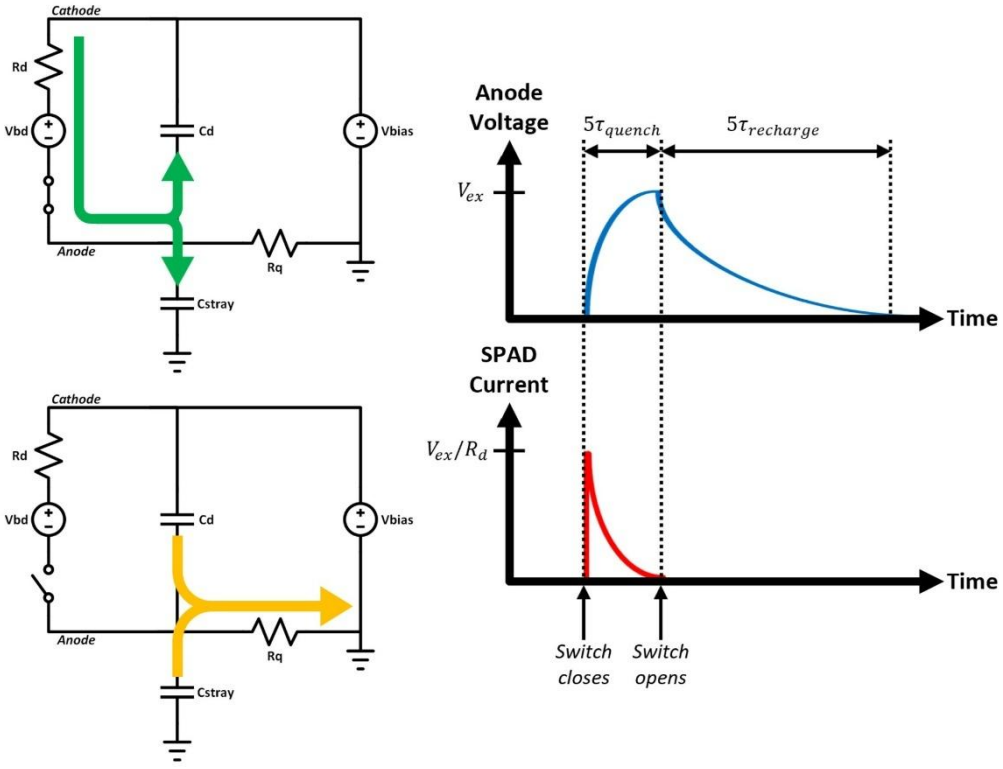


Figure 38: SPAD model operation with anode quenching

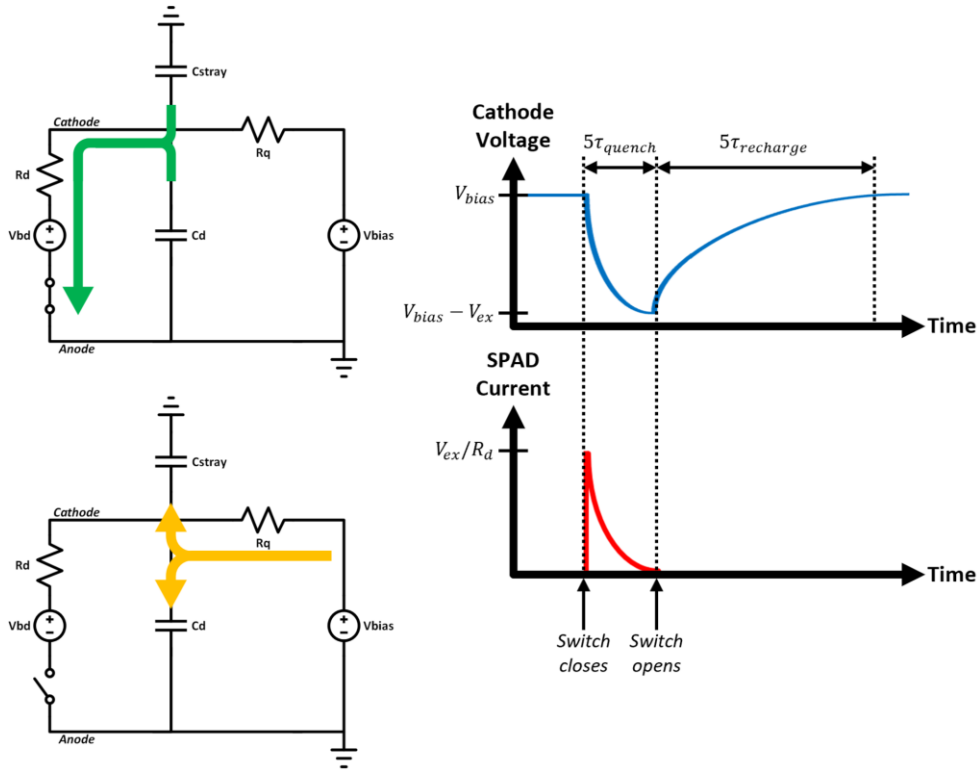


Figure 39: SPAD model operation with cathode quenching

In the context of SPAD testing, $\tau_{recharge}$ was the time constant observed during voltage mode testing, while τ_{quench} was the time constant observed during current mode testing. Following the assumptions of this model, voltage mode pulses should be expected to change with varying Rq values while current mode pulses should stay the same width regardless of the value of Rq. Comparing figure 40 below (current mode waveforms) with figures 32-34 (voltage mode waveforms), this proves to indeed be the case, so it is clear that this model has strong potential to hold somewhat true to actual test results.

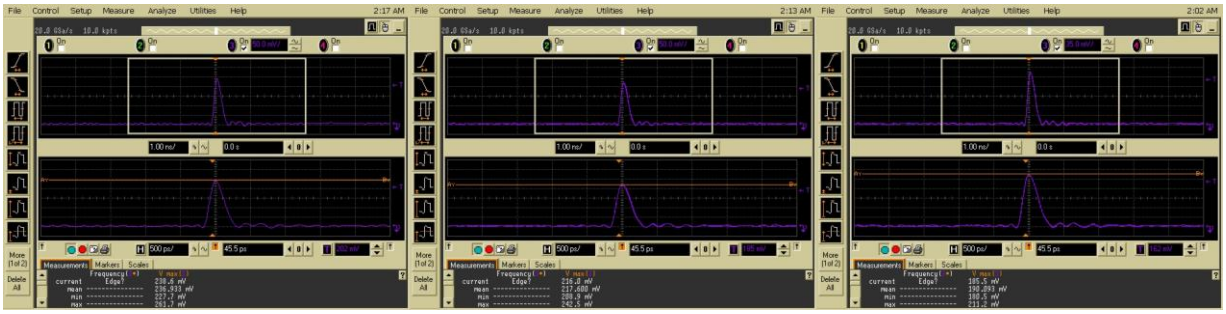


Figure 40: SPAD 2H current mode pulse waveforms using Rq values of (from left to right) 30.1kΩ, 60.4kΩ, and 121kΩ

4.3 Behavioral SPICE Model Development

In order to begin development of the model, the parameters of the breakdown voltage, internal resistance, and internal capacitance of SPAD 2H had to be determined. Using the data from section 3.4, the average was taken of all the breakdown voltages across all 6 current mode test runs to yield an average breakdown voltage of 11.0972V, or approximately 11.1V. In order to estimate the internal resistance Rd, the relationship between the current pulse magnitude and the reverse biasing level needed to be explored further. For the most part, an increase in bias caused an increase in the current, but this increase differed slightly among the various quenching resistances used. To begin to get a better idea of the SPAD's behavior, the current-voltage data from tables 6 through 11 was plotted, and while the linear relationships could clearly be seen, the change in the breakdown voltage for the different values of Rq made it difficult to extract much useful information. To remedy this, the data was normalized so that the current values were plotted corresponding to the excess voltages rather than the actual voltages used, which provided a much clearer picture. The MATLAB script that was created to process the data can be reviewed in Appendix B.

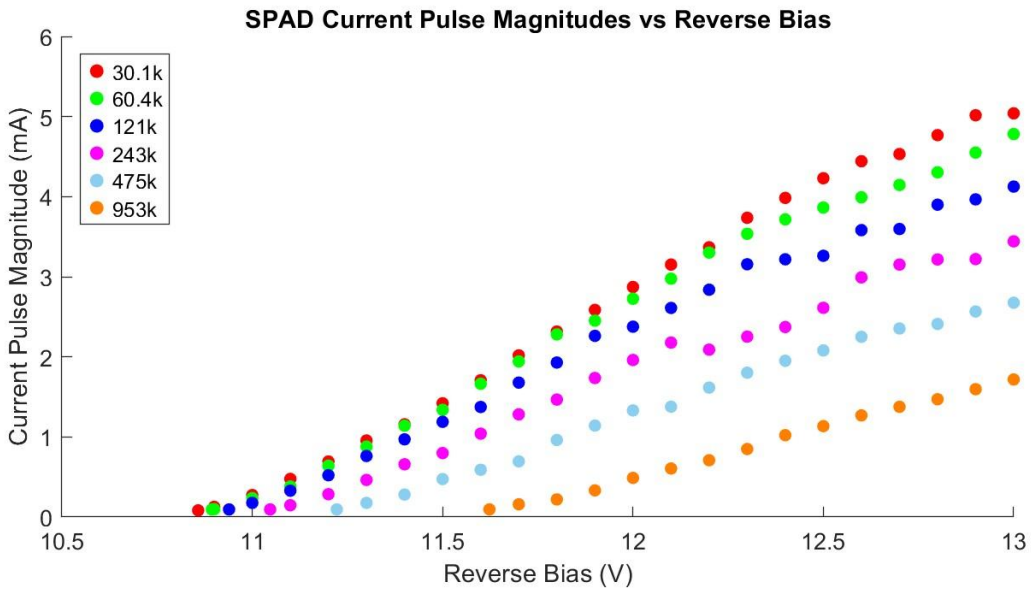


Figure 41: 2H SPAD current pulse magnitudes vs reverse bias

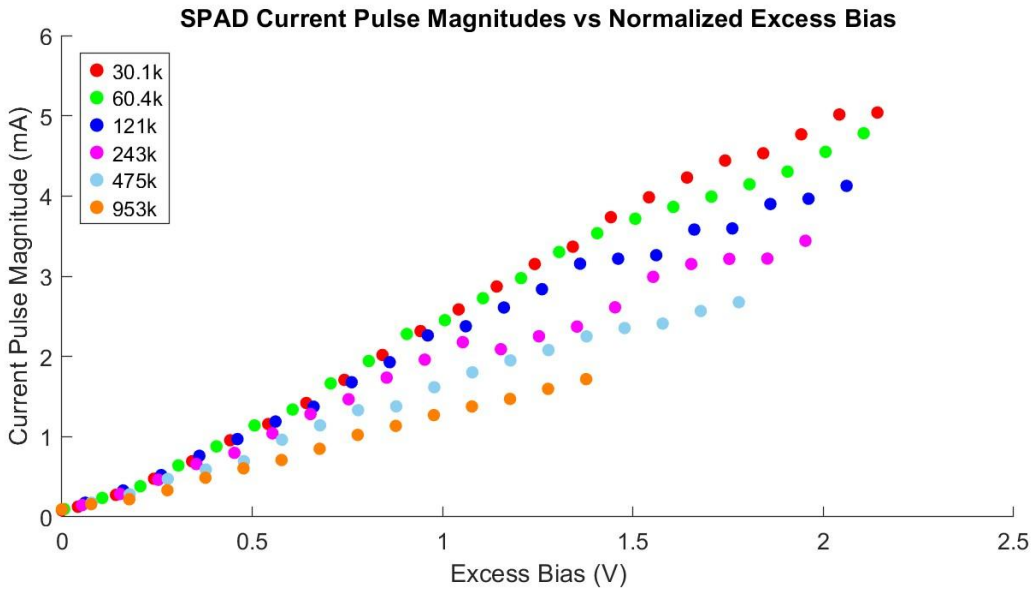


Figure 42: 2H current pulse magnitudes vs normalized excess bias

It was at this point that the normal equation was utilized to determine the line of best fit that would minimize the sum of squared errors, the expression of which takes the form:

$$\theta = (X^T X)^{-1} X^T y \tag{5}$$

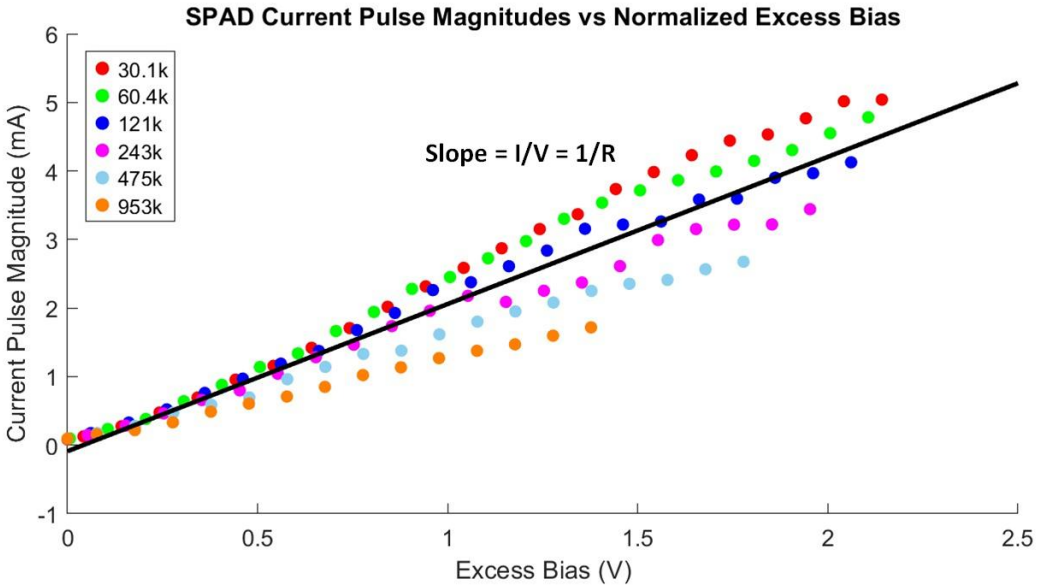


Figure 43: 2H current pulse magnitudes vs normalized excess bias with linear regression utilized

What resulted was a line with a slope equal to I/V = 2.1468mA/V, which in terms of the Haitz model could be used to solve for Rd by taking the reciprocal, yielding an internal resistance of 465.8005Ω, or approximately 466Ω. Having estimated Rd, the calculation of the capacitance was carried out by observing that the settling time of each of the current mode pulses, regardless of bias or quenching resistance, was about $5\tau_{quench} = 500\text{ps}$ if the ripples from what was assumed to be parasitic inductance was ignored (see figure 40). Using equation 3 to solve for the total capacitance acting on the SPAD:

$$\tau_{\text{quench}} = \frac{500\text{ps}}{5} = 100\text{ps} = (466) \cdot \left(C_d + C_{\text{stray}}\right)$$

$$\left(C_d + C_{\text{stray}}\right) = \frac{100 \times 10^{-12}}{466} = 214.592275\text{fF}$$

At this point, it is worth noting that the interface between the chip packaging and the board for the current mode tests was significantly more compact with less room for parasitics compared to that of the voltage mode tests from figure 35. This allowed for much easier estimation of the stray capacitance located at the cathode of the SPAD (the quenching terminal of the device that affects the time constant concerned) through analysis of the board layout. The section of the PCB that connected to the cathode was a single 23.62 mil wide trace over a ground plane (i.e. a microstrip). The distance between the trace on the front of the board and the ground plane on the back of the board was 60 mils, with the board substrate being a standard FR4 material with a dielectric constant of about 4.6 and the copper thickness being 1oz on both sides, as is the standard for OSHPark's 2-layer prototype service. The fall time of the current mode pulse was about 300ps, which corresponds to an effective frequency of $\frac{0.35}{300ps} \approx 1166.667\text{MHz}$. Inputting this data into the Saturn PCB Design Toolkit calculator indicated that such a trace would have roughly 1.4711pF of capacitance per inch.

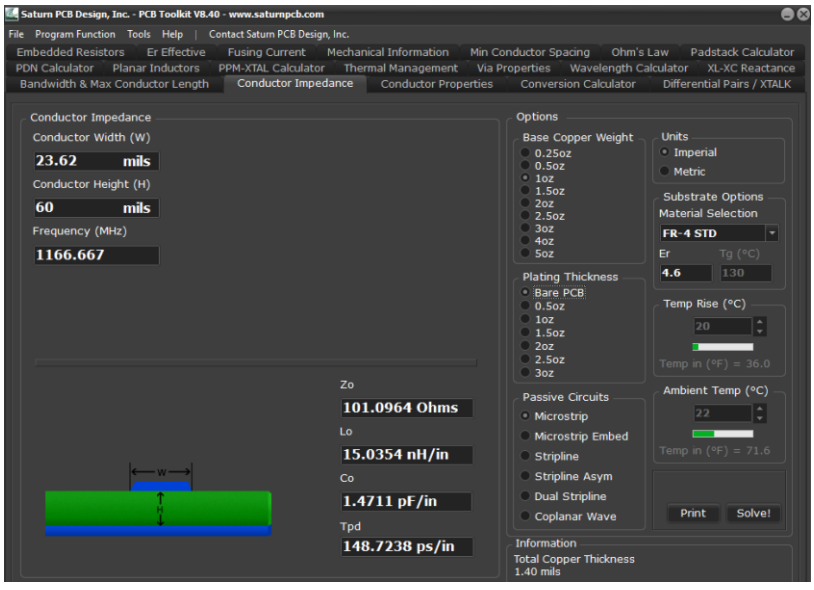


Figure 44: Saturn PCB calculator results

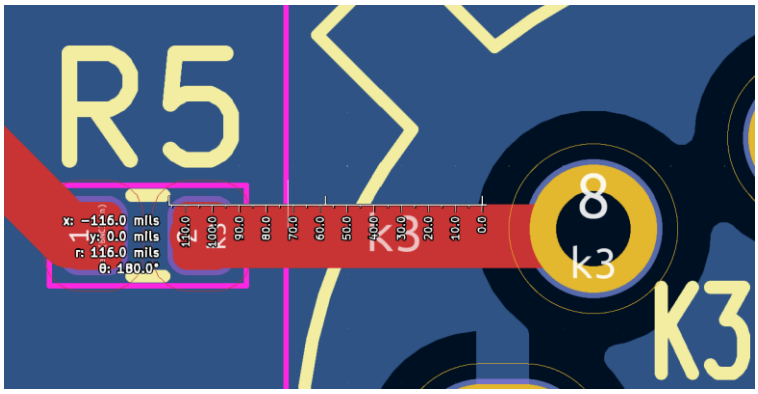


Figure 45: Cathode trace measurement in KiCAD

Measuring the length of the trace that traversed over the ground plane revealed that the trace was about 116 mils long, which corresponded to a stray capacitance of roughly 170.6476fF, meaning that the estimated value of SPAD 2H's internal capacitance, Cd, came out to be $C_d = C_{total} - C_{stray} = 214.592275\text{fF} - 170.6476\text{fF} \approx 44\text{fF}$, which is reasonable for a 5µm-by-5µm SPAD.

Figures 46 and 47 below show the LTspice SiGe SPAD model schematic and symbol that incorporate the calculated parameters. The model operates by closing the main control switch S4 whenever a photon signal triggers the circuit, which passes a high signal to a small capacitor that acts as a sample-and-hold mechanism that keeps the switch on as long as the bias exceeds the breakdown voltage. The bias across the SPAD is tracked via a behavioral voltage source that constantly follows the voltage difference between the cathode and anode pins. The design was optimized to function with photon signals with a 2ps rise and fall time and 10ps pulse width, which allows for very fast operation without inducing discontinuous circuit behavior. However, to operate as intended, the step size of the transient simulation must be limited to 0.5ps to allow the simulator to accurately capture the waveform. Choosing LTspice's alternate solver in the SPICE engine settings also helps to prevent convergence issues.

Whenever the bias falls below breakdown, switch S2 will disconnect the circuit from the 1V voltage source to prevent any other avalanches while switch S3 grounds the sample-and-hold capacitor, turning off the main switch in the process. While the voltage source inside the diode section of the model is declared as 11.09V rather than the 11.1V breakdown voltage, the switches that detect breakdown conditions were modeled with a 100mV hysteresis centered about 11.2V, meaning that the SPAD will still stop conducting when the bias falls below 11.1V. Using 11.09V as the internal breakdown voltage source allows the bias to actually fall low enough to successfully quench, otherwise the model would take a very long time (ideally infinity) to actually reach 11.1V. Regarding the hysteresis, it is a necessary feature that prevents switch S4 from oscillating on and off due to the grounding switch S3 not being on for enough time to effectively ground the sampling capacitor. A current source was also added into the model to simulate leakage currents.

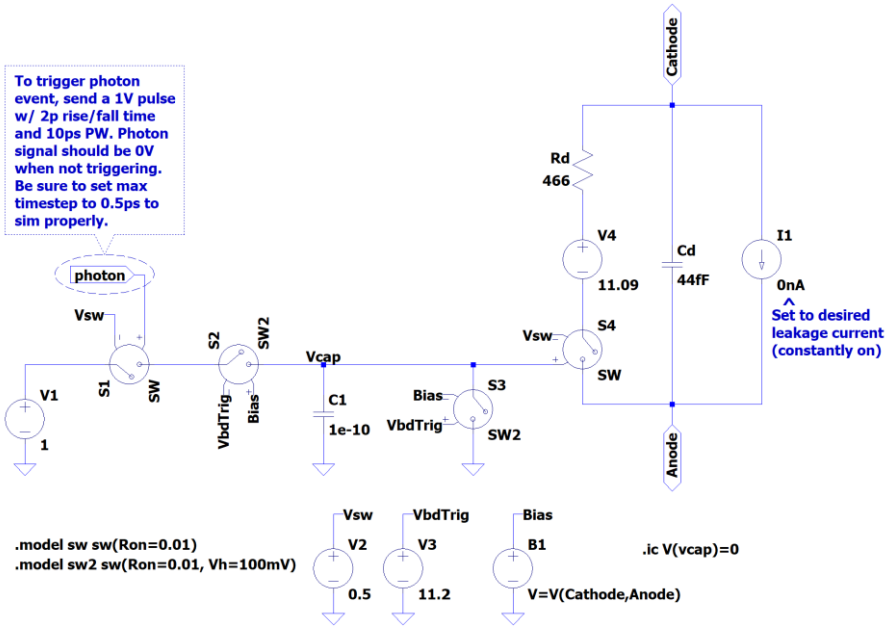


Figure 46: LTspice SiGe SPAD model schematic

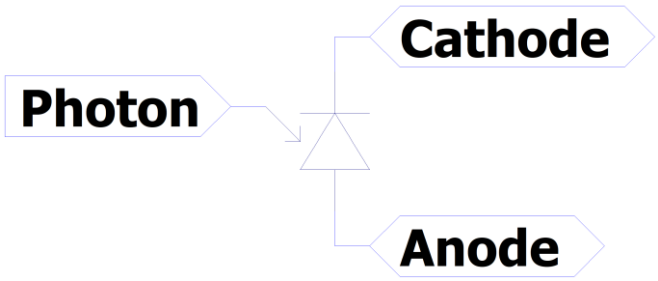


Figure 47: LTspice SiGe SPAD model symbol

4.4 Simulation Results

Assuming a maximum bias level of 13V, the largest current pulse magnitude that the model can provide to discharge Cd is $\frac{13-11.09}{466} \approx 4.1\text{mA}$, but this current immediately falls with the bias drop to converge with the current set by the quenching resistance until the SPAD is completely quenched.

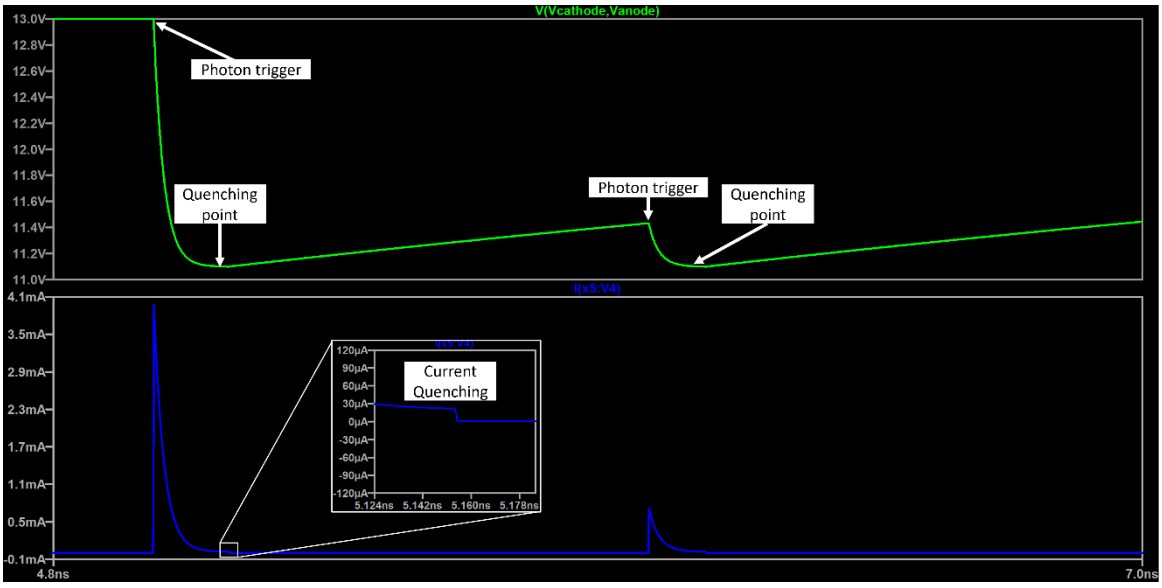


Figure 48: SPAD model simulation showing the reverse bias of the SPAD (green) and the SPAD avalanche current (blue) with two photon trigger events

However, similar to real testing results, there is a minimum quenching resistance below which quenching does not happen reliably in the model and instead results in DC-signal outputs like those seen in figures 29 and 30. The mechanism behind this is more readily understood by graphing the current through the SPAD as a function of the anode voltage (assuming the anode is the quenched terminal) and comparing it with the IV curve of the quenching resistor, which will look similar to figure 36 only that the axis is flipped and shifted. Figure 49 shows an illustration of such a graph.

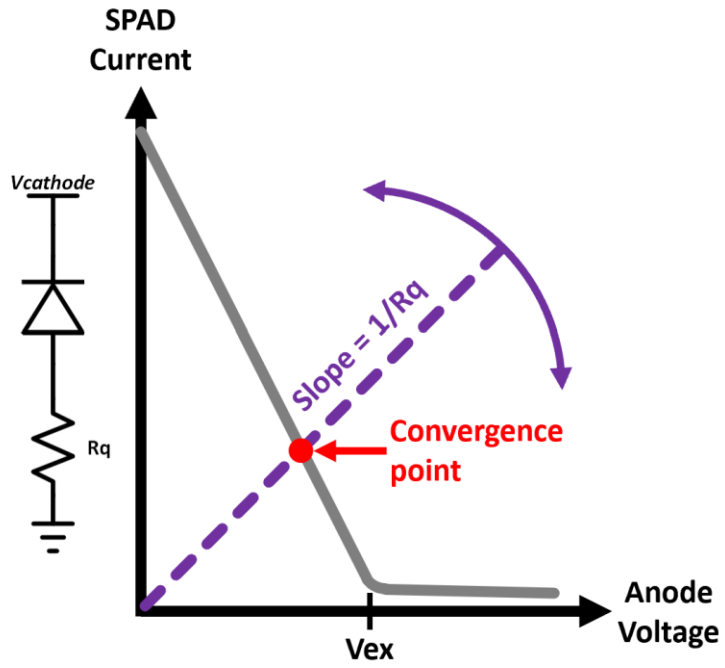


Figure 49: Anode referenced SPAD IV curve with quenching resistor IV curve shown

Intuitively, Ohm's law dictates that the larger Rq becomes, the larger the voltage drop across the resistor becomes for a given current signal, meaning that larger Rq values provide better quenching than smaller values. Mathematically, referring to figure 49, the larger Rq becomes, the shallower the slope of the resistor's IV curve becomes, meaning that the

convergence point where the IV curves of the resistor and SPAD meet has a higher voltage. If the value of Rq is too low, the slope becomes too steep to the point where the convergence point's anode voltage lies below Vex, meaning that the SPAD bias is not able to be reduced below the breakdown voltage, resulting in continuous current. Since the model's anode referenced IV curve can be modeled as a linear function, $I(V_{anode})$, using its internal 11.09V source and 466Ω resistance, the minimum Rq value needed for quenching can be calculated as the resistance that would provide a 1.9V (the maximum excess voltage, $V_{ex,max} = V_{cathode,max} - V_{bd} = 13V - 11.1V$) voltage drop while converging with the IV curve. Using the maximum excess voltage for this calculation ensures that reliable quenching takes place regardless of the bias level used. Simulation of the model showed that the derivation below, which estimated a minimum Rq of 89kΩ, holds true. While this behavior does seem to contradict earlier testing that showed that quenching can be accomplished with resistances as low as 30kΩ, this only means that the SPAD's real IV characteristic may be slightly curved near its quenching point rather than a straight line, allowing for the 30kΩ resistor's IV curve to converge with the SPAD beyond the excess voltage, but for general purpose simulation, the model is still useful.

$$I(V_{anode}) = \frac{1}{R_d}\left(V_{cathode,max} - V_{anode} - V_{bd,model}\right) = \frac{1}{466}(13 - V_{anode} - 11.09)$$

$$\text{Let } V_{anode} = 1.9V$$

$$I(1.9) = \frac{1}{466}(13 - 1.9 - 11.09) = 21.459uA$$

$$\frac{V_{anode}}{R_{q,min}} = \frac{1.9}{R_{q,min}} = 21.459uA \rightarrow R_{q,min} = 88.540k\Omega \approx 89k\Omega$$

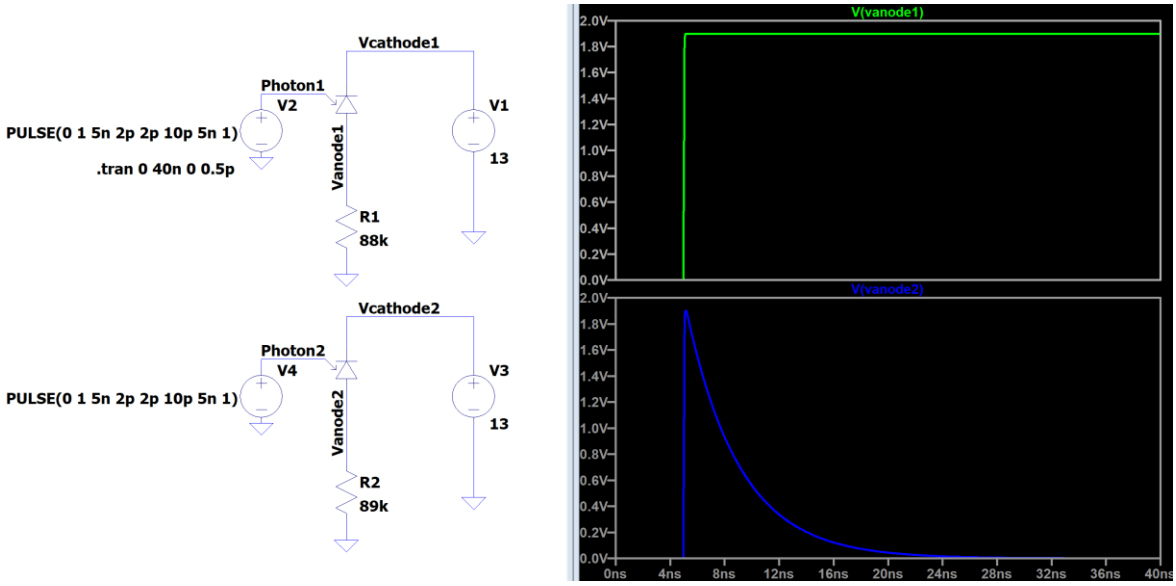


Figure 50: SPAD model simulation comparing the anode response to using an Rq of 88kΩ (green) vs 89kΩ (blue)

In addition to successfully modeling low quenching resistance behavior, the SPICE model also captures how the SPAD's pulse size increases with the applied reverse bias. Figure 52 shows how the model responds to photon signals using both anode and cathode quenching as the bias is sweeped from below breakdown all the way up to 13V.

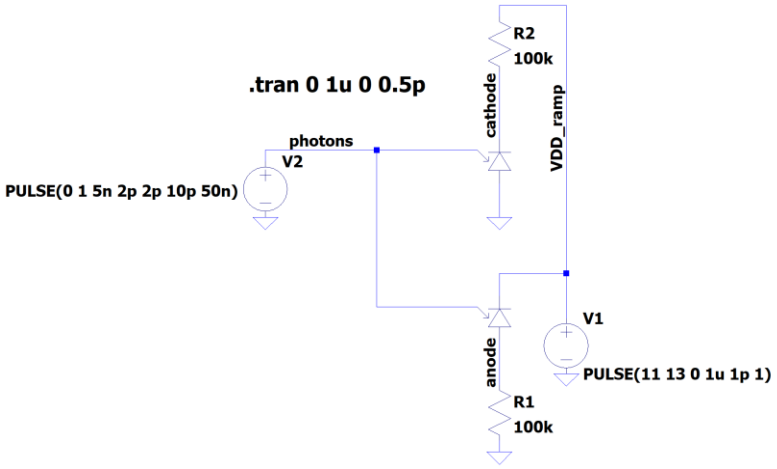


Figure 51: Schematic for testing anode and cathode quenching using a bias sweep

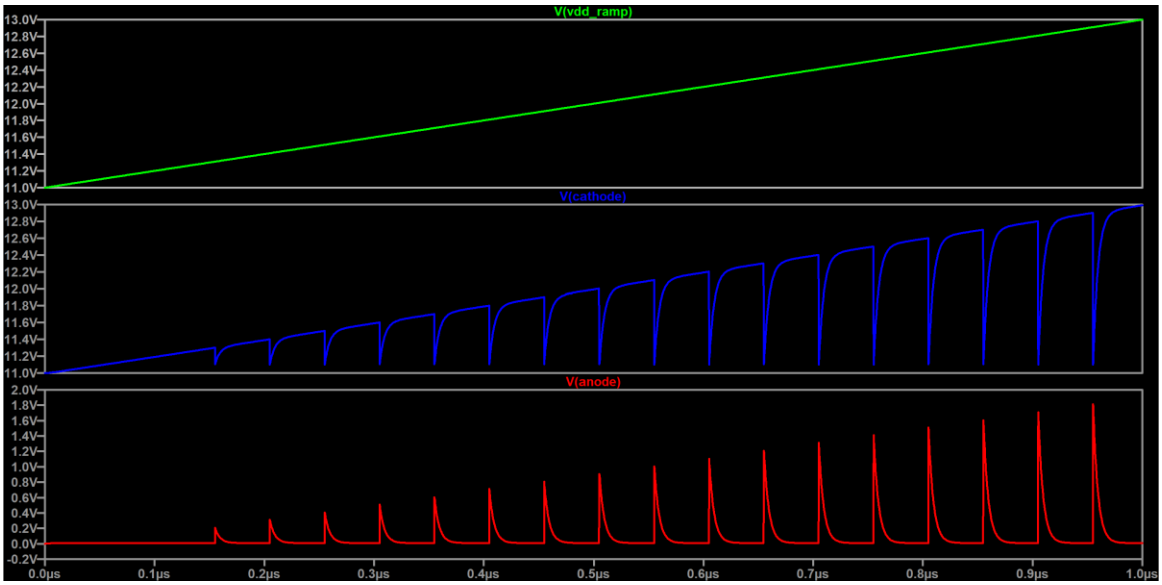


Figure 52: Simulation results of schematic from figure 51 showing bias ramp (green), cathode pulses (blue), and anode pulses (red)

The recharge time of the model also scales with the quenching resistance as expected, following the formula $5 \cdot (R_q) \cdot (44\text{fF})$ while the quenching time remains constant at $5 \cdot (466) \cdot (44\text{fF}) \approx 102\text{ps}$.

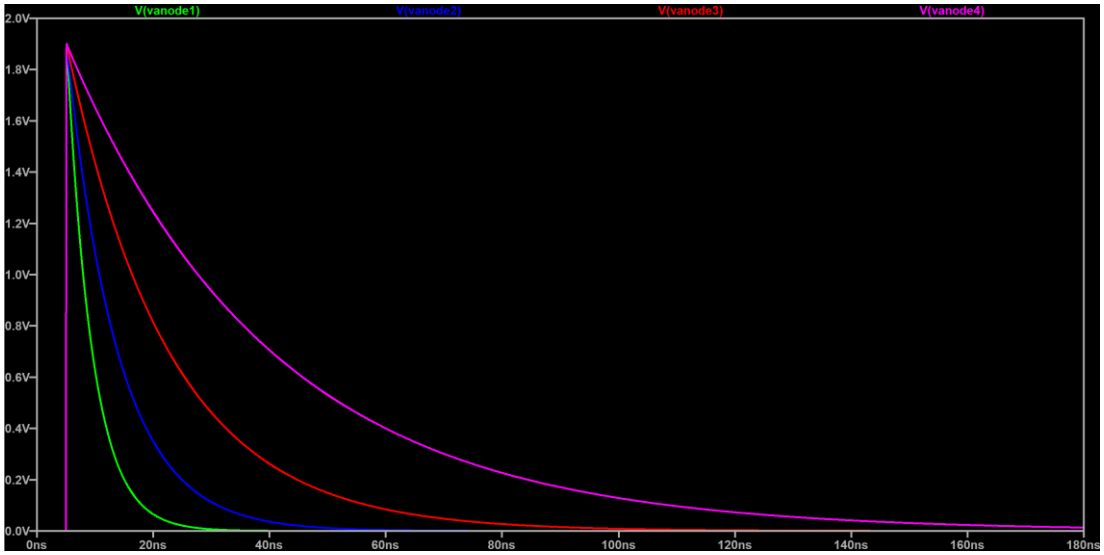


Figure 53: Simulation showing recharge times using Rq values of 100kΩ (green), 200kΩ (blue), 400kΩ (red), and 800kΩ (pink)

4.5 Experimental Behavioral SPICE Model (Not Used)

In the early stages of this project, prior to conducting the extensive current mode testing from section 3.4, a separate attempt to model SPAD 2H in LTspice was made, only that the focus was to get the output to appear as close as possible to the waveform seen in figure 196 from batch testing, which was a 140mV pulse across the 50Ω resistor (i.e. a 2.8mA pulse) that had a pulse width of roughly 170ps with the SPAD biased at 13.5V and cathode-quenched with 976kΩ. While the model covered in the previous section does a good job at modeling the SPAD's general behavior, the waveforms do not appear exactly as they do on the oscilloscope due to factors unable to be accounted for in the Haitz model. The rise time of the current, for instance, is nearly instantaneous in the Haitz model, but in reality, there is a slight delay before reaching the peak current.

Despite the improved accuracy of the pulse shapes provided by this alternative model, the internal capacitance is not very accurate and attempted to implement the two different time constants, τ_{quench} and τ_{recharge}, by using two different capacitors, one on the anode and one on the cathode, with the bigger capacitor needing to be placed on the node being quenched (instead of relying on a single capacitor and two different resistances Rd and Rq, which is more realistic). Since the goal was to match a current mode test result, the larger capacitor was placed on the cathode in this model (meaning that anode quenching is not accurately modeled, only cathode quenching). Another aspect that this model does not capture well is the minimum quenching resistance limit, meaning that in the case where no quenching resistance is used, it will still generate a finite current pulse instead of a steady current. At the time of this model's development, the stochastic nature of the SPAD's avalanching behavior was overemphasized, and it was assumed that all avalanches could be quenched regardless of the biasing (which can be

true in some device structures under the right conditions, but not in this case). As a result, every single photon triggered output generated by this model has a FWHM pulse width of 170ps unless quenched. Regardless, this section discusses this model for the purpose of documenting the potential for other waveform accurate models that may be developed in the future.

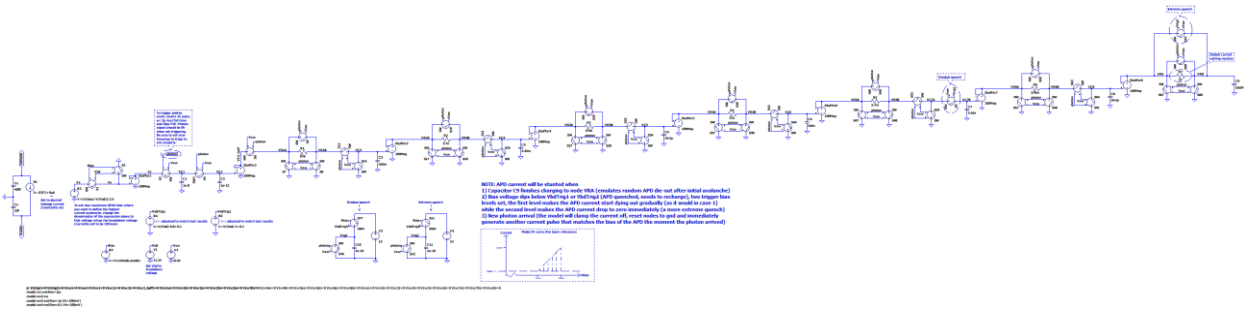


Figure 54: Experimental SiGe SPAD SPICE model schematic

The schematic of this model consists of ideal circuitry that samples the bias at the time of triggering and generates a current pulse corresponding to that bias, with switches placed to clamp and reset the current under the right conditions. There are three main sections of the circuit: (1) Static/dynamic sources that set the characteristics of the SPAD, (2) a bias sampler that samples a normalized version of the excess voltage across the model when triggered, and (3) a pulse generator made from an RC transmission line that emulates the smooth pulse shape observed from the current mode test from figure 196. Section 3 includes switches in charge of clamping and resetting the circuit when the SPAD is quenched or retriggered. Throughout the model, ideal buffers are used to isolate different sections of the circuit to avoid sensitivity to parasitic currents caused by the internal resistances of the ideal switch models. Similar to the previous model, in order to work, the user must use LTspice's alternate solver engine, a 0.5ps step size, and 10ps-wide photon signals with 2ps rise and fall times.

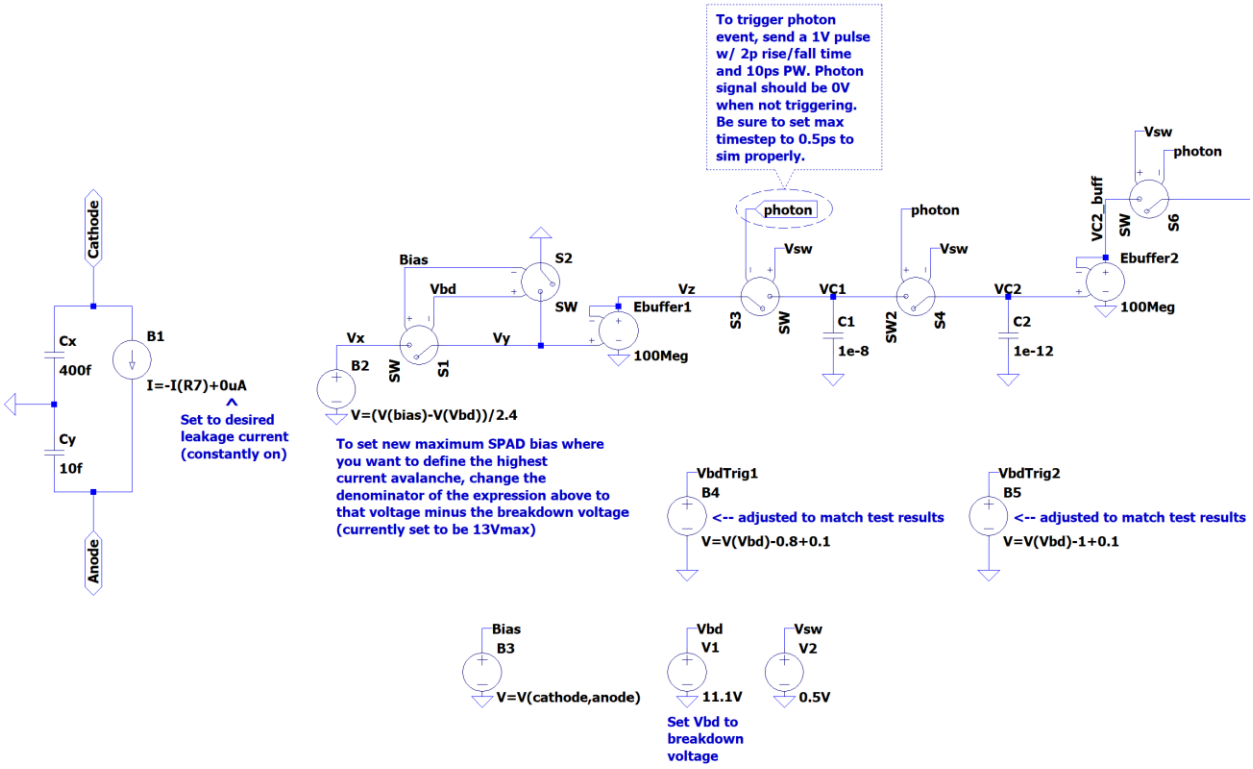


Figure 55: Sections 1 and 2 of the circuit

The operation of the model begins by using a photon-signal-triggered sample-and-hold circuit comprised of switches S3 and S4 and capacitors C1 and C2 (see figure 55) to sample the excess bias across the SPAD, which is normalized to a voltage between 0V and 1V and then passed on to the pulse generating section by switch S6 after the trigger signal returns to a low state. Normalization of the excess bias is done using the formula:

$$V_{norm} = \frac{V_{bias} - V_{bd}}{V_{ex,max}}$$

If the bias across the SPAD was 13.5V for example, with a breakdown voltage of 11.1V and a maximum excess voltage of 2.4V, the normalized voltage that would be sampled would be 1V (if $V_{bias} = 12.3V$ then V_{norm} becomes 0.5V, and if $V_{bias} = 11.1V$ then V_{norm} becomes 0V, etc.). The behavioral voltage source that generates this normalized voltage is source B2, and it is assumed that its output will never exceed 1V. The bias across the SPAD and its breakdown voltage are defined by voltage nets Bias (source B3) and Vbd (source V1), respectively. The voltages VbdTrig1 (source B4) and VbdTrig2 (source B5) exist to set different quenching points whenever the model is in the avalanche state. The bias falling below VbdTrig1 initiates a gradual quench (current avalanche stops increasing and gradually settles back to zero) while the bias falling below VbdTrig2 (lower than VbdTrig1) initiates an extreme quench (current clamps to zero instantly). Setting two quenching points was done to allow for the model to retain the smooth pulse shape on its output without sacrificing the ability to effectively quench under the right conditions. The mechanisms behind the gradual quench and extreme quench will be covered shortly.

Whenever the bias falls below the breakdown voltage, switches S1 and S2 will isolate and ground the node leading to the sample-and-hold's input, ensuring that the sampled voltage stays at 0V until the bias rises above breakdown again. The avalanche current that is generated as a result of the sampled voltage is output by behavioral current source B1, which copies the current passing through the last resistor in the pulse generator chain, resistor R7. An extra DC current term can be added to this source to mimic leakage current in the SPAD. The two capacitors connected in parallel to the source, Cx and Cy, were determined through simulation trial and error until an output matching that of the current mode test was observed.

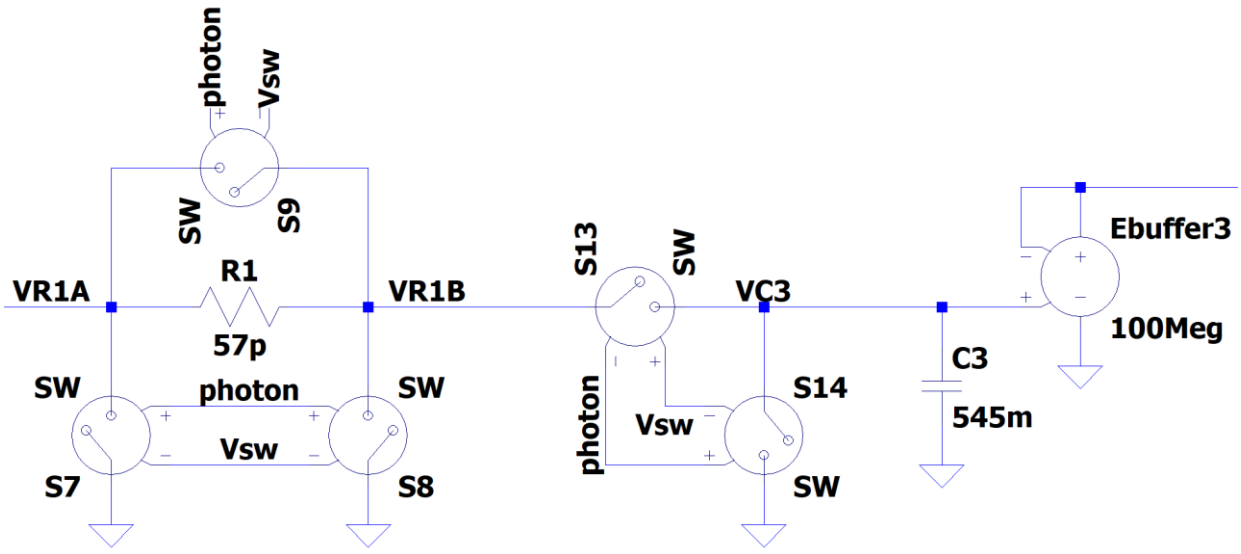


Figure 56: A single typical RC stage of section 3 of the model

After the normalized voltage has been sampled, it is passed on to an RC transmission line made up of 7 different RC stages. Each subsequent stage increases the resistance by a factor of 100 and decreases the capacitance by a factor of 100, with the RC time constant remaining the same for each stage (31.065ps). The specific values used were also determined by trial and error to match the pulse shape from figure 196. The larger the sampled voltage is, the more current is able to travel through the transmission line, which results in a larger avalanche current that is shaped by the voltage drop across the current setting resistor R7, which is located in the final RC stage.

Each RC stage is connected to switches that short and ground both terminals of each resistor while also isolating and grounding each capacitor whenever a new photon signal is input to the model. This serves to reset the circuit as fast as possible in order to prepare section 3 to generate a new current pulse corresponding to the new sampled voltage. The fifth and seventh stages of section 3 contain extra switches that are in charge of performing the actual quenching

of the SPAD, and are activated by trigger signals that are set by voltages VbdTrig1 and VbdTrig2 and cleared by the arrival of a new photon-signal rising edge.

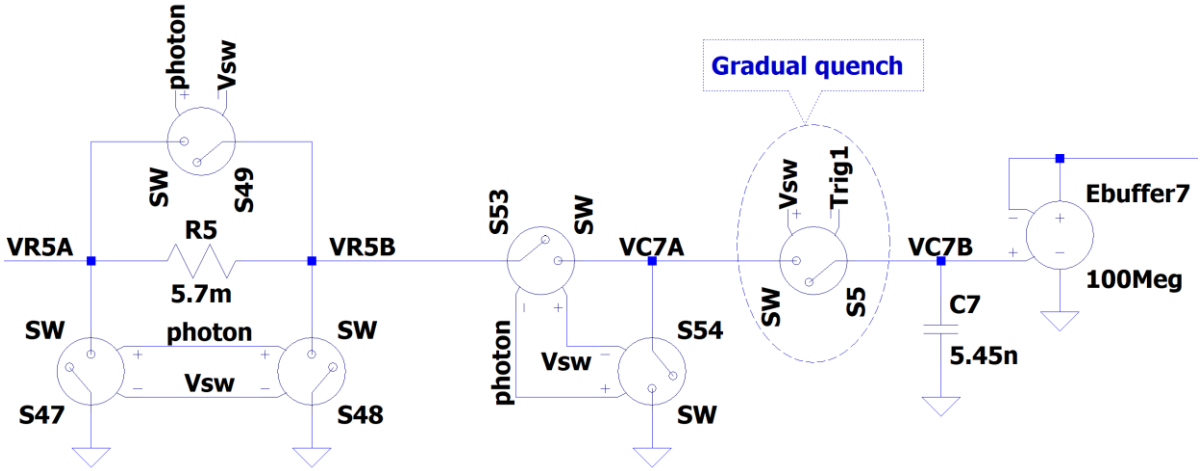


Figure 57: The fifth RC stage of section 3 of the circuit, which contains the gradual quenching switch

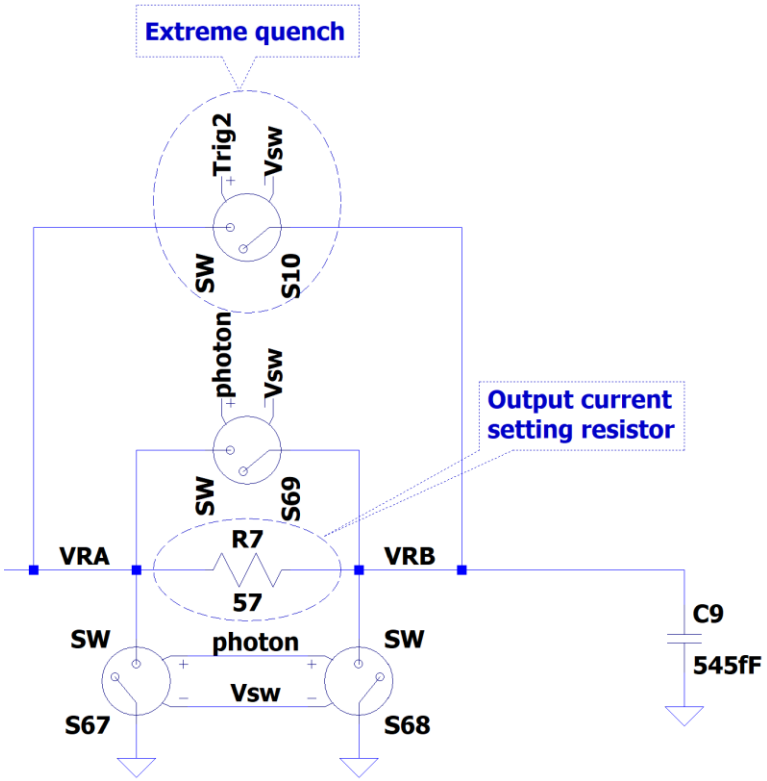


Figure 58: The final seventh RC stage of section 3 of the circuit, which contains the extreme quenching switch

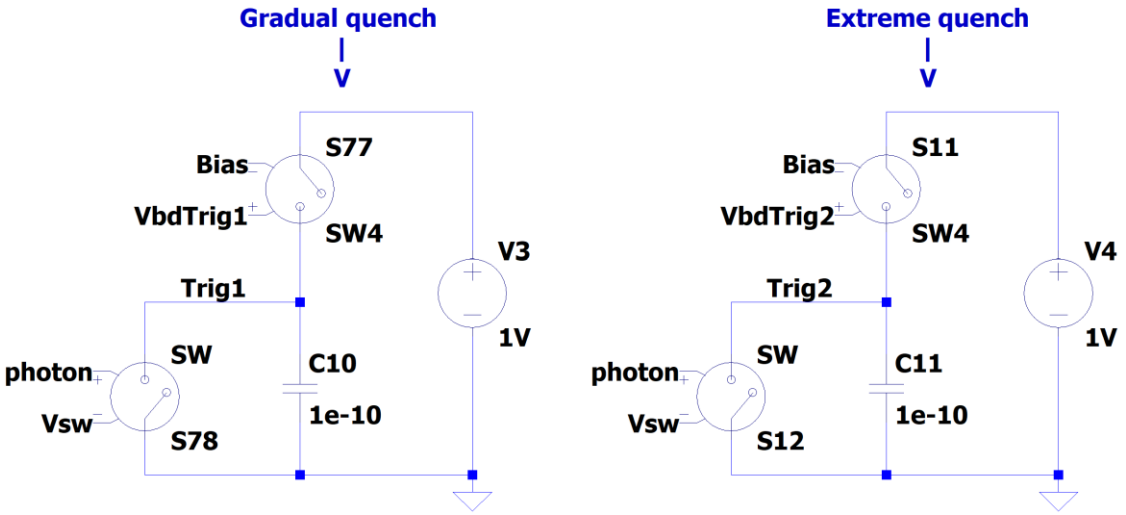


Figure 59: Gradual and extreme quench control circuitry

The gradual quench works by stopping the flow of current through the transmission line two stages ahead of the current setting resistor, which allows for the currents and voltages in the last two stages to reach steady state on their own, gradually reducing the avalanche current to zero. The extreme quench, on the other hand, simply shorts the terminals of the current setting resistor to stop the avalanche current entirely in an instant. Figures 61-63 show simulations that illustrate the difference between a nominal pulse, a gradually quenched pulse, and an extremely quenched pulse. For each of the figures, the top waveform window shows all of the RC voltage nodes throughout stage 3, the center window shows only the voltages on both sides of the current setting resistor R7, while the bottom window shows the resulting voltage pulse caused by the avalanche current (which follows the voltages in the middle window). Note that the symbol for this experimental model is identical to that shown in figure 47.

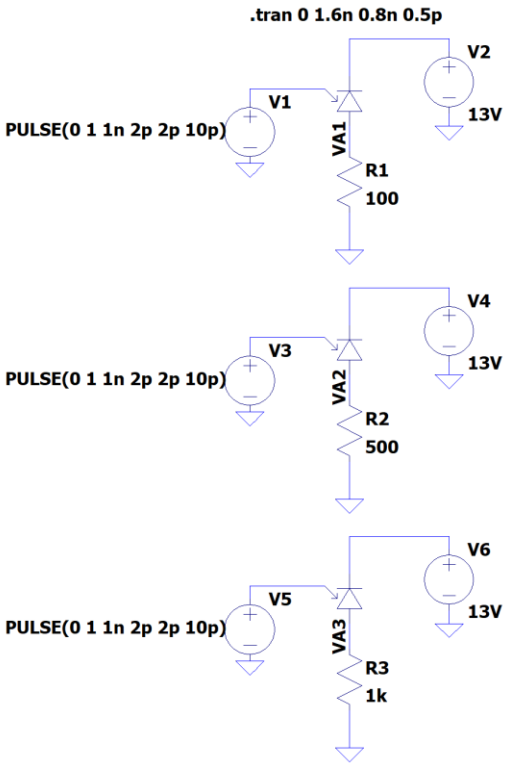


Figure 60: Circuits used to simulate a nominal pulse (top), gradually quenched pulse (center), and extremely quenched pulse (bottom)

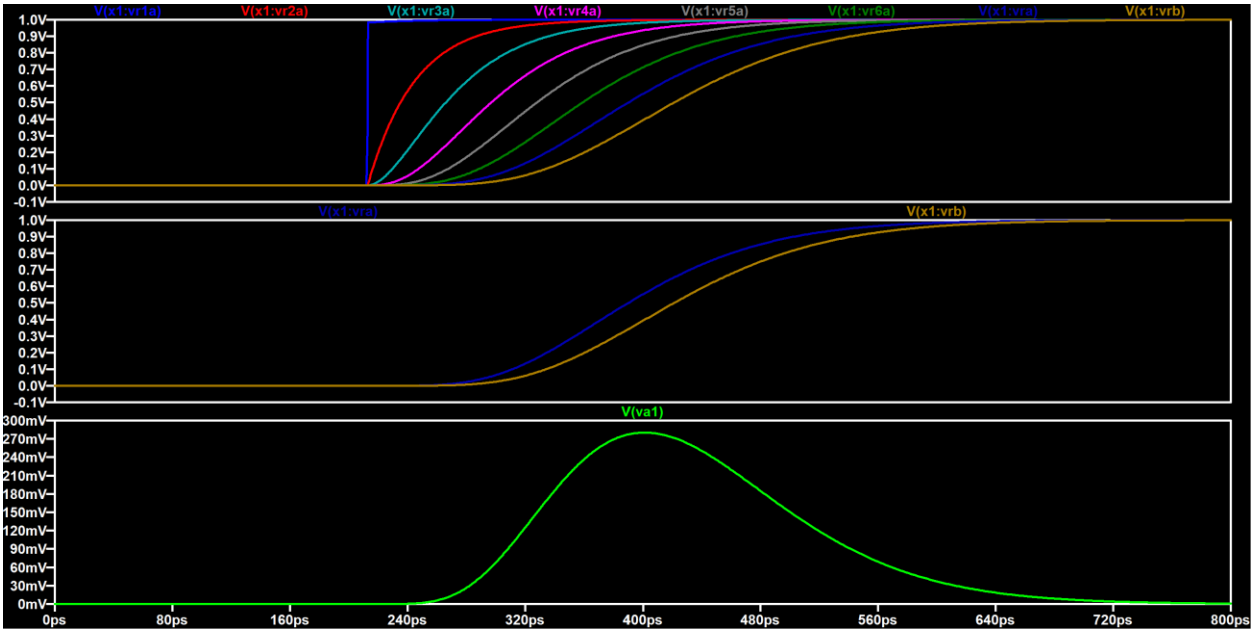


Figure 61: Nominal pulse model behavior

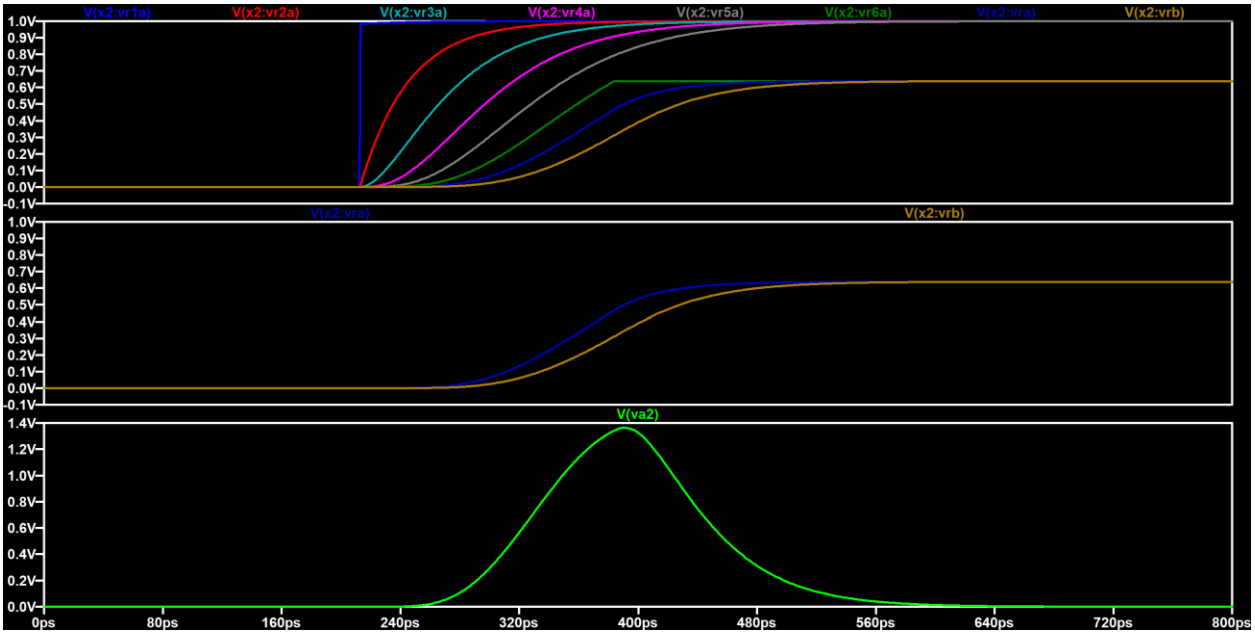


Figure 62: Gradually quenched pulse model behavior

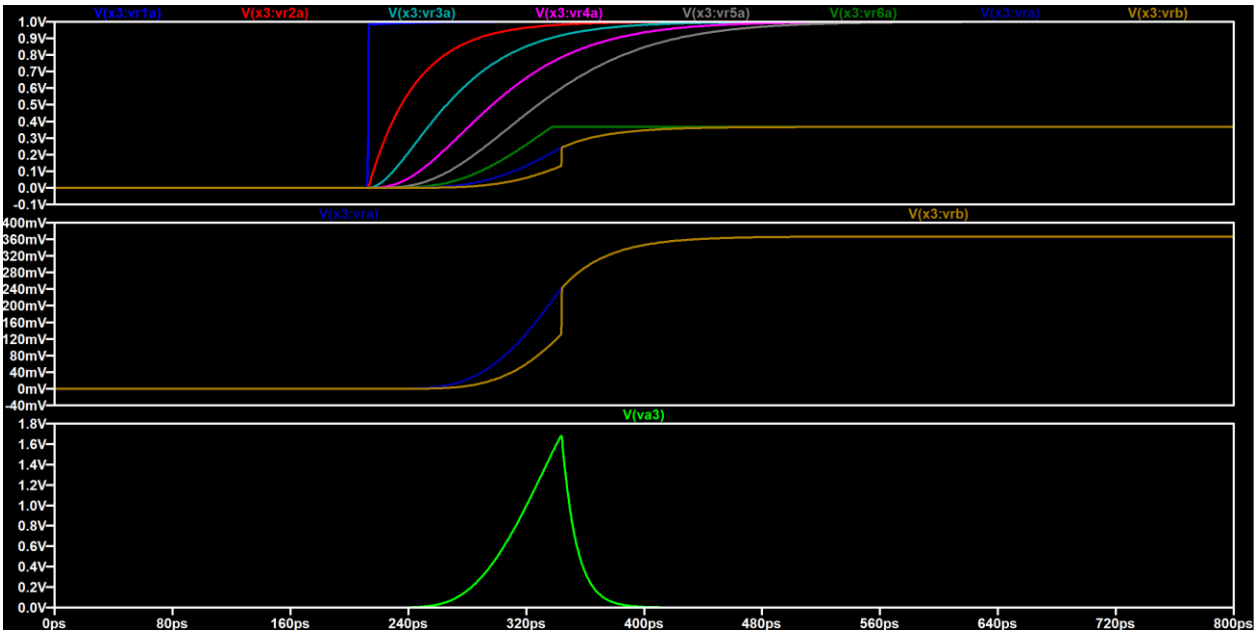


Figure 63: Extremely quenched pulse model behavior

Most importantly, when simulating the conditions of the referenced current mode test, the anode voltage waveform seemed accurate to the measured result from figure 196.

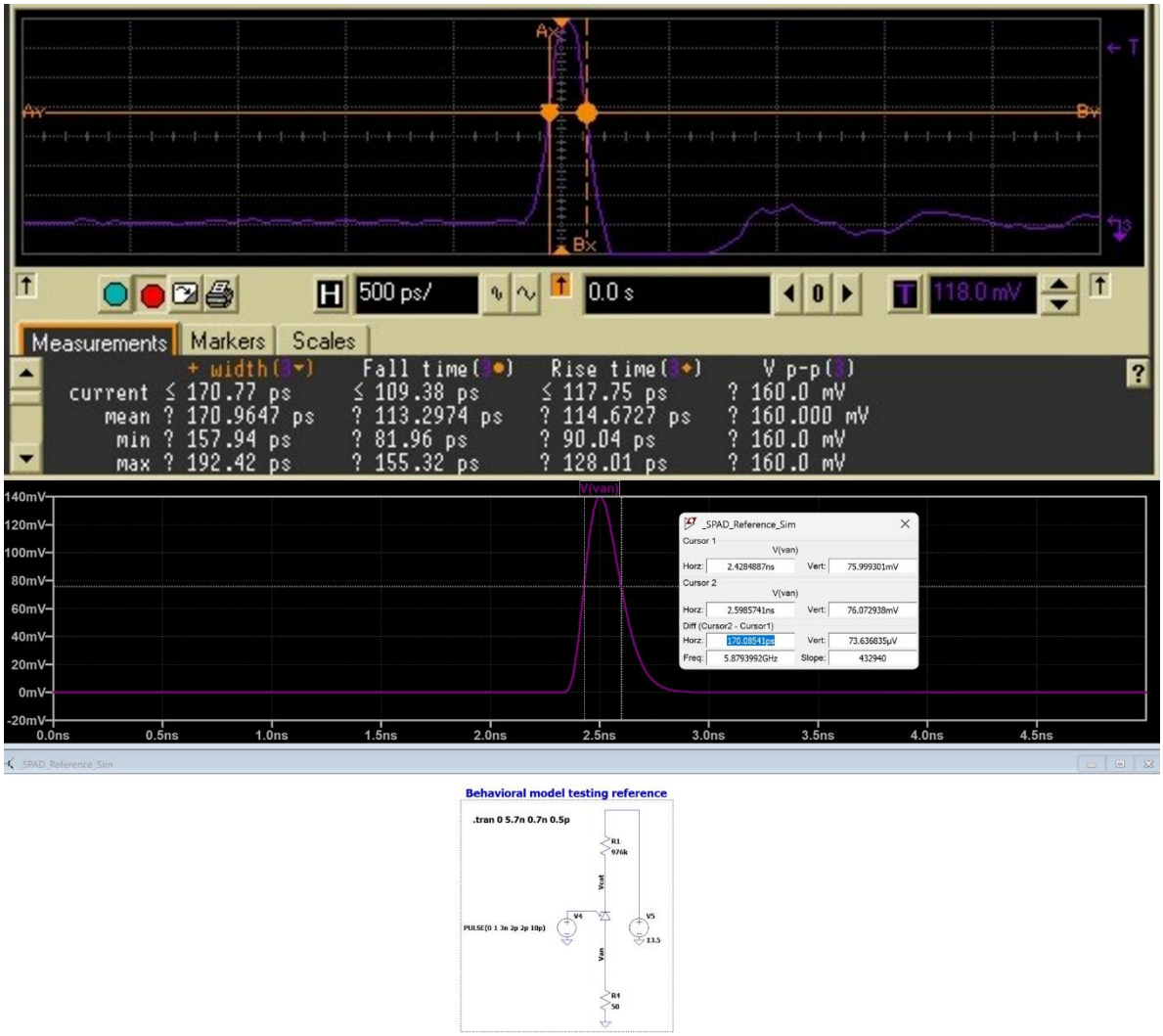


Figure 64: Comparison between referenced current mode test waveform and experimental model simulation

Regardless of this result, because of the problems discussed regarding the model's internal capacitance implementation and quenching behavior, this experimental model was not used. In the future, an effort may be made to combine both the operational accuracy of the Haitz model with the waveform accuracy of the experimental model, but for the purposes of integrated circuit design, the Haitz model has proven sufficient and was developed using a much more comprehensive dataset regarding the SPAD's behavior.

CHAPTER 5: EXISTING 350NM ACTIVE AND PASSIVE QUENCHING DESIGNS

A chip intended for photon counting, PDC1 (Photon Detection Circuits 1), was designed by former members of the lab as part of a previous research initiative and contained both active and passive quenching circuits. Although only the passive quenching operated as intended, the lessons learned from these designs greatly informed the development of the new quenching circuits and will be the focus of this chapter. This specific chip was manufactured in the same S35 process mentioned in section 3.2.

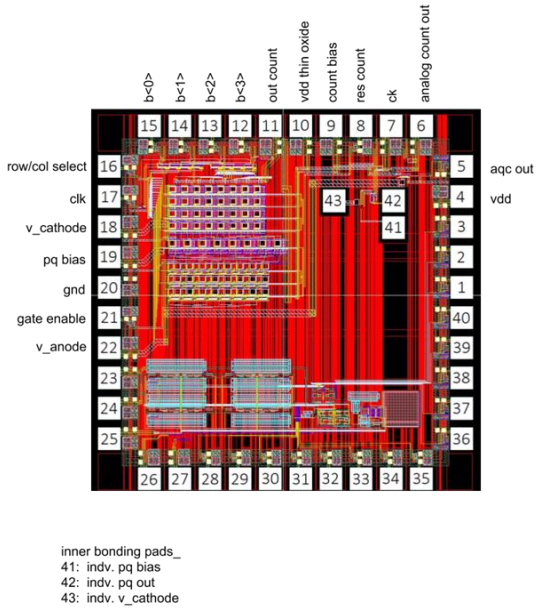


Figure 65: Original chip containing photon counting circuits

5.1 Original Active Quenching Design

The active quenching method that was used in PDC1 was based off of a design created by Eisele et al. [19] that uses a positive-feedback monostable circuit to momentarily reduce the bias across the SPAD and provide an output pulse that can be passed onto external counting circuitry.

This is accomplished through a set of transistors connected to the cathode of the diode that are controlled by a series of inverters and a NAND gate as shown in figure 66.

Since the voltage rail in the S35 process was limited to 5V maximum, a large negative voltage was required on the anode in order to bias the device beyond breakdown (as would be the case for most standard CMOS/BiCMOS processes). Application of large negative voltages relative to the P-substrate (typically tied to ground) on integrated circuits can pose a high risk of conducting leakage currents through the bulk silicon, which can cause malfunction of devices on other areas of the chip. To attempt to remedy this, deep trench isolation (DTI) was implemented to better isolate the SPAD from the substrate. In order for the design to function, the negative bias, -Vbias, must be low enough in magnitude so that it alone does not exceed the breakdown voltage, Vbd, but still high enough so that $VDD + Vbias > Vbd$. Furthermore, the pull up transistor, MU, must be made to be stronger than the pull-down transistor, MD, to successfully reset the SPAD. Similarly, M2 must be sized so that it is stronger than M1 to be able to return the circuit to steady state.

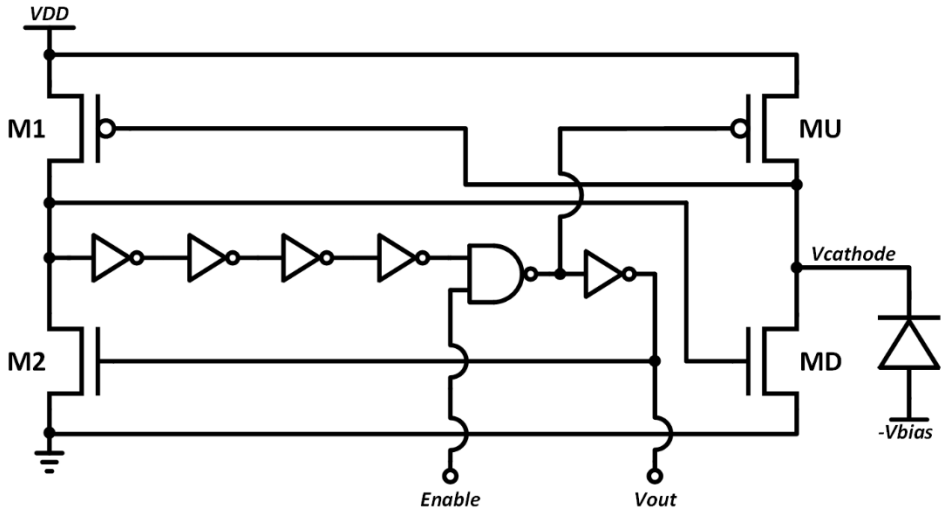


Figure 66: Active quenching circuit from PDC1

At steady state (i.e. before the avalanche) transistors M1, M2, MU and MD are all off in the circuit, with the cathode voltage, Vcathode, at VDD and the output, Vout, at a logic low level. Upon detection of a photon, Vcathode will begin to fall due to the avalanche current. When Vcathode falls below the PMOS threshold voltage, M1 activates and pulls the voltage on the gate of MD high, which quickly forces Vcathode down to ground to perform the quench. After a short delay, the rising edge on the input to the first inverter propagates through the inverter chain and (assuming that the enable signal is high) flips the NAND output low, activating MU and pulling Vcathode back up to VDD, resetting the SPAD and turning off M1. One inverter-delay after the NAND output changes, Vout goes high and turns on M2, which results in a low input to the inverter chain (turning MD off) that propagates through the chain and turns MU off and brings Vout low (turns off M2 last). At this point, the quenching process has been completed and the circuit is once again in steady state and ready for subsequent photon detections. The photon-signaling output in this circuit configuration is a rising-edge pulse with a width dependent on the amount of time it takes M2 to pull its drain node voltage low and for that low signal to propagate through the inverter/NAND section. Strategic use of the enable signal would allow for this design to be useful in time-gated photon counting.

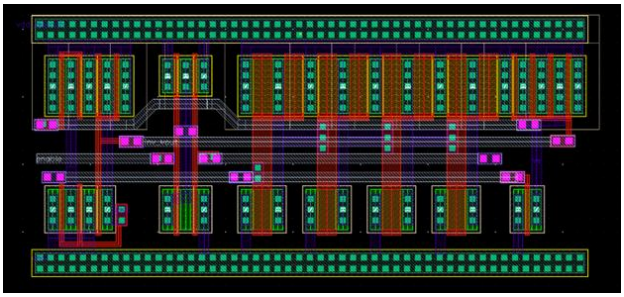


Figure 67: Original active quenching circuit layout by Gonzalo Arteaga

5.2 Original Passive Quenching Design

The original passive quenching method borrows from a design developed by Pancheri et al. [20] and took advantage of a pair of thick oxide transistors with higher operating voltages available in the process to provide front-end protection of the SPAD electronics. One thick oxide transistor acted as the resistive load responsible for quenching/recharging the SPAD while the other acted as a clamping device, passing the resulting SPAD pulse to the rest of the circuit. This clamping approach ensured that no pulse larger than $\mathrm{VDD}_{\mathrm{ThickOxide}} - \mathrm{V}_{\mathrm{THN\_ThickOxide}}$ reached the remaining devices.

The pulse-shaping circuitry consisted of a monostable gating circuit comprised of an inverter and a three-input NAND gate, both designed with NMOS devices only, with a capacitor connected between the two. The benefit to avoiding PMOS devices in SPAD pixel circuitry is the reduction of transistor sizing (fill factor increases) but comes at the cost of lower voltage driving strength for instances where the voltage must be pulled high. In this case, the inverter was implemented by using an active load (a long-L NMOS) connected to the drain of the driving NMOS while the three-input NAND gate was implemented with an active load connected to two NMOS devices in series, with two inputs feeding into their gates and the third input connected to the source of the bottom-most NMOS. This third input, referred to as WINi, was the inverted form of the enable signal, WIN, that could be used to open the detection time window for time-gated photon counting. One user-controlled DC voltage source, Vbq, was needed for this design to set the on-resistance of the quenching transistor. The voltage that resulted in the largest pulse sizes without excessive recharge dead times was determined experimentally. Unlike the active circuit, the higher voltage bias was applied to the cathode rather than the anode, removing the risk of substrate leakage.

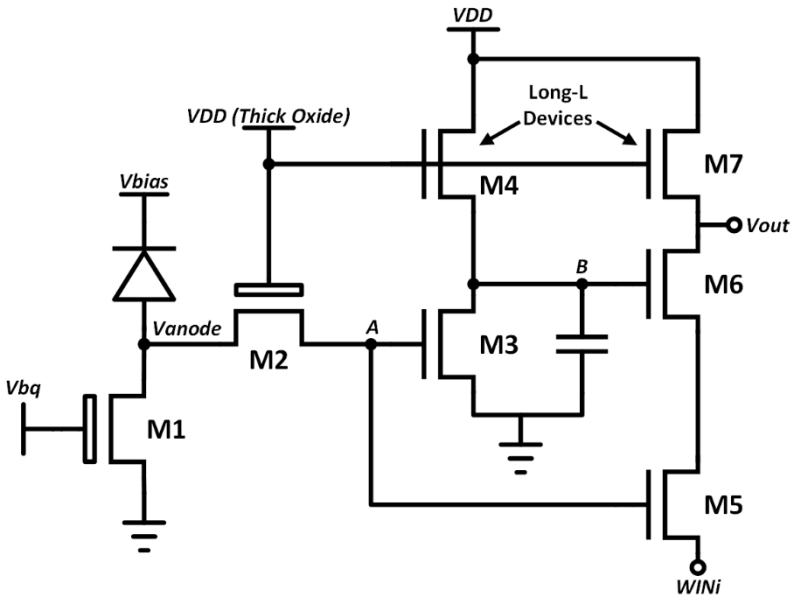


Figure 68: Passive quenching circuit from PDC1

The circuit's operation begins with steady state conditions, where the anode voltage, Vanode (and by extension node A), is pulled low by the resistive quenching transistor M1 while the outputs of the inverter, node B, and the NAND gate, Vout (the output), are high. When the SPAD avalanches, a pulse is generated across M1 and clamped by M2, yielding a pulse at node A that turns on M3 and M5 (assuming that WIN is high). Because of the presence of the capacitor, node B is slow to go low, so for a brief moment both M5 and M6 are on and bring the output voltage down. However, once the inverter is able to discharge the capacitor enough, M6 turns off, causing Vout to rise once more. Throughout this process, the SPAD is passively quenched due to the initial voltage drop across M1 and gradually recharges as Vanode is pulled back down to ground. Once this occurs, the circuit returns to steady state and can again detect another photon. In this configuration, the photon-signaling output is a falling-edge pulse with a width determined by the amount of time it takes for the capacitor to be discharged to the point of turning off M6.

5.3 Original Analog Counter Design

The output pulses from photon detection circuits are useless if the quantity of pulses that transpire over a time period cannot be tracked, which is why integrated counters are used. While digital flip-flop-based counters are among the most common counters implemented in integrated circuits in general, their use in photon counting applications can be limited due to the amount of space required on-chip to incorporate them. For this reason, analog counters are typically used instead, as they allow for effective photon counting with lower power consumption and layout area [5]. The analog counter design used in PDC1 was also inspired by the design outlined in the published passive quenching circuit [20] and is shown below.

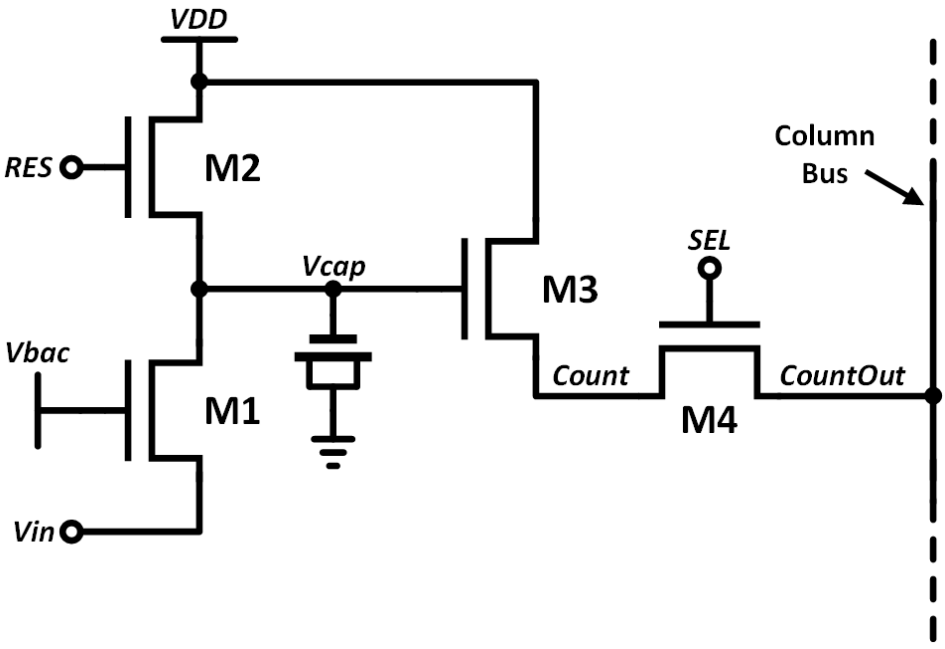


Figure 69: Analog counter circuit

The counter functions by removing small packets of charge from the capacitor by sending a series of falling-edge input pulses to the source of M1 and can be reset at any time by

recharging the capacitor via M2. The width of the input pulses and the user-controlled bias voltage, Vbac, on the gate of M1 determine the amount of charge removed from the capacitor. Each time a charge packet is removed, the voltage across the capacitor drops, causing the output of the source follower (transistor M3) to fall by a fixed amount. When the output is ready to be read and passed on to an analog-to-digital converter (off-chip), the select signal, SEL, goes high and allows M4 to pass the final analog count to the column bus for read-out. MOSCAPs were used in the original design to minimize layout area at the expense of non-linearity for large counts, which can result in excessive bias reduction across the device (MOSCAPS perform better when biased sufficiently high to operate in the strong inversion region [6], at lower biases the capacitance will vary). Figure 70 shows the layout of the passive quenching circuit interfaced with the analog counter as designed in PDC1.

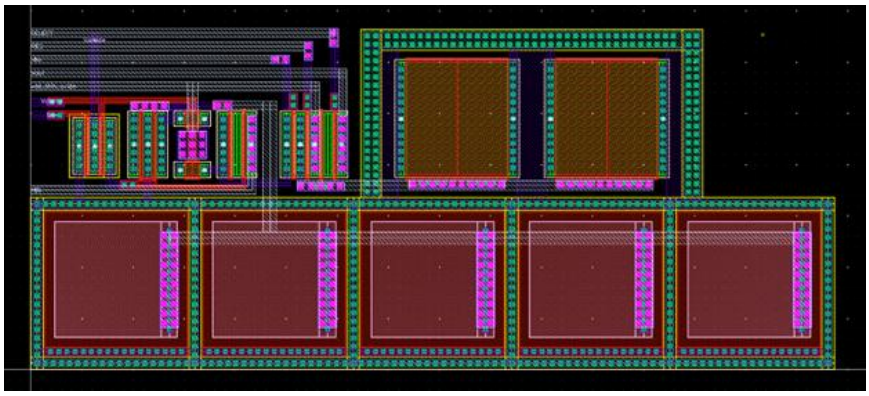


Figure 70: Original passive quenching and analog counter circuit layout by Gonzalo Arteaga

5.4 Existing Chip Design Testing

In order to adequately test the PDC1 chip in an efficient manner, a chip-on-board (COB) PCB had to be developed that was capable of accommodating integrated circuits wirebonded to

CQFJ-28 packages while also allowing easy interfacing with Thorlabs brand integrating spheres. Integrating spheres are cube-encased spherical cavities coated with a special reflective material that allows for the uniform distribution of light and are commonly used in optics. In the context of photon detection, these spheres can be used to distribute light from an LED onto the chip, which would be optically coupled to the sphere. The PCB was a redesign of a board previously developed by Bryan Kerstetter for the same chip that was tailored for SSOP-28 packaging.

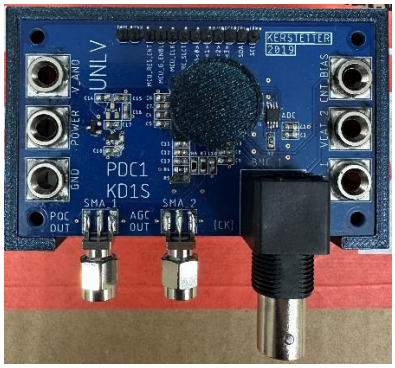


Figure 71: Original PDC1 board

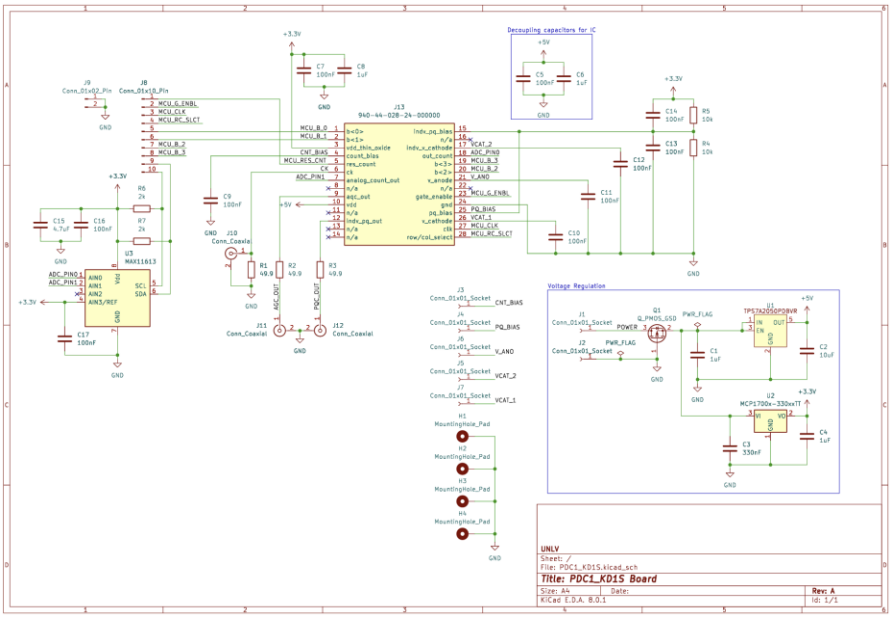


Figure 72: New PDC1 board design schematic (done in KiCAD)

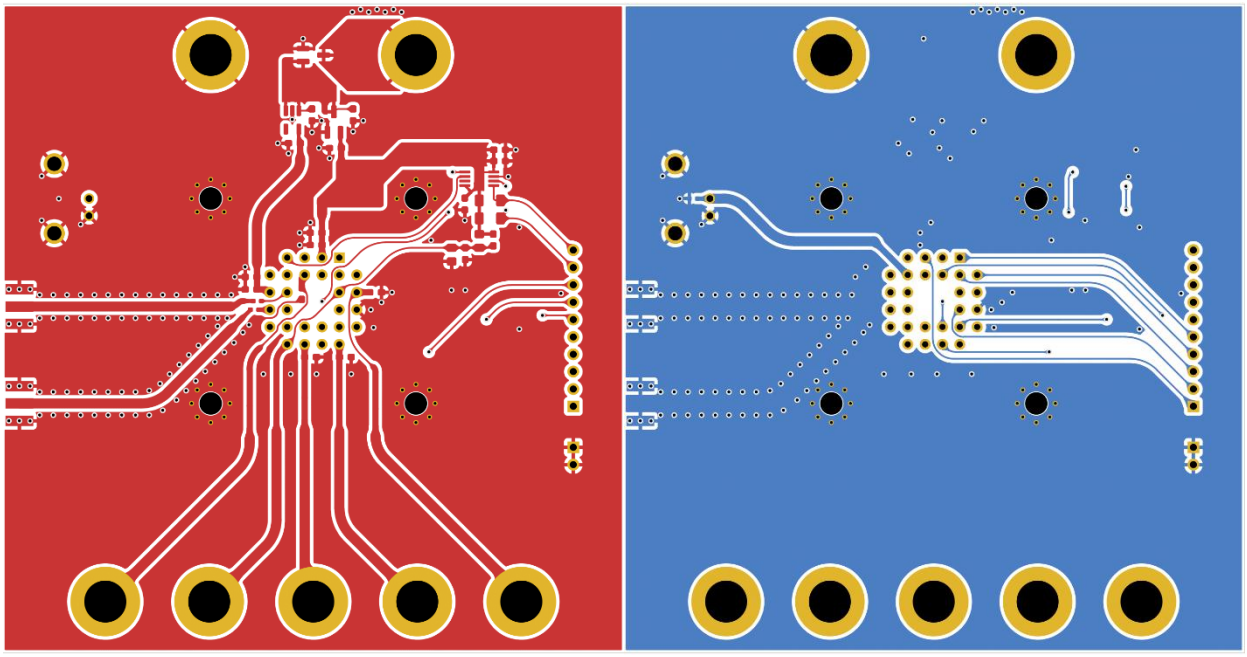


Figure 73: New PDC1 board design front (left) and back (right) copper layers

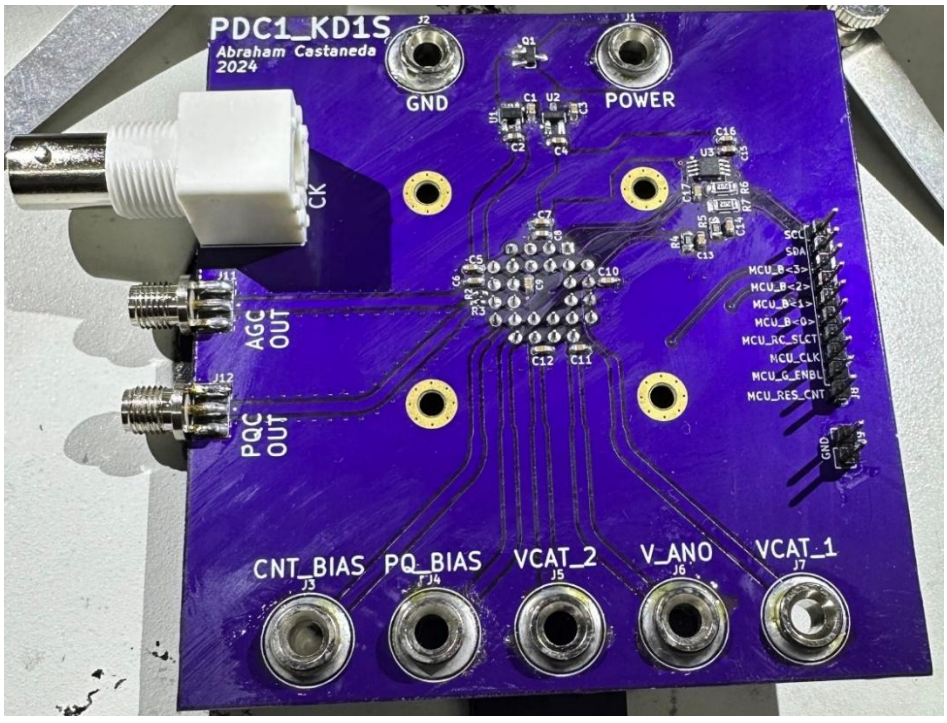


Figure 74: Assembled PCB front view

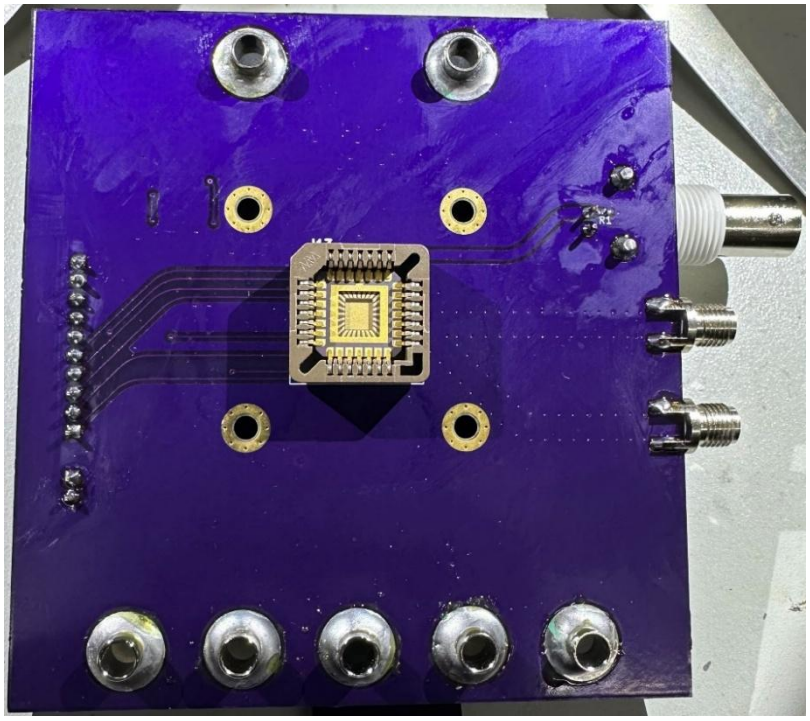


Figure 75: Assembled PCB rear view showing CQFJ-28 package and receptacle

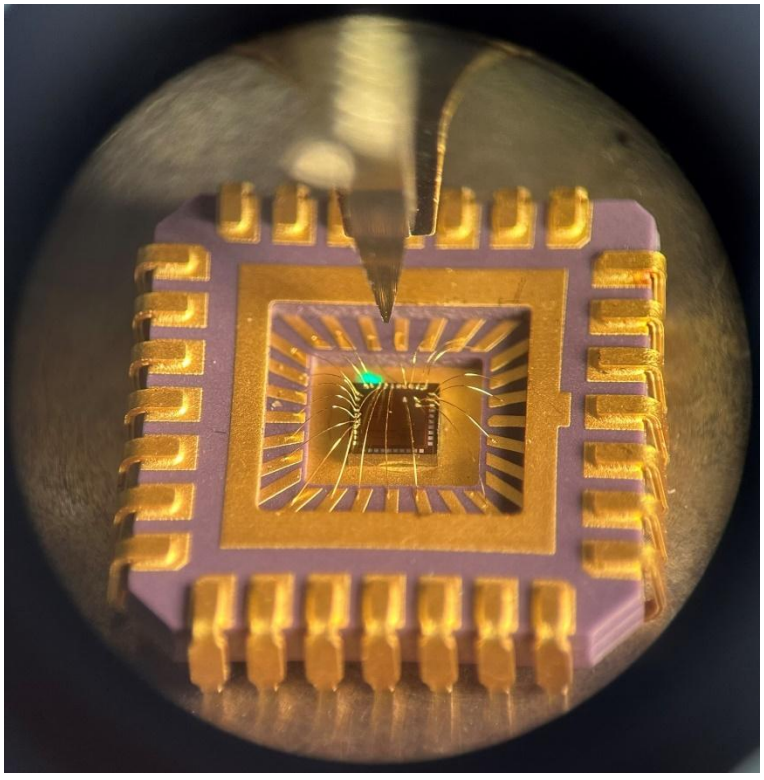


Figure 76: PDC1 chip wirebonded to CQFJ-28 package

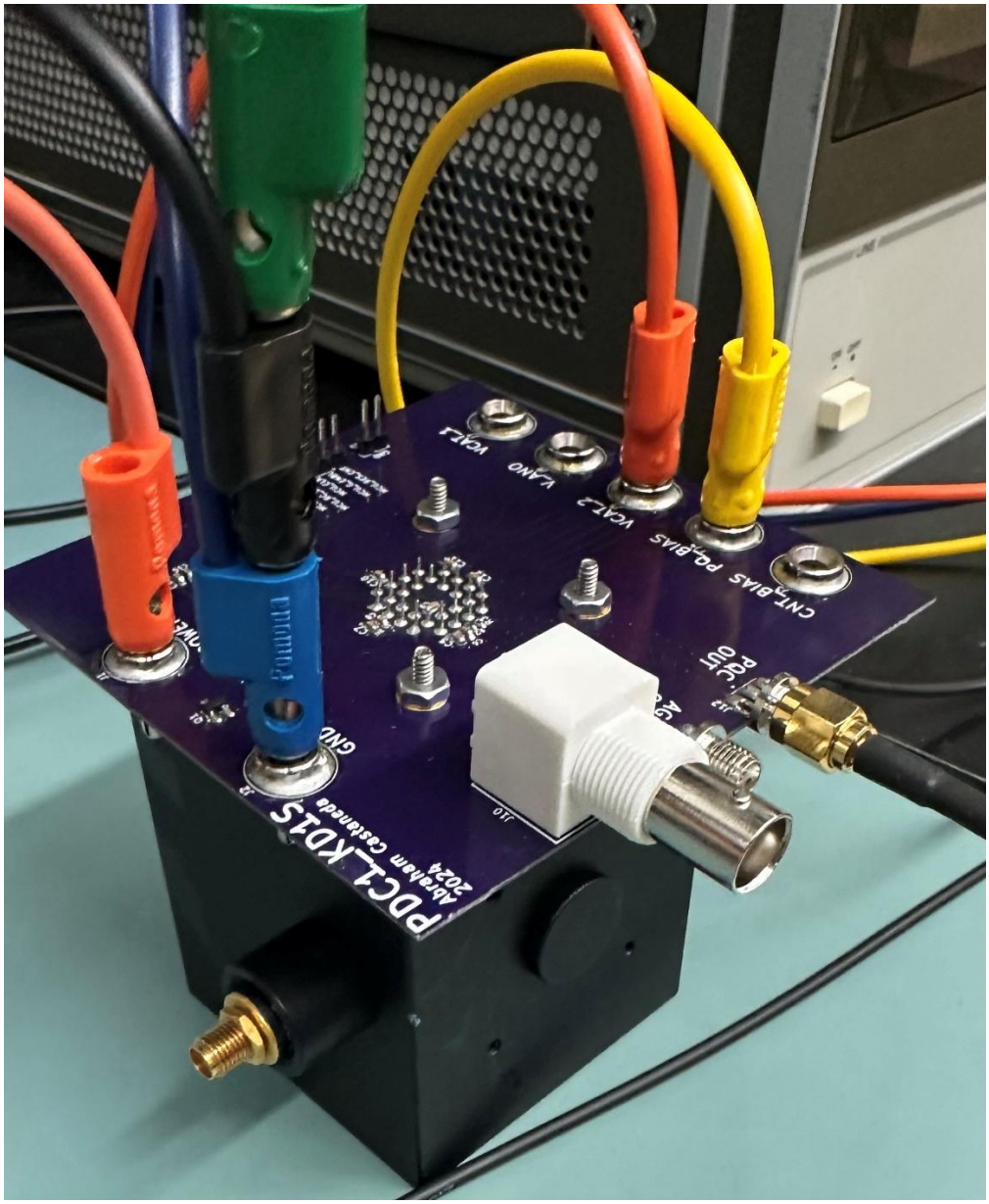


Figure 77: Board connected to integrating sphere

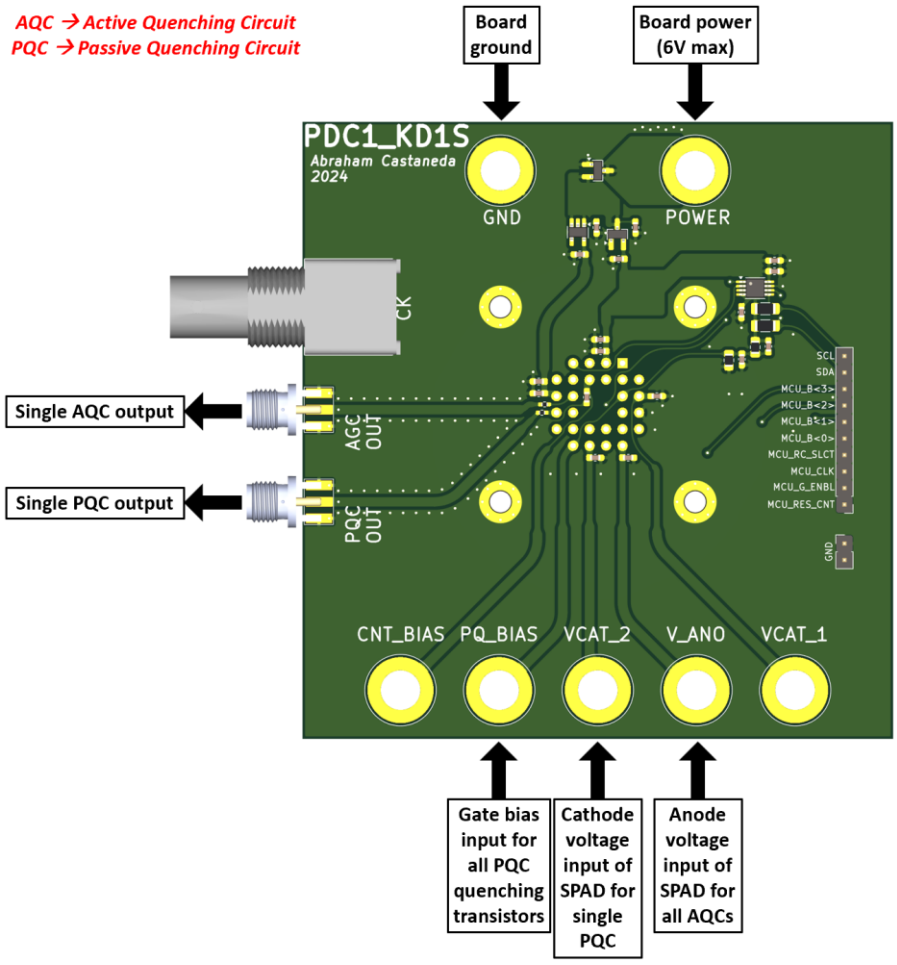


Figure 78: PDC1 connections used for single quenching circuit testing

The buffered single passive quenching circuit output on the board was generated by a circuit comprised solely of transistors M1 and M2 from figure 68, which was meant to provide a simple means of comparing its timing performance to the active quenching method. Through trial and error, it was determined that a SPAD biasing of 13.18V and a quenching transistor bias of 1.2V provided the ideal conditions for pulse generation. Testing the chip in a dark environment revealed that the narrowest pulse width possible was about 4.3ns wide, but when ambient light was allowed to illuminate the chip, the pulse widths could range from 6.3ns to

nearly 400ns long, indicating that the SPAD combined with the passive quenching configuration was prone to saturation and long reset times, which was expected.

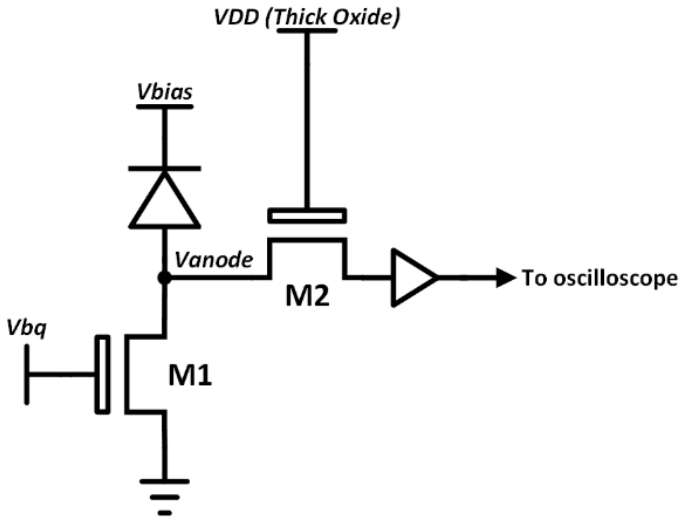


Figure 79: Single PDC1 passive quenching circuit for testing

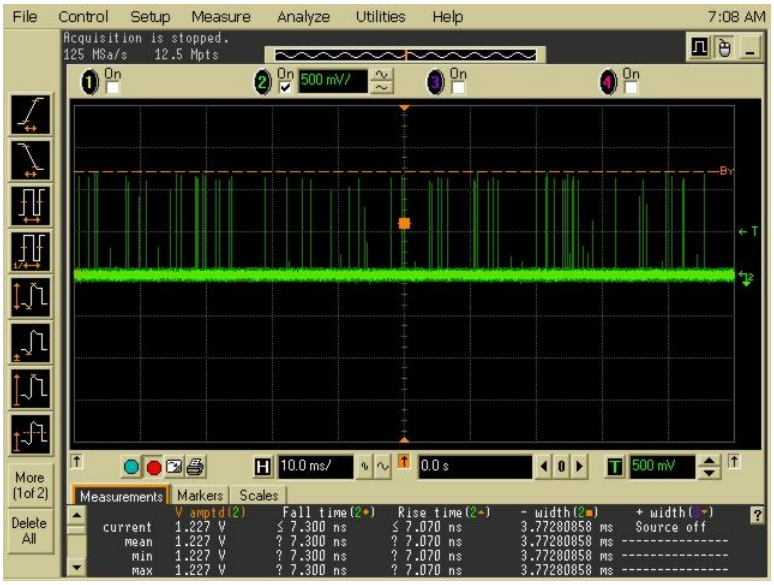


Figure 80: Single passive quenching output pulses

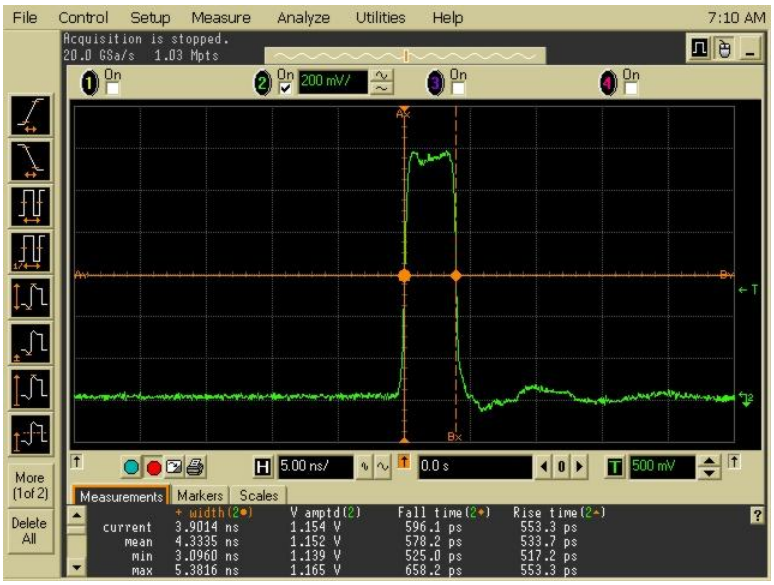


Figure 81: Narrow passive quenching pulse

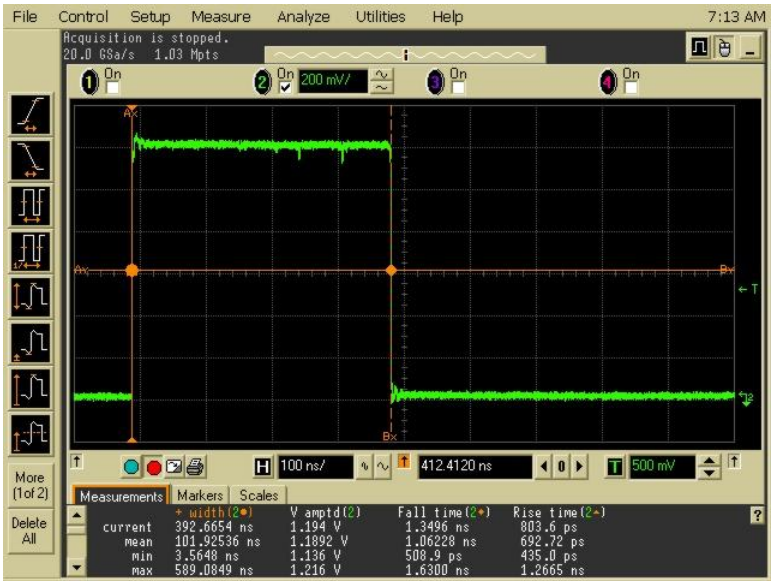


Figure 82: Wide passive quenching pulse

For the single active quenching circuit, unlike the single passive quenching circuit, the output on the board was generated by the circuit in its entirety, with the output signal being a buffered and inverted form of the output Vout (see figure 83). What was immediately noticed

however, was that the circuit would output a series of pulses despite the SPAD being biased far below breakdown. The pulses in question were spaced uniformly apart, and appeared to be oscillations of some form where the frequency would increase with the reverse bias applied to the device.

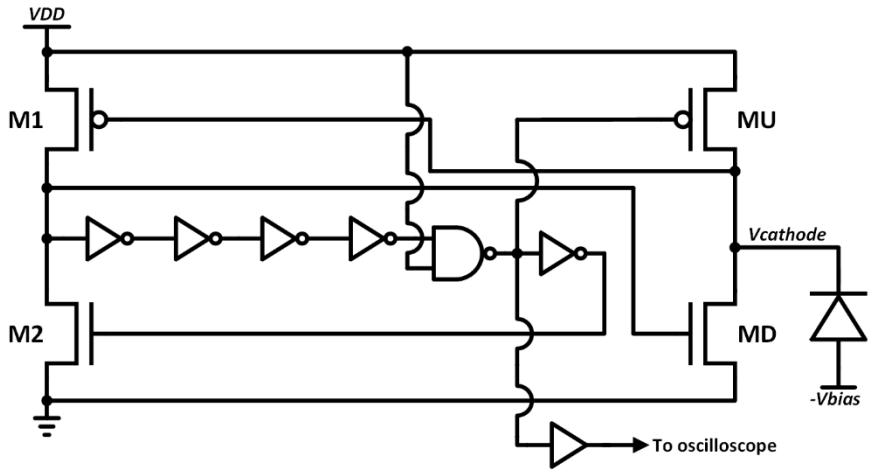


Figure 83: Single PDC1 active quenching circuit for testing

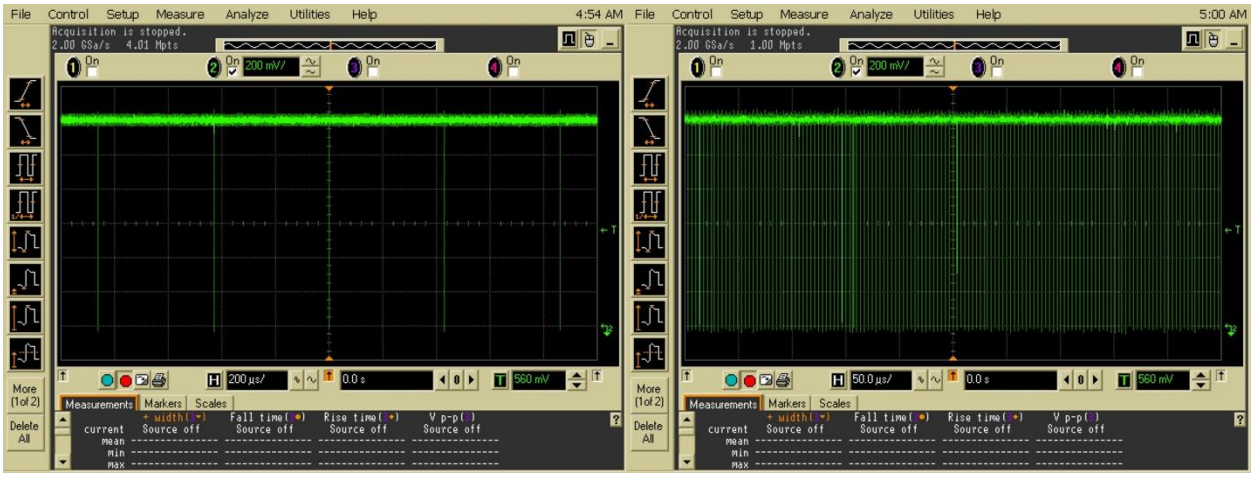


Figure 84: PDC1 active quenching oscillations with 0V at anode (left) and -0.75V at anode (right)

Figure 85: Zoomed in waveform of oscillation pulse

The suspected cause of this behavior was determined to be leakage current from the SPAD the circuit was connected to, which over time would slowly discharge the voltage at the cathode until it was low enough to activate transistor M1 and be mistakenly registered as an avalanche, resulting in a steady stream of self-induced quenching events. As discussed in section 2.3, leakage current is a small, but constant current that can flow through the SPAD when it is reverse biased regardless of illumination levels. After redesigning the circuit in LTspice, simulation results confirmed that a leakage current as small as 5nA is indeed capable of producing this unwanted effect.

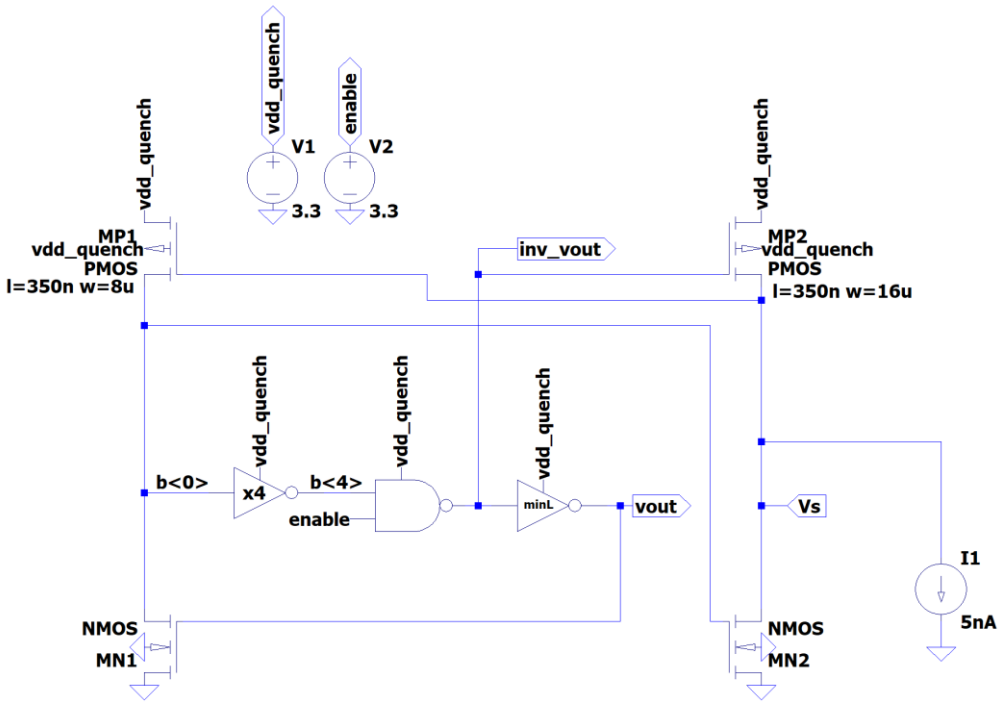


Figure 86: PDC1 active quenching circuit implemented in LTspice

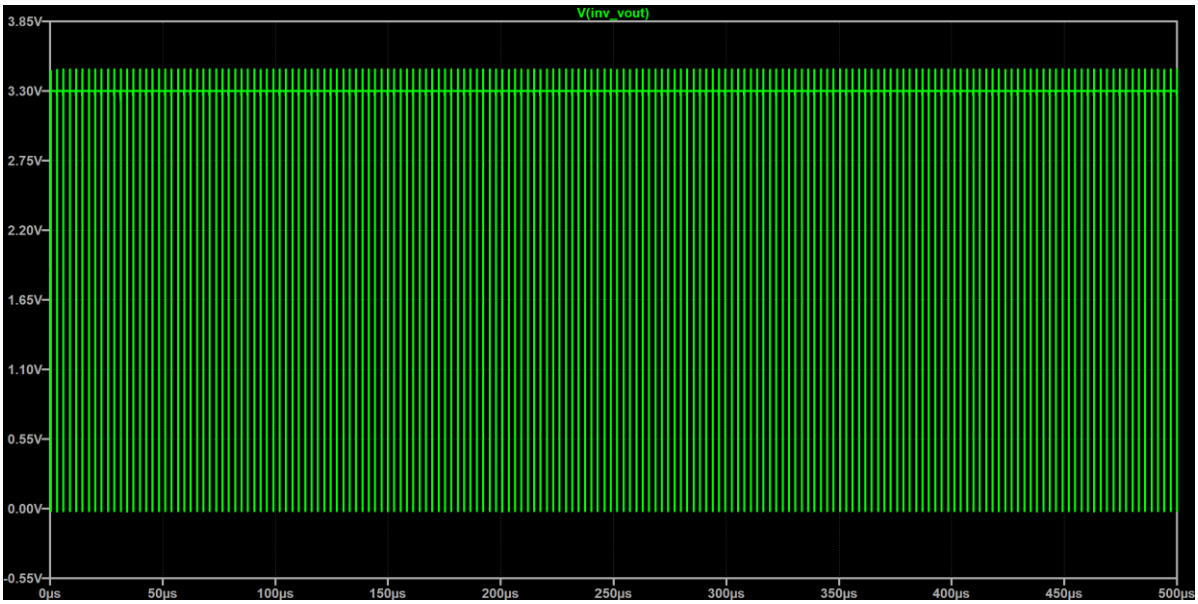


Figure 87: PDC1 active quenching simulation showing oscillations with 5nA leakage current

Although there is not much that can be done to completely eliminate leakage from a SPAD, there are many measures that can be taken to make quenching circuits more formidable against these kinds of malfunctions. The simplest of these solutions involves the inclusion of an active current source load to counteract any leakage current that would otherwise trigger the circuit. In addition to mitigating false triggers, the incorporation of weak pull-up/pull-down devices has the added benefit of providing a passive resistance that can be used to perform passive quenching, which can partially assist in the active quenching process. Figure 88 shows an alteration to the PDC1 active quenching design that may have prevented oscillations from occurring.

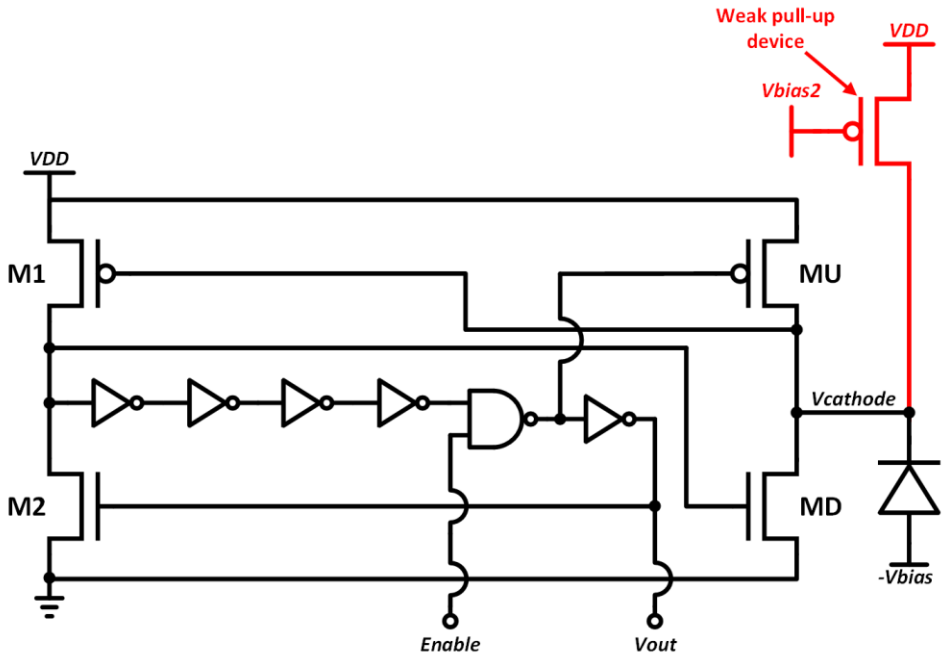


Figure 88: PDC1 active quenching circuit with possible remedy

CHAPTER 6: PROPOSED 180NM ACTIVE QUENCHING DESIGNS

Although the active quenching design in figure 88 may have worked, there was an inclination to avoid any designs that required large negative voltages being applied to the cathode on-chip due to the risks involved. For this reason, new anode-centric active quenching approaches needed to be developed, requiring thick oxide front-end circuitry similar to the PDC1 passive quenching circuit. This chapter describes the operation of two new time-gated active quenching circuit designs that meet the performance metrics needed for the physics application. Both designs include user-controlled adjustments that can be used to compensate for any non-linearities inherent to the SPAD that may not have been captured by the SPICE model developed in chapter 4. Furthermore, active paths for leakage currents are also provided within the designs to prevent false triggers. The operating conditions assume that the SPAD will be biased at the maximum level of 13V to maximize the size of the SPAD-generated signal.

The circuits in question were developed using the TSMC 180nm process models, with 350nm thick oxide devices, which were identical enough to the TowerJazz models to perform design and simulation in LTspice and allowed for easier integration of the SPAD SPICE model. Since the minimum length of the thick oxide device was close to double the thin oxide device minimum length, the lengths of all thick oxide devices were made to be 360nm rather than 350nm in order to facilitate a more orderly layout. Level shifters (both inverting and non-inverting) were also utilized to enable combined thin and thick oxide device operation. Simulation results of the proposed circuits will be covered in chapter 7.

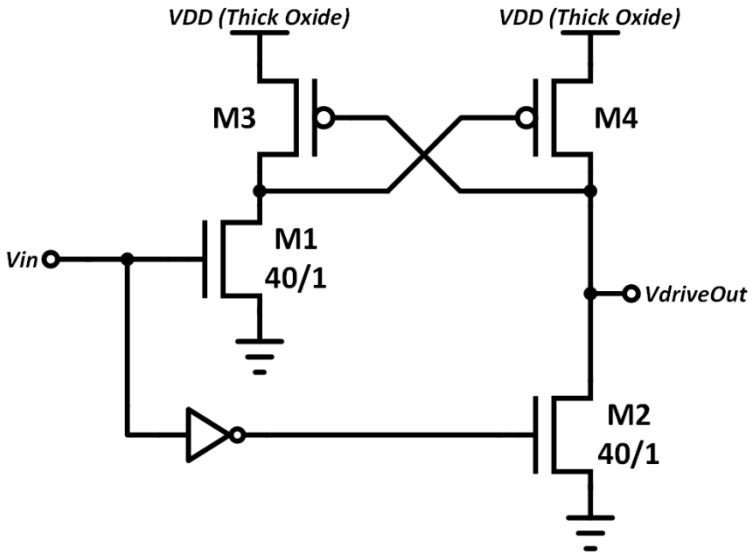


Figure 89: Non-inverting 1.8V to 3.3V level shifter

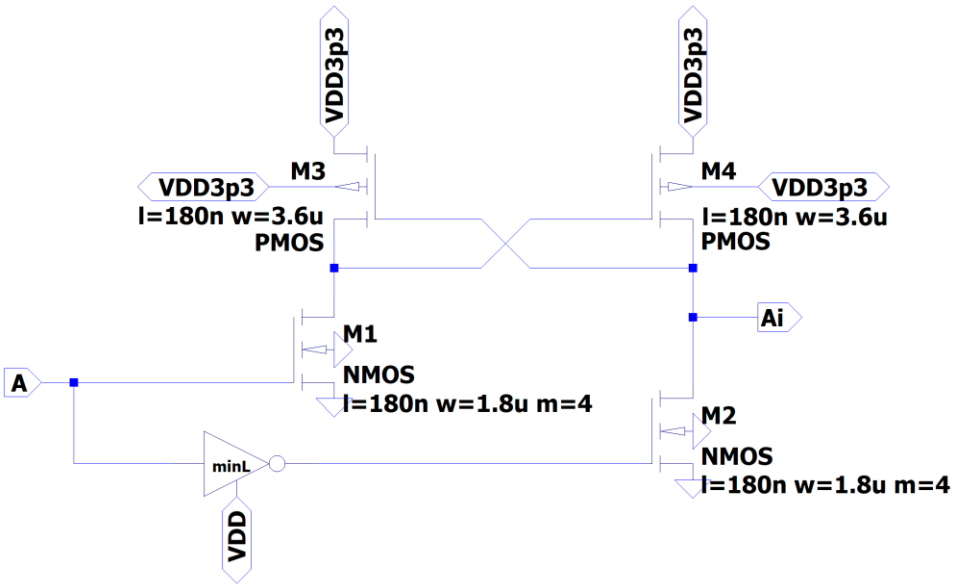


Figure 90: Non-inverting level shifter LTspice implementation

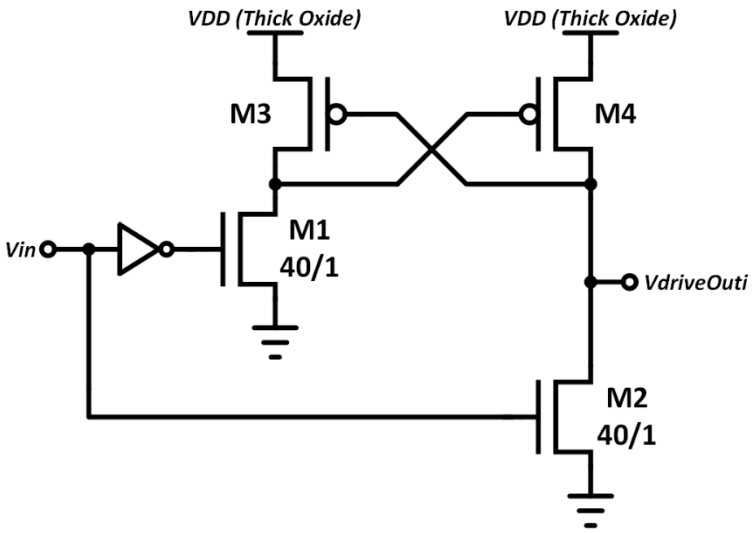


Figure 91: Inverting 1.8V to 3.3V level shifter

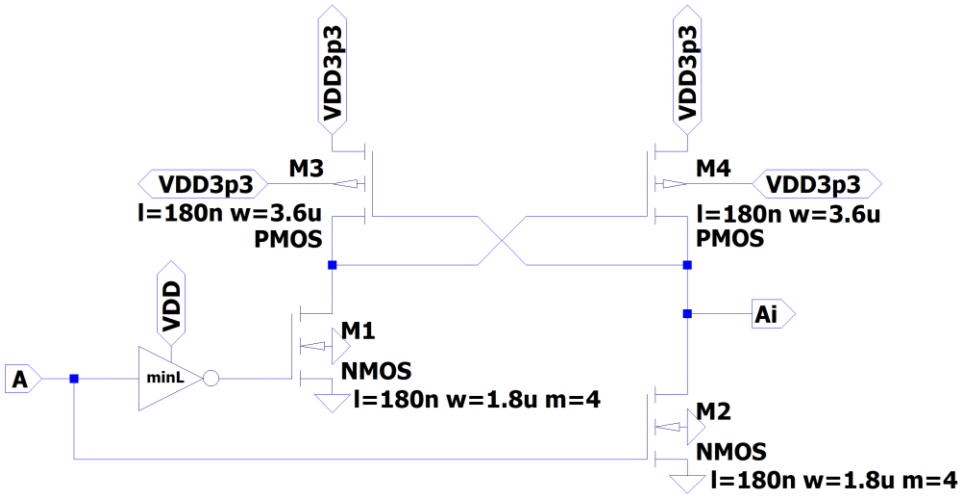


Figure 92: Inverting level shifter LTspice implementation

6.1 Variable-Load Active Quenching Design

The first design's mode of operation takes inspiration from the quenching approach developed by Tisa et al. [21], where the current of the SPAD is used to quench itself rather than applying an external voltage, although the circuitry used to do so differs from the referenced text.

This self-quenching method involves taking advantage of the SPAD's characteristic IV curve and a variable active load to induce quenching. The user-controlled digital input WIN (1.8V logic) in this design acts as an enable that can be leveraged to perform time-gated photon counting for specified time windows.

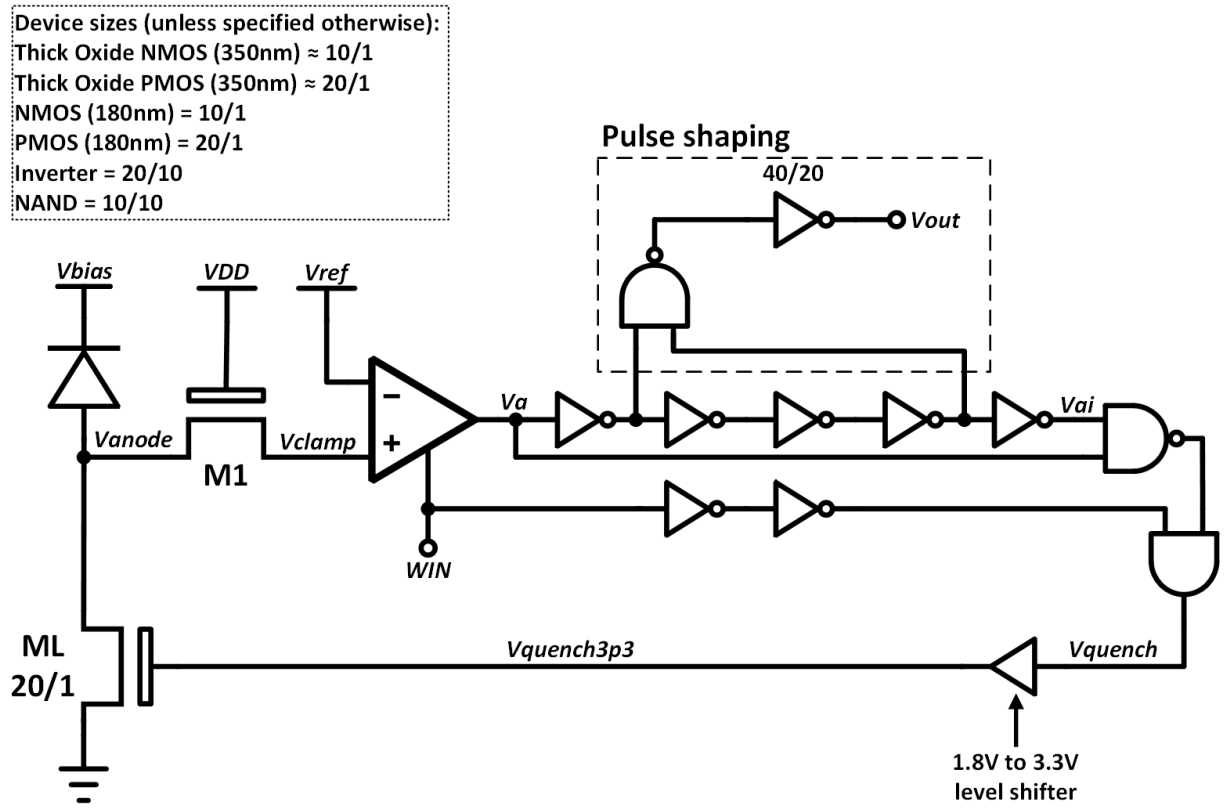


Figure 93: Variable-load active quenching circuit

In this circuit, both the quenching and resetting of the SPAD is performed by a single thick oxide load transistor, ML, that is initially fully activated with its gate driven to 3.3V by a level-shifted high AND output, which keeps the anode at ground and provides a low resistance load, Ron, to the SPAD. At steady state, the output of the comparator, Va, is low, resulting in a high signal on the output of the inverter chain, Vai. Upon detecting a photon, the voltage at the

anode quickly rises as the avalanche current decreases to converge with the current sunk by ML. However, because the current drawn by the transistor is fairly large, the anode voltage does not rise enough to quench the SPAD, resulting in a continuous avalanche current that gives rise to a steady DC signal with a magnitude below the excess voltage. This behavior is the same phenomenon responsible for the DC signals encountered when voltage mode testing was conducted using low-value passive quenching resistors and can be considered for all intents and purposes a “partial quench”.

Assuming that the comparator reference voltage, Vref, is adequately biased to sense the clamped anode voltage rise and that the time-window signal, WIN, is asserted, the comparator output responds by going high. This high signal bypasses the inverter chain and switches the NAND output low, which also brings the AND output low, deactivating ML in the process. The deactivation of ML results in a very high impedance load (Roff) on the SPAD’s anode that, combined with the already initiated avalanche current, immediately causes the SPAD bias to be reduced to the breakdown voltage (anode voltage rises to Vex), quenching it in the process. ML remains deactivated until the comparator output rise is able to propagate through the inverter chain and bring Vai low, at which point the NAND output will re-assert (along with the AND output), reactivate ML and pull the anode voltage back down to ground to reset the SPAD. In the case where WIN is low, both the comparator and level shifted AND outputs are forced low, which prevents further counts while simultaneously turning off ML and placing the SPAD in a constantly quenched state due to the high impedance at the anode. Two inverters are placed between WIN and the AND gate to grant the natural output of the comparator enough time to control ML and avoid conflicting outputs when reopening the time window.

While quenching is performed, two opposite nodes within the inverter chain are constantly tapped by a NAND gate to generate the rising-edge digital photon-detection signal. The monostable nature of this design helps keep the photon signal pulse widths narrow while also reducing the amount of time the SPAD spends in the quenching phase before being reset. This quenching process is illustrated in figure 94, showing that this approach operates under mechanisms similar to passive quenching, only that the resistance of the SPAD's load is actively varied throughout the circuit's operation.

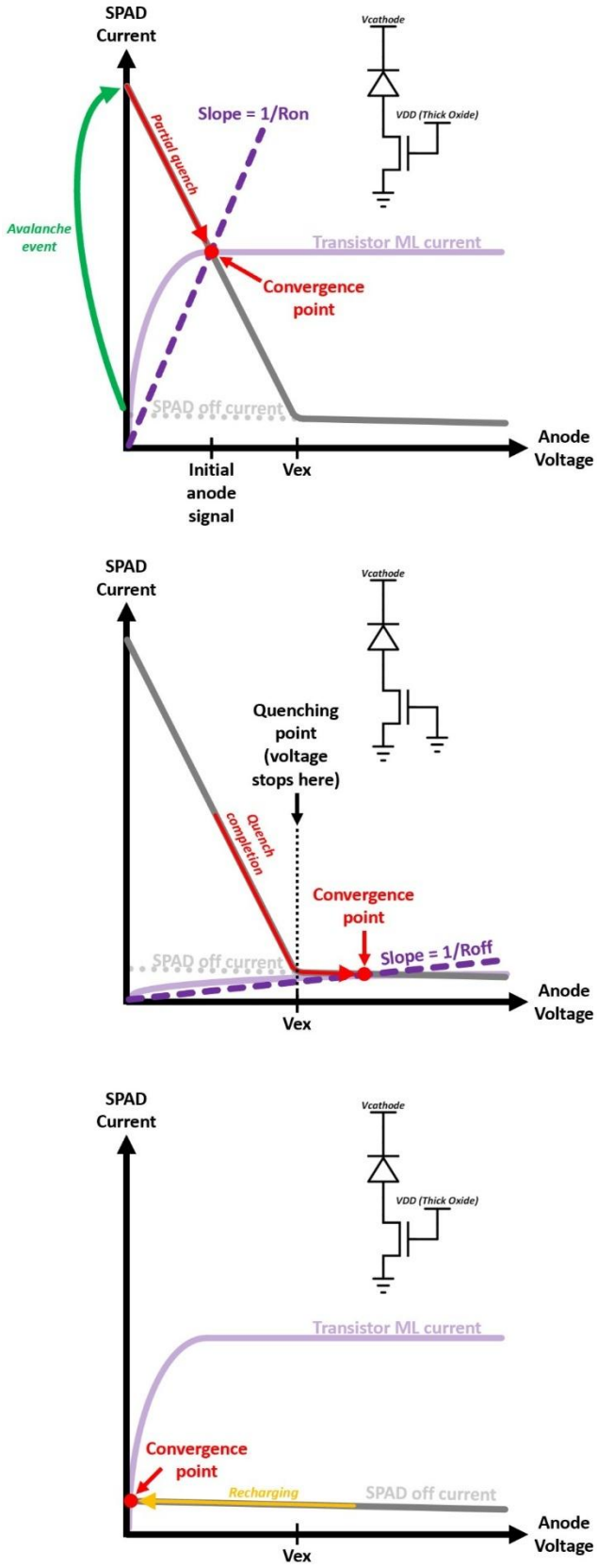


Figure 94: From top to bottom, the IV curve operation of the variable-load active quenching circuit

Since the initial anode DC signal can be too low to activate/deactivate regularly sized NMOS/PMOS devices, the use of a rail-to-rail differential amplifier comparator was determined to be the best approach for detecting the avalanche, as it ensures that the rising-edge anode signal can be detected across a wide input range to reliably trigger the following stages of the circuit. The comparator itself was designed using thin oxide devices, but is protected from the SPAD by a thick oxide clamping device, M1, with the gate tied to the thin oxide VDD, which ensures that the largest voltage the comparator is exposed to is approximately $\mathrm{VDD}_{\mathrm{ThinOxide}} - \mathrm{V}_{\mathrm{THN\_ThickOxide}}$, or 1.6V from simulations. Since speed over sensitivity was the primary goal, only one differential amplifier stage was used with an inverter placed on the output to buffer the signal. Additional devices were added to enable and disable the comparator through signal WIN.

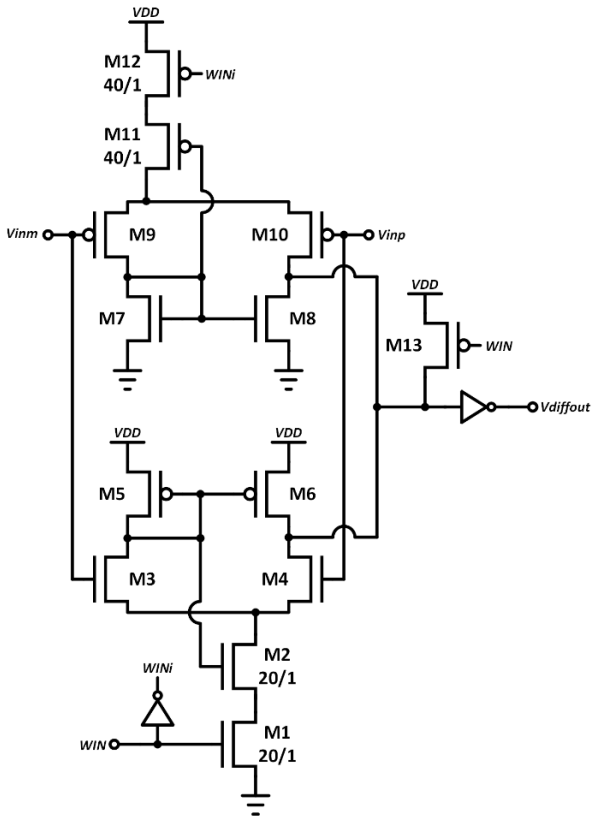


Figure 95: Comparator design

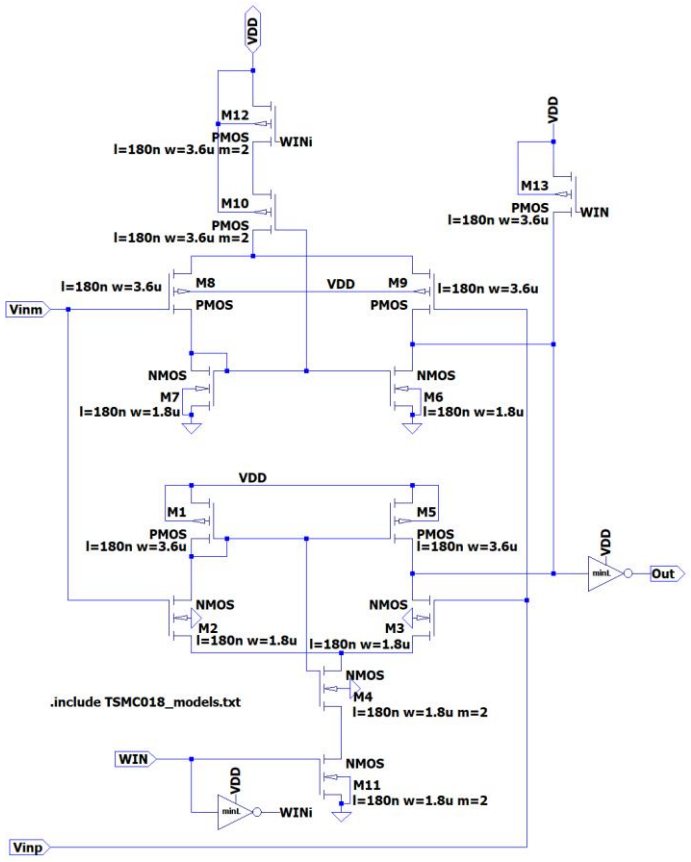


Figure 96: Comparator LTspice implementation

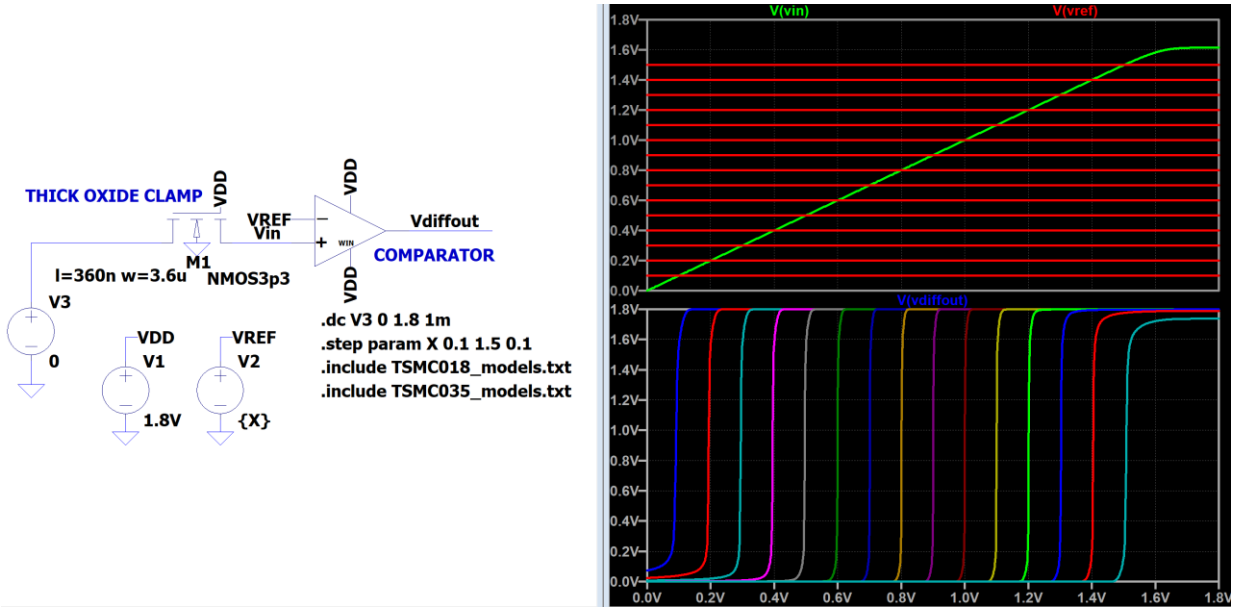


Figure 97: DC simulation of comparator with clamped input

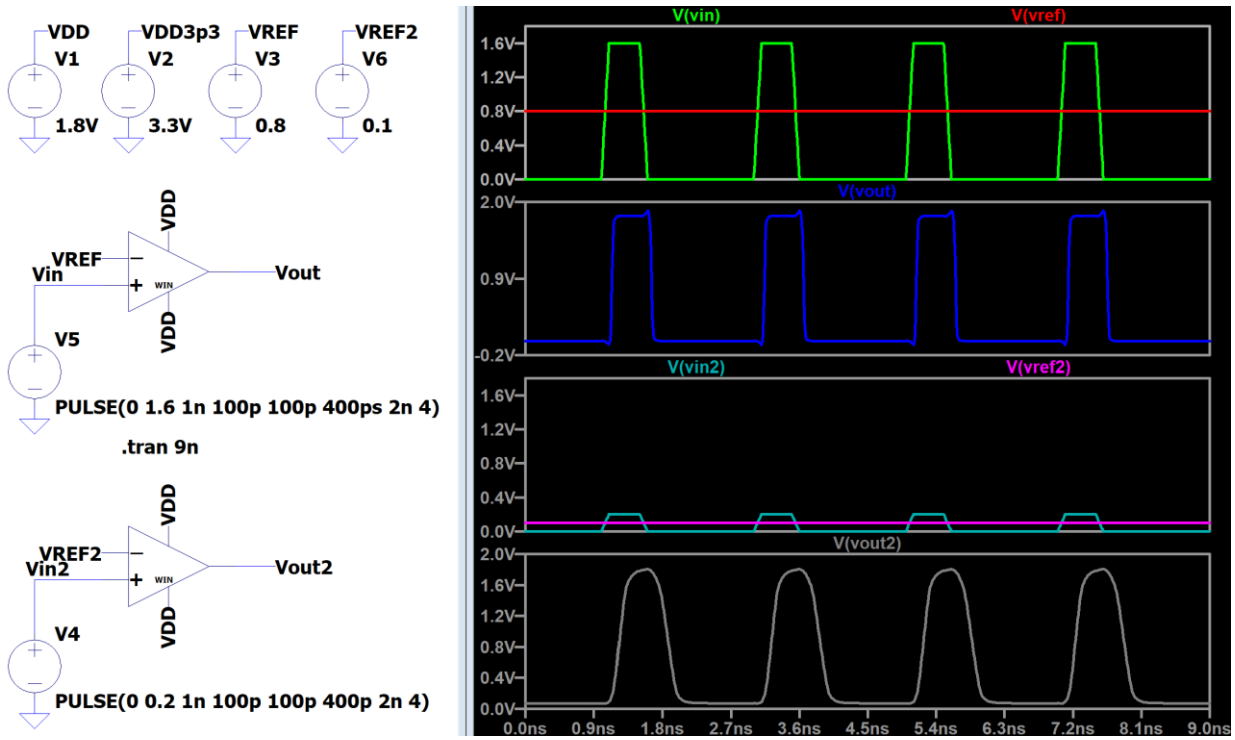


Figure 98: Simulation showing comparator responses to 400ps wide signals of varying amplitude

For the design to operate correctly, the DC reference input to the comparator, Vref, must be set to be less than the initial anode signal, which can be estimated by calculating the convergence point of the SPAD and MOSFET IV curves or determined experimentally by the user when the former is not viable. Using MATLAB to overlay the IV curves of the ML transistor and the SPAD model (based on its 466Ω internal resistance), it was estimated that with 13V biasing, the converging voltage level would be approximately 0.823V, so a 0.4V reference voltage would ideally work.

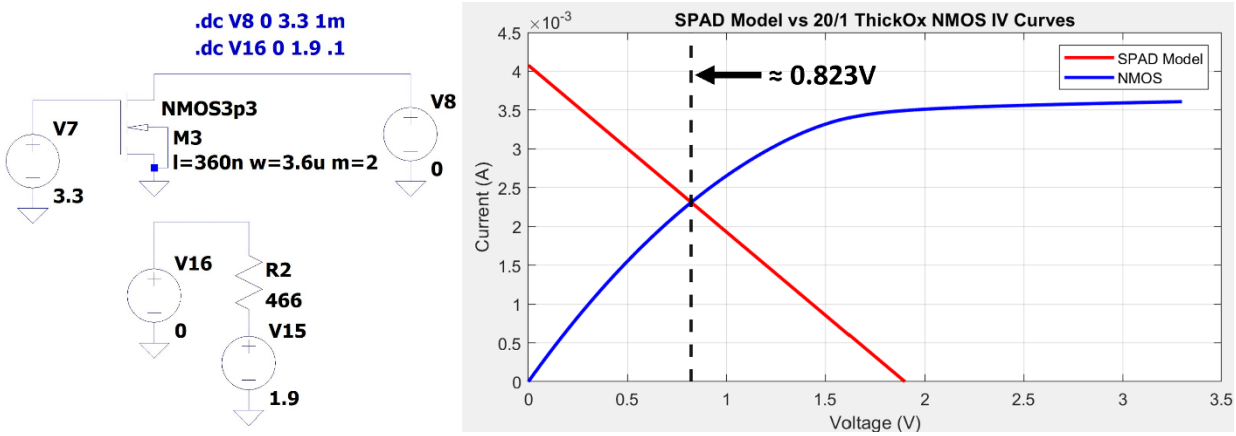


Figure 99: Determining convergence point of SPAD and variable-load transistor

Overall, the benefits of this design include minimal use of thick oxide devices, practical immunity to leakage currents due to the extreme current sinking provided by ML and a very simple mode of operation that is not dependent on too many user-controlled parameters.

6.2 Latching Active Quenching Design

The second design covered in this section falls more in line with traditional active quenching techniques and operates by using the thick oxide front-end to latch the anode to the thick oxide VDD, 3.3V, effectively reducing the bias from 13V to 9.7V whenever a photon detection is sensed by the circuitry. This key difference aside, the monostable aspect of the circuit is similar to the variable-load design and uses the same configuration to generate the narrow pulse-width photon-detection signal (NAND gate with inputs connected three inverters apart). Furthermore, time-gating can be implemented in the same manner using the 1.8V-level digital signal WIN.

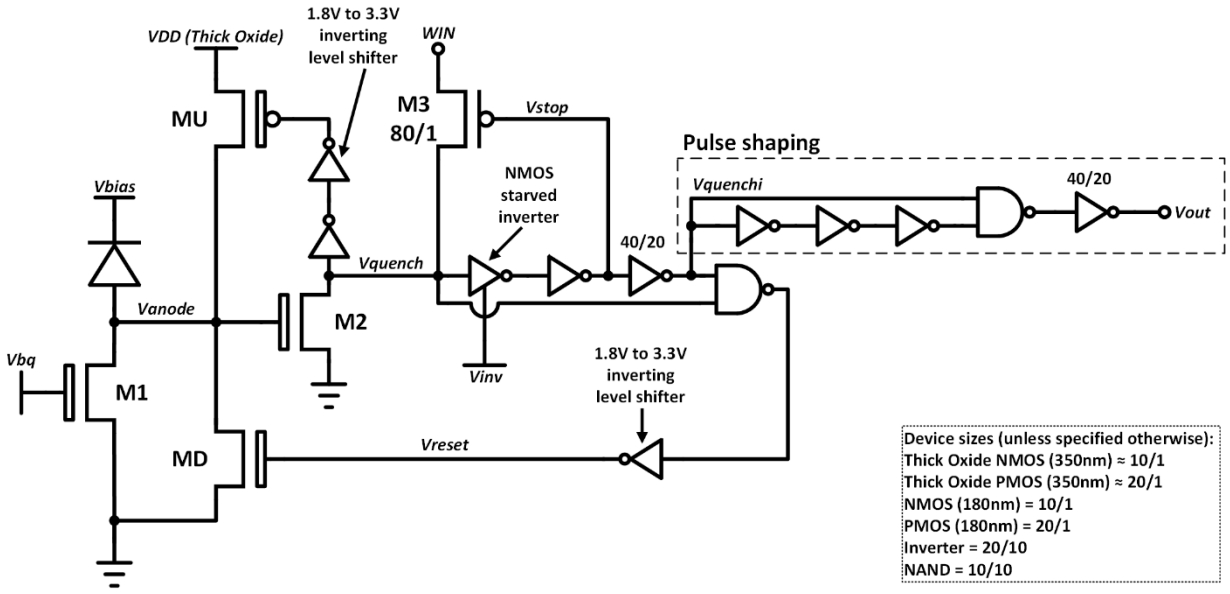


Figure 100: Latching active quenching circuit

At steady state, Vanode is low, M2 is off, nodes Vquench and Vstop are high, Vreset and Vquenchi are low, and M3 is off, along with the pull-up and pull-down transistors MU and MD. Operation of the circuit begins with user-controlled transistor M1, which must be biased with a voltage, Vbq, low enough to provide a high enough resistance load at the anode to passively quench the SPAD. The motive behind this is to ensure that the anode pulse reaches the highest magnitude possible so that the avalanche sensing transistor, M2, is properly triggered. However, M1 should not be too weak to sink the SPAD's leakage current, which for most CMOS SPADs is typically in the picoampere to nanoampere range. To err on the side of caution, a Vbq value ranging from 0.56V to 0.73V is recommended and will enable passive quenching while still allowing the device to sink up to 1uA of leakage current.

When the SPAD detects a photon and is passively quenched by M1, M2 is activated by the resultant anode pulse. The activation of M2 pulls Vquench to ground, which immediately activates MU, latching the anode voltage up to 3.3V to quench the SPAD. As this takes place, the

falling edge of Vquench propagates through the inverter chain, brings Vstop low and activates M3 (assuming that WIN is high). Since M3 is stronger than M2, it is able to pull Vquench high despite the 3.3V voltage at the gate of M2, which deactivates MU. By the time Vquench is pulled high, it's previous low state will have already propagated and made voltage Vquenchi high as well, which causes the NAND output to go low, bringing Vreset high and turning on MD to ground the anode to reset the SPAD. To allow enough time for MD to reset the SPAD before disabling the M3 latching of Vquench (which keeps MU off), the propagation of Vquench going high is intentionally slowed down by using an NMOS-starved inverter at the beginning of the inverter chain, an inverter variant with a 5/1 sized NMOS connected the inverter's NMOS source.

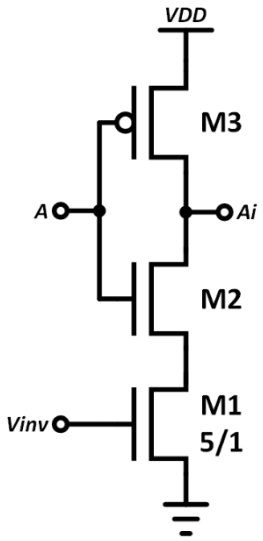


Figure 101: NMOS-starved inverter

The extent to which this inverter is starved of current is set by user-controlled bias Vinv. For proper operation, the inverter must be slow enough to prevent M3 from turning off before the anode is grounded (otherwise Vquench will fall and trigger an extra quench), but fast enough to

turn off MD before the next detection period (otherwise the bandwidth decreases). Simulations suggest that a bias between 0.82V and 0.90V makes this feasible. When the rising edge of Vquench eventually propagates through the inverter chain, M3 is disabled along with the level shifted and inverted NAND output, turning off MD and returning the circuit to the ready state. It is during the first Vquench falling-edge inverter-chain propagation that the pulse-shaping section generates the digital photon-counting signal. In the case where WIN is low, M3 is prevented from pulling Vquench back up after the initial sensing and quenching operation, which keeps the SPAD anode latched to 3.3V. The latch formed by M2 and MU keeps the SPAD quenched until the user asserts WIN to allow the circuit to proceed with the reset operation and continue photon counting.

Although this design's operation is slightly more complex and sensitive to the user input bias provided to the inverter, the significant benefit to this quenching method is the increased reduction of the SPAD bias. While having the SPAD be quenched down to the breakdown voltage (as passive quenching accomplishes) works for stopping the avalanche, the added step of forcing the bias even further below breakdown drastically reduces the electric field strength within the device post-avalanche and helps to prevent residual trapped charge carriers from accelerating and causing undesirable after-pulsing effects, potentially reducing noise.

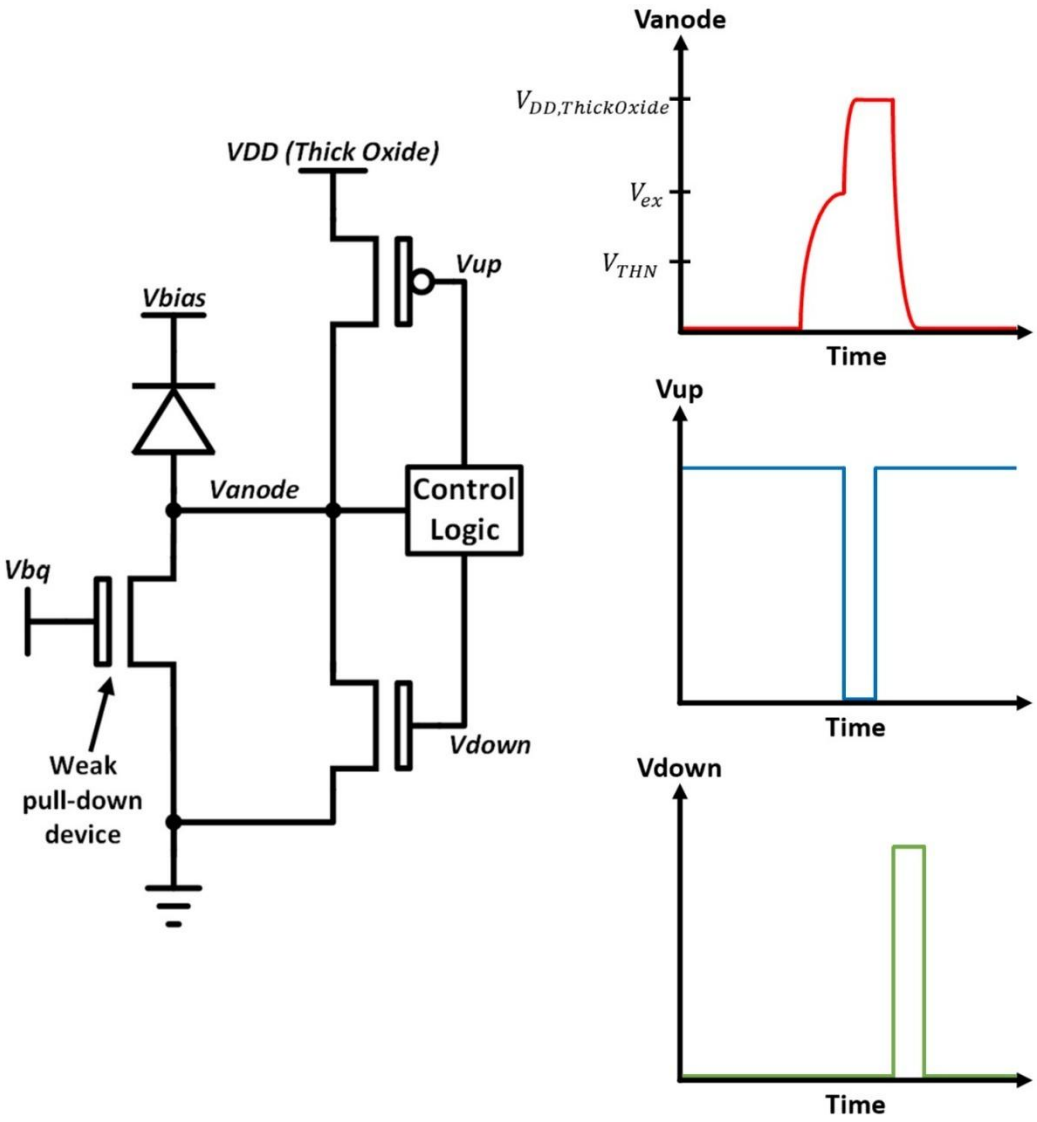


Figure 102: Latching active quenching circuit simplified operation

6.3 Analog Counter Design

With no fault to the design ever being evident from past projects, the PDC1 analog counter from figure 69 was adopted into the 180nm process, so with the exception of the dimensions, the design remained identical to the original. Figure 103 shows the analog counter schematic annotated with all of the non-nominal sizes used.

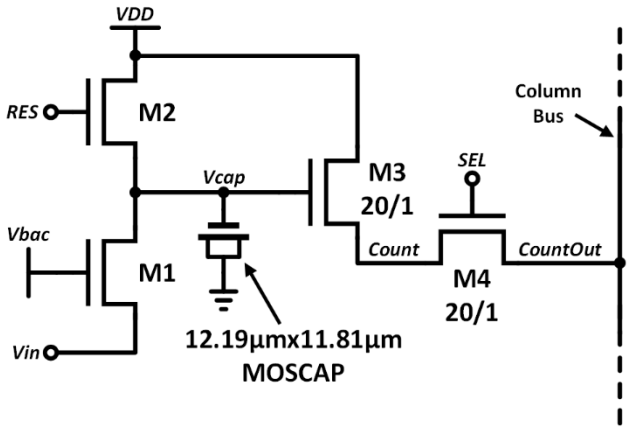


Figure 103: 180nm analog counter design

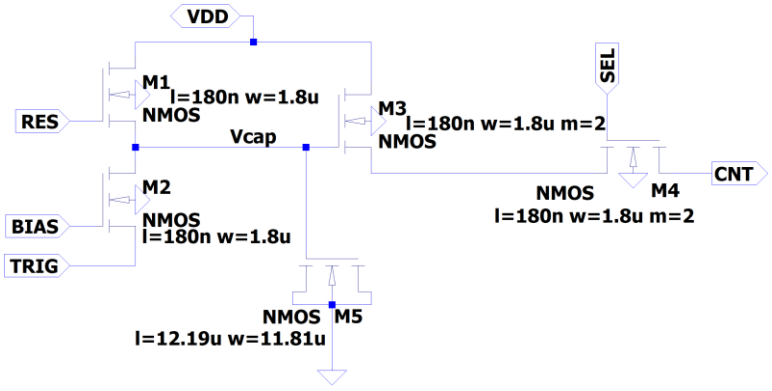


Figure 104: Analog counter LTspice implementation

What is not shown in the schematics above is the column bus loading transistor that is in charge of ensuring that the counter output is able to effectively go to ground after reaching the maximum number of counts. Without this loading, when the capacitor voltage falls too low and the source of M3 is not low enough, M3 begins turn off and becomes unable to continue tracking the discharge events. Simulations indicated that a 10/1 NMOS load, gate-driven at 0.7V, was sufficient to prevent this issue. The 12.19µm-by-11.81um MOSCAP provides a capacitance of approximately 1.2pF as long as it is operated in the strong inversion region and can be reset to

1.8V by driving transistor M2's gate with 3.3V. The reset time of the counter, including the time necessary for M3's source to reflect the capacitor recharge, is approximately 10ns. The output can be passed to a column bus by driving the gate of M4 with 3.3V. Regarding the counter resolution, 5-10mV per count was chosen as the ideal voltage step size as a compromise between maximizing the number of counts that can be done before necessitating a reset and reducing susceptibility to noise. The counter bias used to acquire this step size will be primarily dependent on the pulse width of the falling-edge trigger signal. Since the new active quenching designs exhibited pulse widths close to 100ps, a 0.85V bias provided ample driving power to the charge removal device M1 to achieve a 5-10mV step size. The counter can reliably perform about 70-80 counts before the voltage step size becomes non-linear and deviates from the expected value.

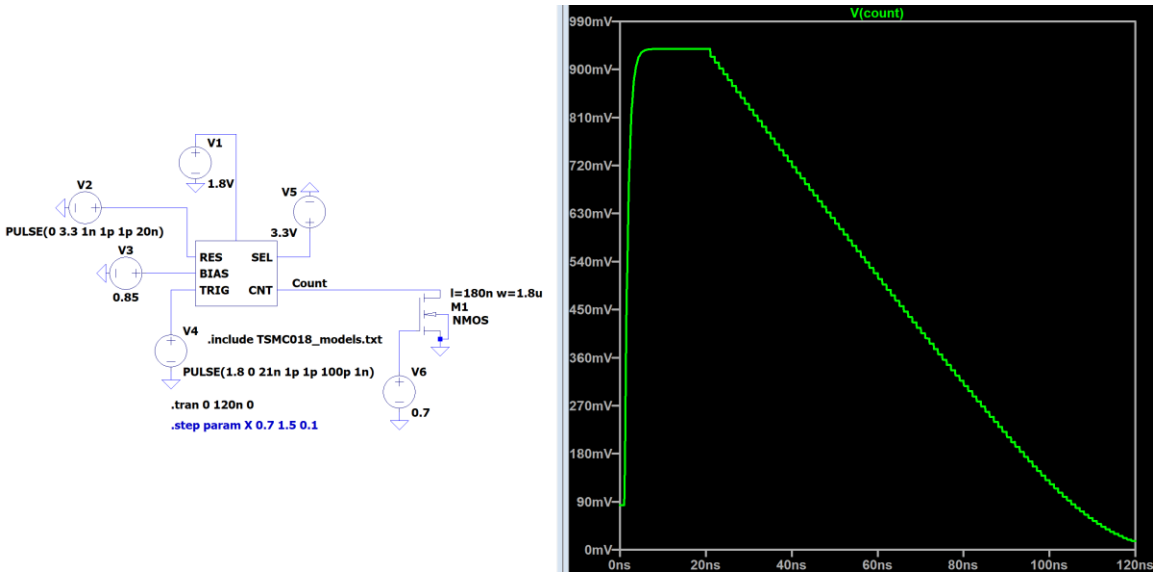


Figure 105: Analog counter simulation

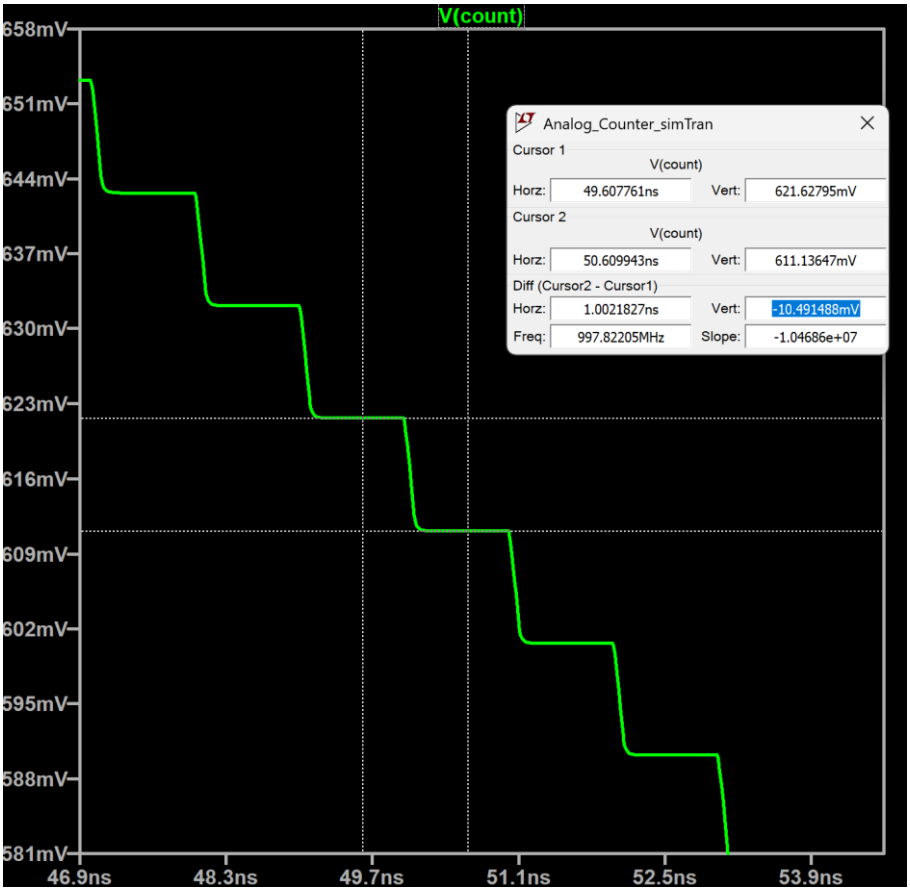


Figure 106: Zoomed analog counter simulation showing step size

CHAPTER 7: SYSTEM-LEVEL SIMULATIONS

This section details the simulation results of the active quenching designs discussed in chapter 6 using the 2H SiGe SPAD SPICE model, with the main metrics of interest being the reset time (the time it takes for the SPAD bias to recharge up to 99.3% of the applied reverse bias, or about 12.91V) and the FWHM of the digital photon-detection output. The operational limits of the user-controlled inputs will be shown as well as the designs' ability to handle leakage currents of up to 1uA. An attempt to simulate corners was made by adjusting the threshold voltage parameter (VT0) by $\pm 10\%$, the oxide thickness (TOX) by $\pm 5\%$, the carrier mobility (U0) by $\pm 15\%$, and the source-drain series resistance (RDSW) by $\pm 10\%$. Process corners represent the most extreme variations possible within the NMOS and PMOS devices fabricated in a semiconductor process that can affect the operation of integrated circuits, especially at high speeds. To ensure reliability, simulations are typically performed with the NMOS and PMOS models possessing various speeds, usually in the fast-fast, slow-slow, slow-fast, and fast-slow configurations.

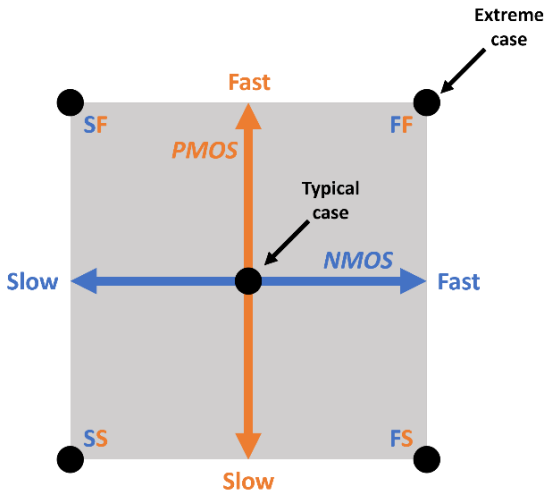


Figure 107: Illustration of process corners

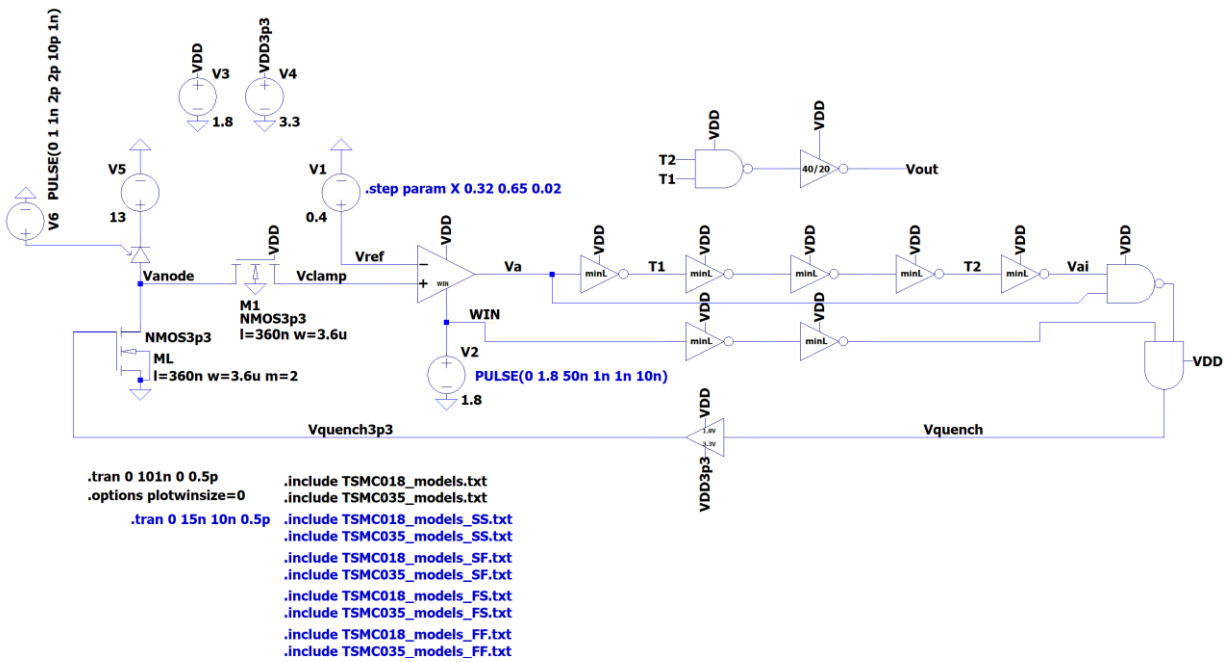


Figure 108: Variable-load active quenching circuit LTspice implementation

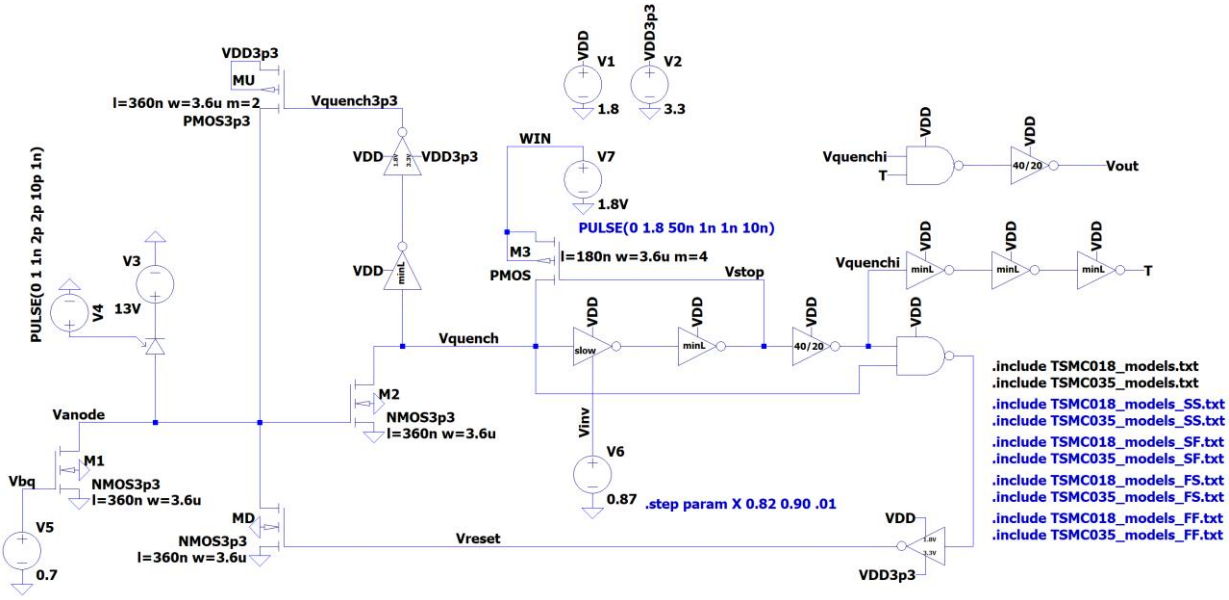


Figure 109: Latching active quenching circuit LTspice implementation

7.1 Combined Simulation Results Summary

The table below summarizes the simulated performance of both designs for typical and corner parameters using a 13V bias and a trigger rate of one photon per nanosecond. Each simulation was run over the course of 100 photon-trigger events, with the waveforms being analyzed after the hundredth quench and reset instance in order to ensure the removal of any initial conditions present within the circuit that could skew results.

TYPICAL NMOS / TYPICAL PMOS			
Design tested	Reset time	Output FWHM	Power consumption
Variable-load AQC	738ps	103ps	3.0mW
Latching AQC	735ps	73ps	4.9mW
SLOW NMOS / SLOW PMOS			
Design tested	Reset time	Output FWHM	Power consumption
Variable-load AQC	752ps	103ps	3.0mW
Latching AQC	786ps	73ps	4.9mW
SLOW NMOS / FAST PMOS			
Design tested	Reset time	Output FWHM	Power consumption
Variable-load AQC	752ps	103ps	3.0mW
Latching AQC	779ps	73ps	4.8mW
FAST NMOS / SLOW PMOS			
Design tested	Reset time	Output FWHM	Power consumption
Variable-load AQC	737ps	103ps	3.0mW
Latching AQC	716ps	72ps	5.0mW
FAST NMOS / FAST PMOS			
Design tested	Reset time	Output FWHM	Power consumption
Variable-load AQC	737ns	103ps	3.0mW
Latching AQC	693ps	73ps	5.0mW

Table 12: Quenching circuit simulation results

The results show that both designs are able to achieve sub-nanosecond reset times with photon-detection signal pulse widths at or below 100ps, well within the 1-2ns reset time and 100-500ps pulse-width metrics set for the intended application. The larger power consumption of the

latching AQC is an expected result of the contention current that is created between M2 and M3 during the SPAD recharging phase.

7.2 Variable-Load Active Quenching Simulations

The waveform windows shown in figure 110 portray two photon-trigger events handled by the variable-load AQC. Starting from the bottom, the initial anode signal and its clamped counterpart (green and red, respectively) can be seen reaching the estimated value of 0.823V, which exceeds the 0.4V reference voltage and results in the comparator asserting (pink). The comparator going high eventually causes the ML gate voltage (dark green) to fall, turn off ML and quench the SPAD successfully, as indicated by the anode voltage rising up to the excess voltage of 1.9V. When ML's gate voltage rises again due to voltage Vai falling (grey), the anode voltage can be seen being pulled to ground. An important aspect of the timing to note is that there is about a 1.1ns delay between the moment the avalanche begins and the moment the digital photon-detection output signal (blue) goes high (the first output signal seen in the figure is from a preceding photon trigger). The waveform shown in figure 111 shows the time-gated operation of the circuit, where photons are only detected while signal WIN (orange signal on bottom) is high.

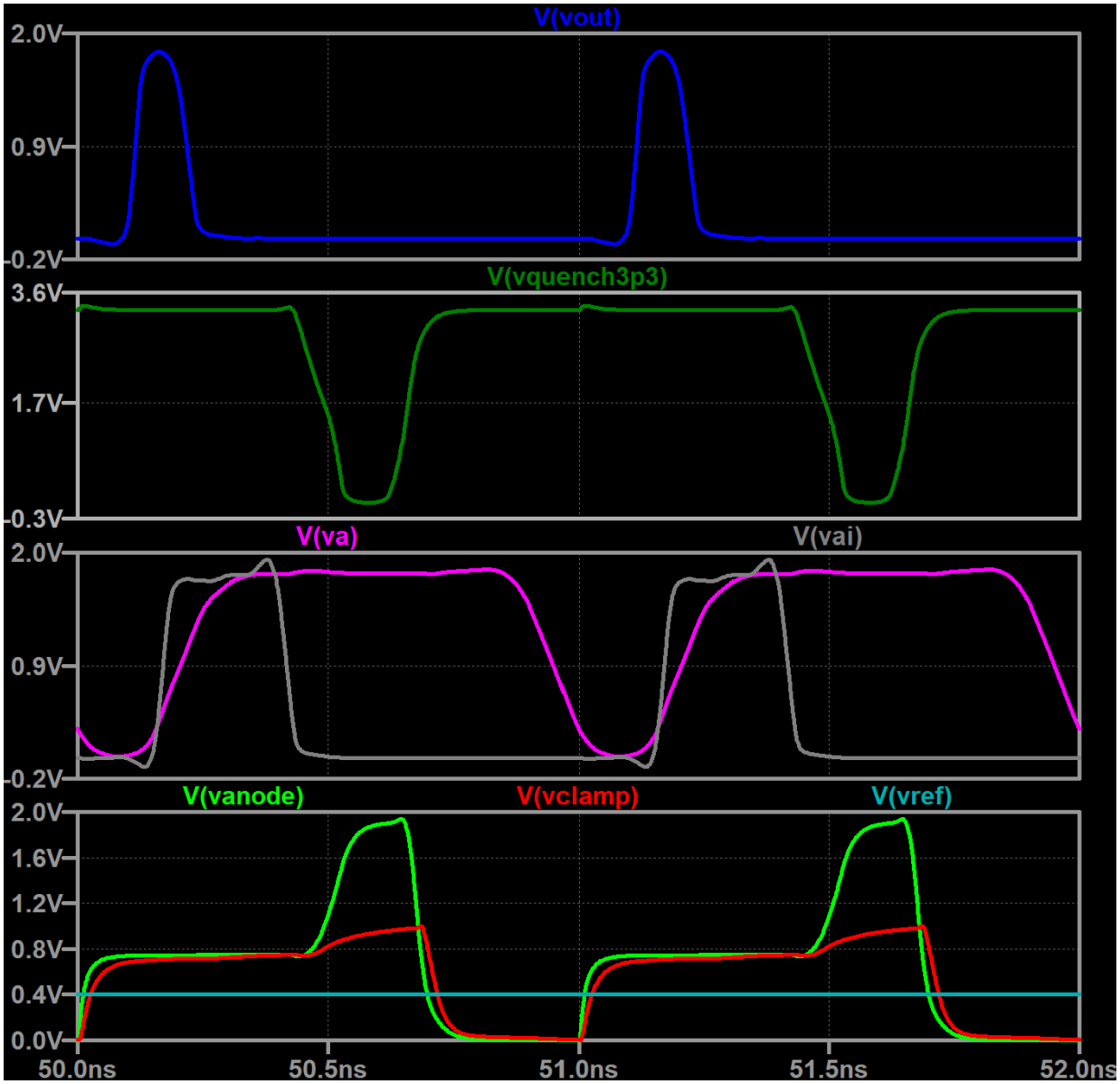


Figure 110: Quenching waveforms for variable-load AQC

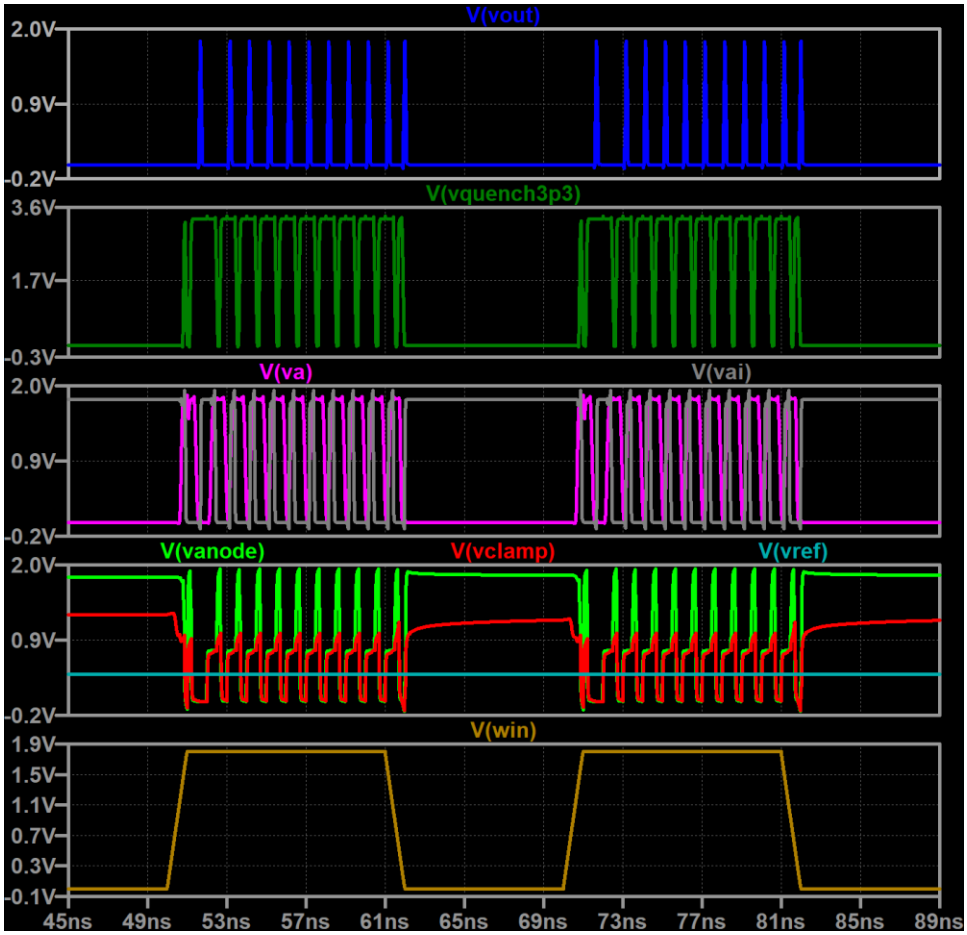


Figure 111: Time-gated operation of variable-load AQC

In order to test susceptibility to leakage currents, the SPAD was replaced with a simple current source outputting 1uA to observe the circuit response. Unsurprisingly, provided that the design's natural state has transistor ML fully enabled, the design saw no unwanted triggering due to the applied current, as all of it was successfully sourced to ground. Furthermore, operating the SPAD model with 1uA leakage included resulted in normal operation identical to figure 110.

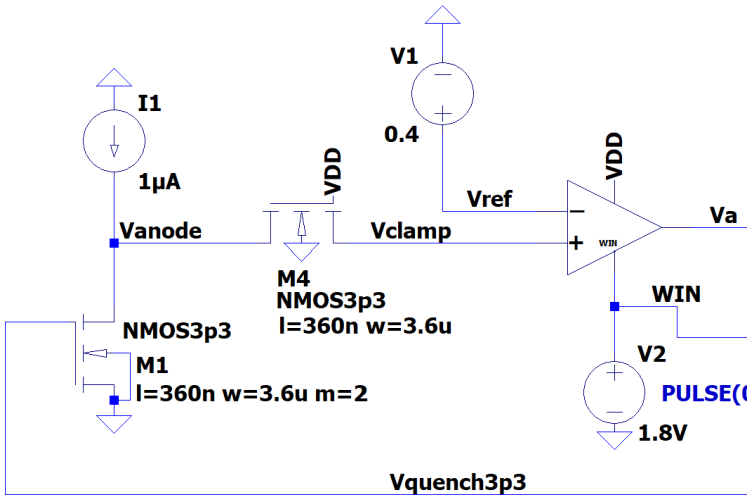


Figure 112: Schematic setup for testing leakage current on variable-load AQC

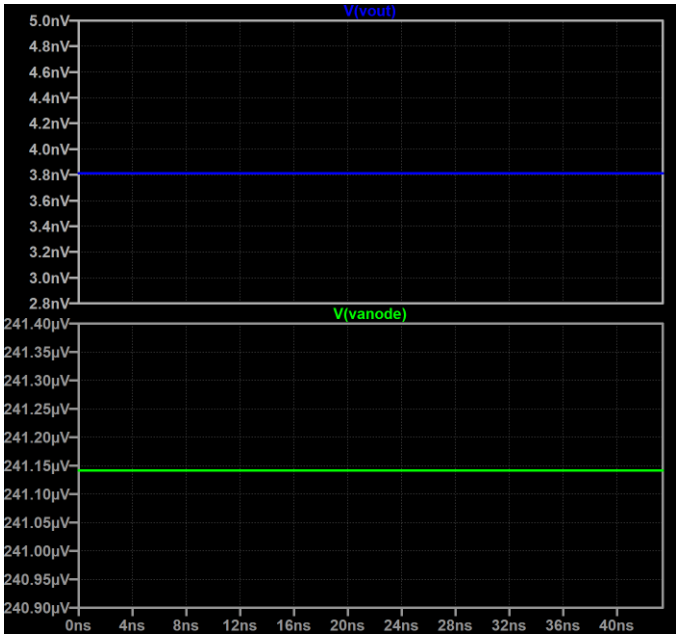


Figure 113: Variable-load AQC 1uA leakage current response showing non responsive anode voltage (bottom) and output signal (top)

Regarding the user-controlled voltage Vref, parametric analysis revealed that the quenching circuit responds best when Vref is in the range of 0.32-0.65V. 10mV beyond either of

those voltages results in the comparator failing to trigger and recognize the avalanche. Regardless of the bias within this range however, sub-nanosecond reset times are still achieved.

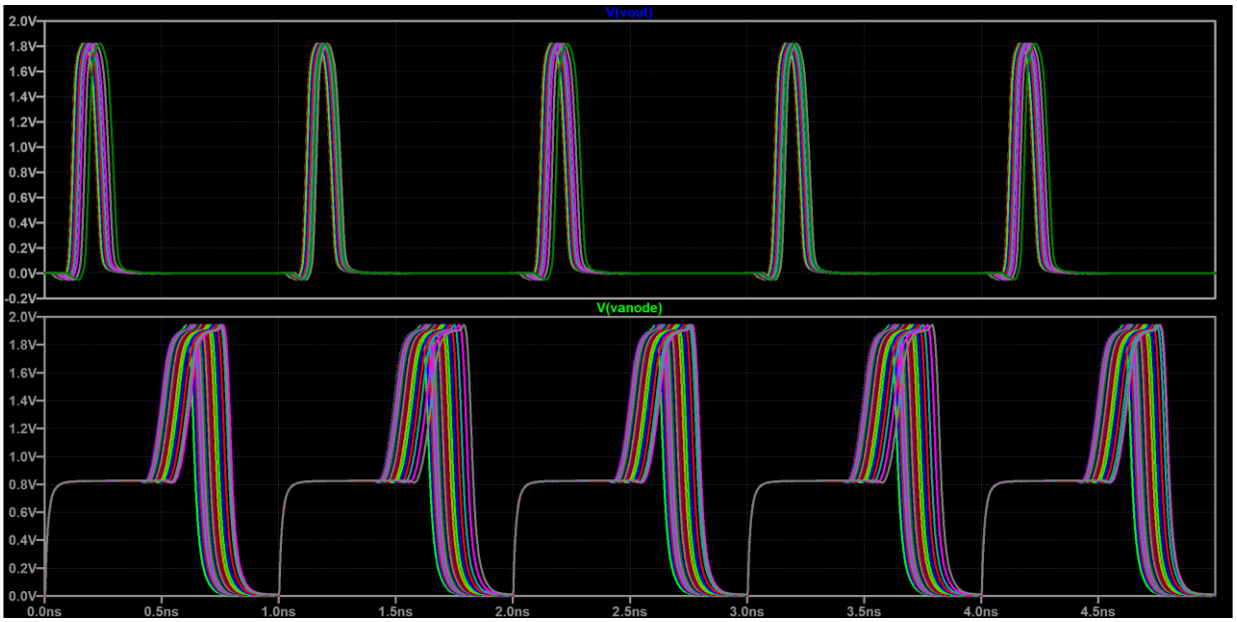


Figure 114: Parametric simulation showing normal quenching dynamics for Vref values of 0.32-0.65V (20mV steps)

For a more comprehensive system-level simulation, the analog counter was connected to the inverted photon-detection output signal. Figures 115 and 116 show the complete pixel's operation, where the quenching circuit is disabled via WIN whenever the analog counter needs to be reset.

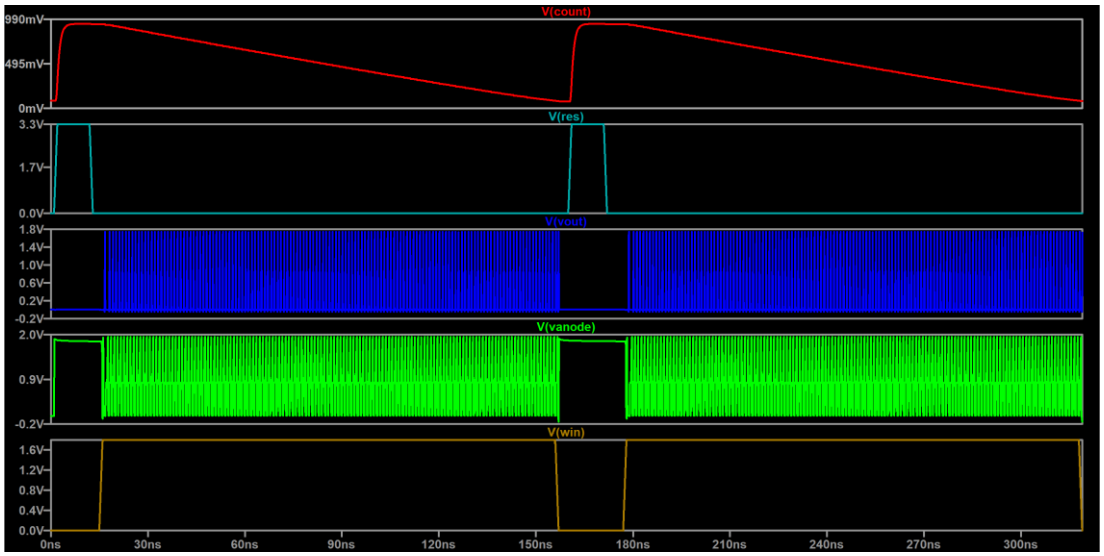


Figure 115: Complete variable-load AQC pixel simulation with analog counter

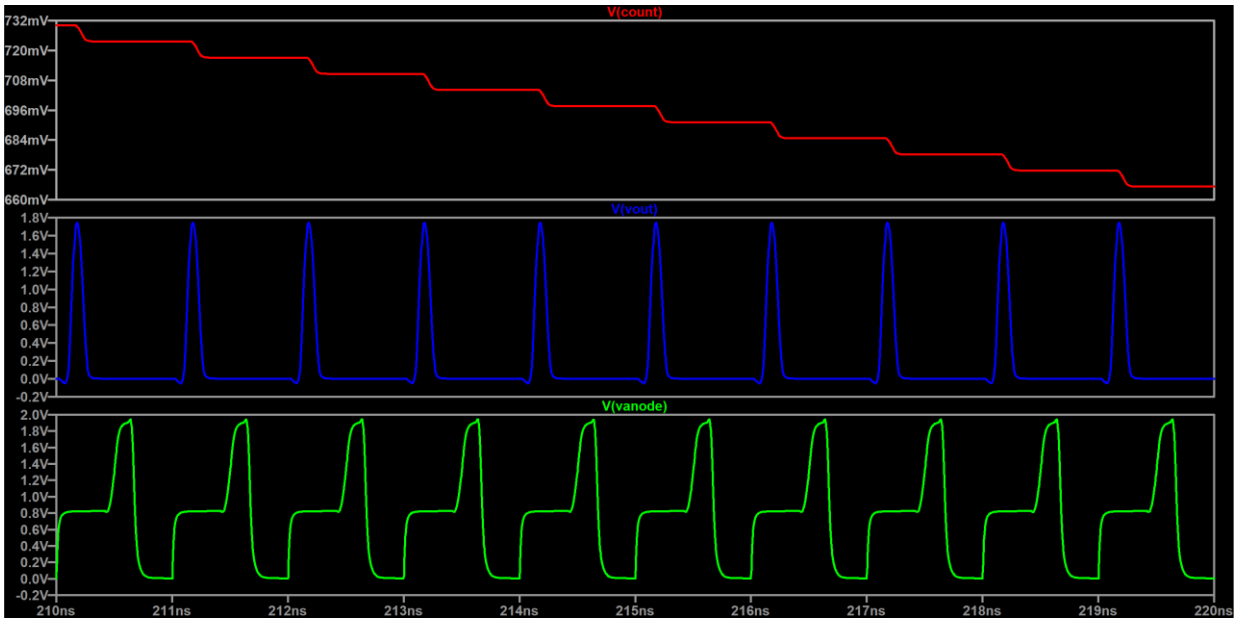


Figure 116: Zoomed system-level simulation of variable-load AQC showing anode voltage (green), photon-detection output signal (blue), and analog counter (red)

7.3 Latching Active Quenching Simulations

Figure 117 shows the entirety of the quenching and reset process over the course of two photon-trigger events. At first, the anode voltage (green) can be seen rising up to the excess voltage, 1.9V, as it is passively quenched by the resistive NMOS device, which causes the signal Vquench (red) and it's 3.3V buffered version (teal) to fall. This turns on the pull-up device, as can be evidenced by the anode waveform starting to rise to 3.3V. However, this pull-up period is short, because the gate voltage (pink) of the PMOS connected to Vquench falls not long after, pulling Vquench (and it's 3.3V duplicate) back up. At this point, it can be seen that both Vquench and Vquenchi (green) are high, which triggers the NAND gate and switches Vreset (grey) high. This begins the process of pulling the anode voltage down to ground. It is worth noting that Vstop is slow to rise up again after Vquench goes high. This is a result of the NMOS-starved inverter, which keeps M3 on for a longer period of time, preventing the high voltage of the anode from pulling Vquench back down. By the end of the SPAD recharging process, the slow inverter will have finally switched and caused Vstop to go completely high while Vquenchi and Vreset go low, thus resetting the circuit. One distinct advantage over the variable-load design that can be observed is an increase in the temporal accuracy of the digital photon-detection output signal, which appears almost three times closer to its corresponding avalanche event with a delay of only 400ps.

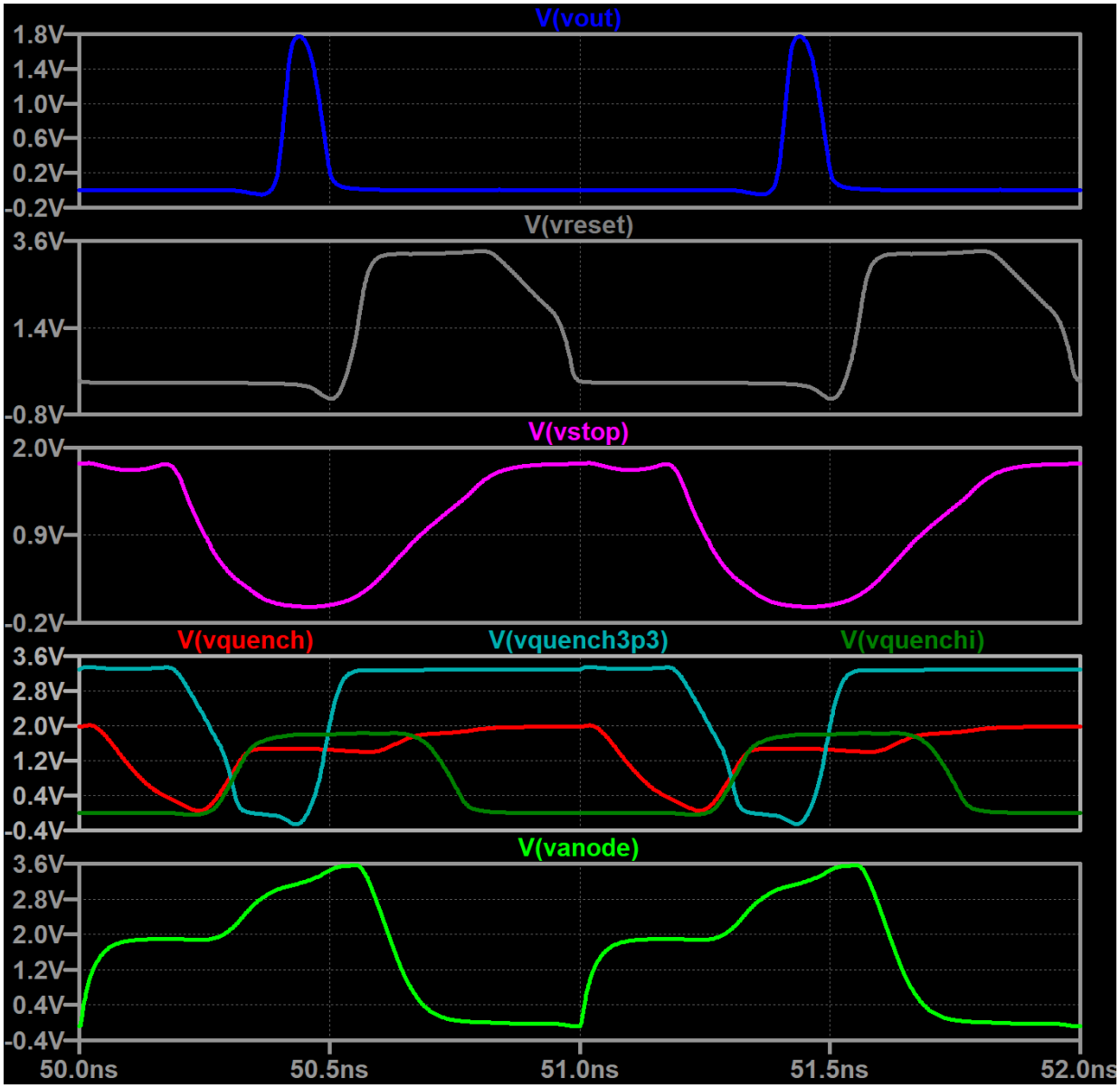


Figure 117: Quenching waveforms for latching AQC

The hardware implementation of the time-gating signal, WIN, is simpler in this design compared to the variable-load design and does not require any incorporated delays to avoid signal propagation conflicts. This is owed to the nature of the latch formed by M2 and MU, which if left alone without any interference from other devices, namely M3, is a static, stable

logic structure. Figure 118 shows the time-gated operation of the design using the WIN signal (orange signal on bottom) on the source of M3.

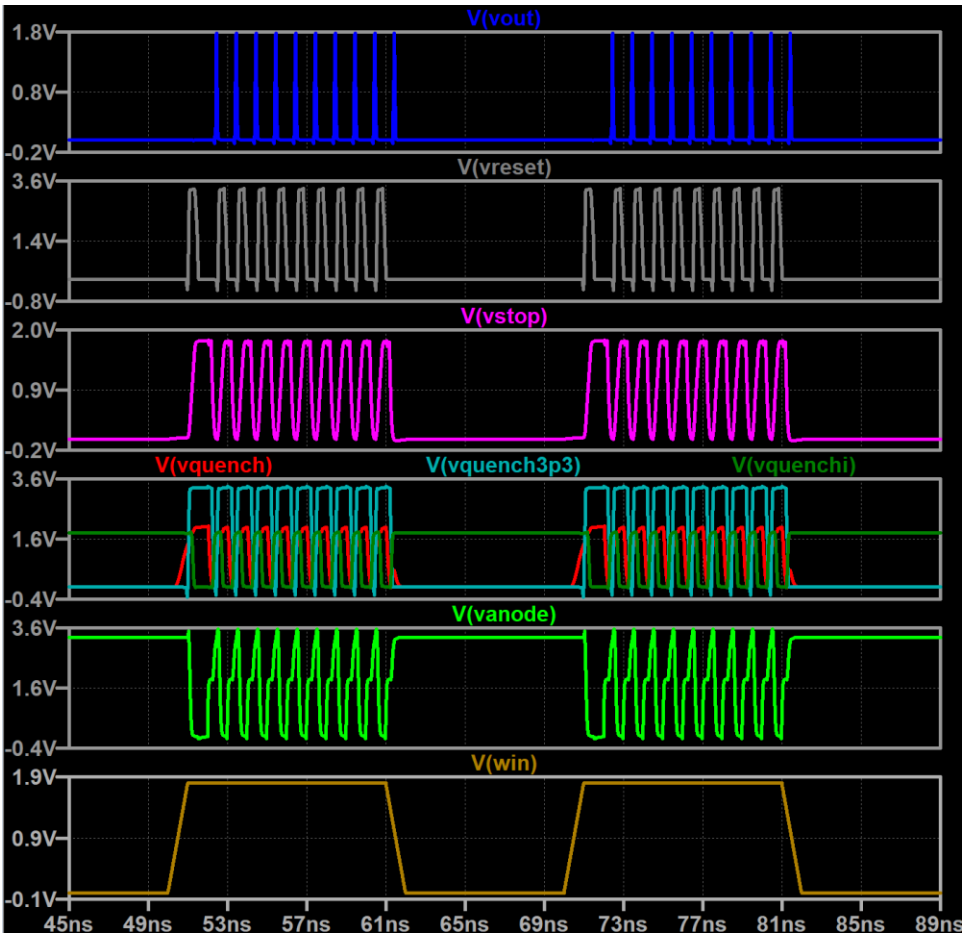


Figure 118: Time-gated operation of latching AQC

The same approach that was taken with the variable-load circuit to test susceptibility to leakage currents can also be used on the latching circuit, and as mentioned in section 6.2, bias voltages of 0.56V to 0.73V for NMOS M1 were deemed ideal. Running a parametric analysis using these values with a 1uA current source on the anode section of the circuit showed that the design is indeed protected against the leakage-current-induced oscillation issues encountered in

section 5.4. Simulation of the SPICE model with 1uA of leakage current also resulted in nominal operation identical to that seen in figure 117.

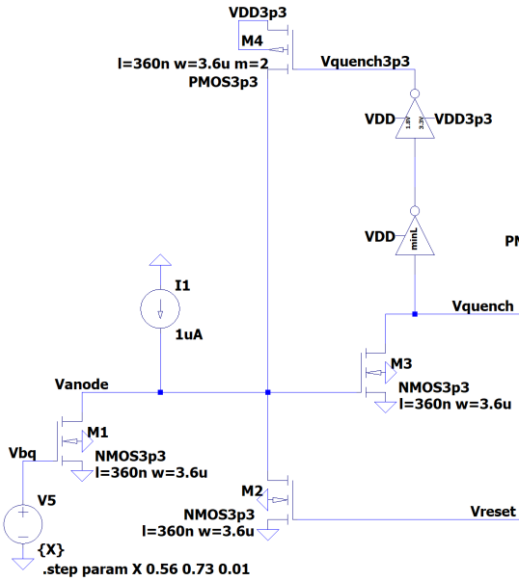


Figure 119: Schematic setup for testing leakage current on latching AQC

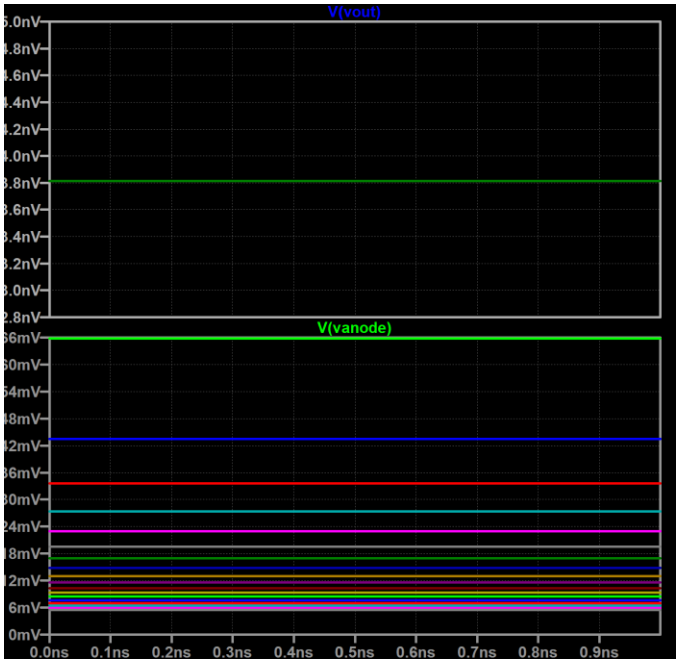


Figure 120: Latching AQC parametric 1uA leakage current response showing nonresponsive anode voltage (bottom) and output signal (top)

The drawback to this design is the extreme sensitivity to the user-controlled DC voltage Vinv. For the NMOS-starved inverter, parametric analysis revealed that the optimal range for the bias signal Vinv was between 0.82V and 0.90V. Applying voltages 10mV outside of this range causes the design to stray from the intended circuit behavior. Comparing the simulations from figures 121-123, it can be seen that the anode voltage waveform is affected for Vinv values that are too low while the Vquench voltage waveform is affected by Vinv values that are too high.

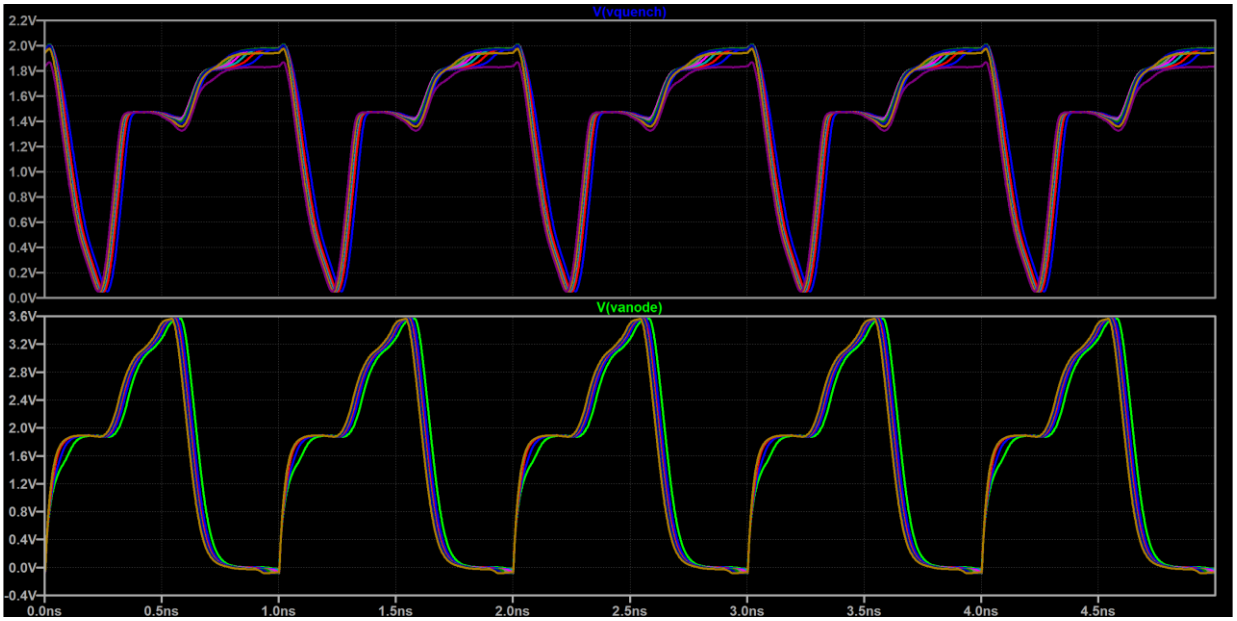


Figure 121: Parametric simulation showing normal quenching dynamics on Vanode (bottom) and Vquench (top) for Vinv values of 0.82-0.90V (10mV steps)

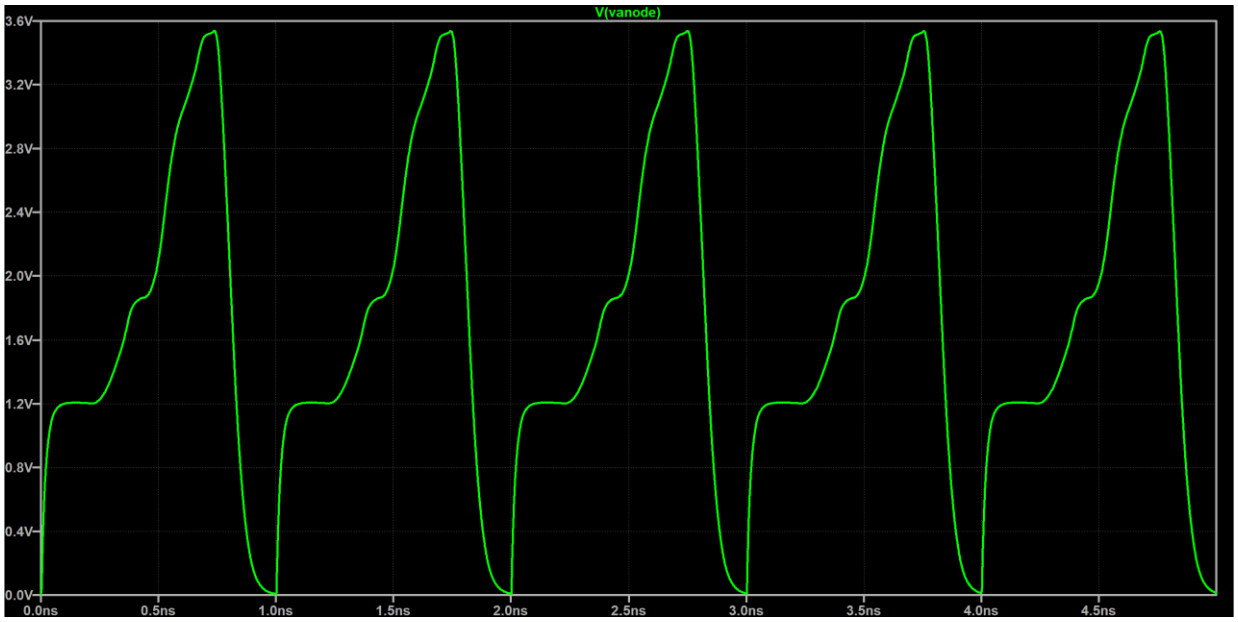


Figure 122: Abnormal quenching dynamics developed on Vanode due to Vinv being too low

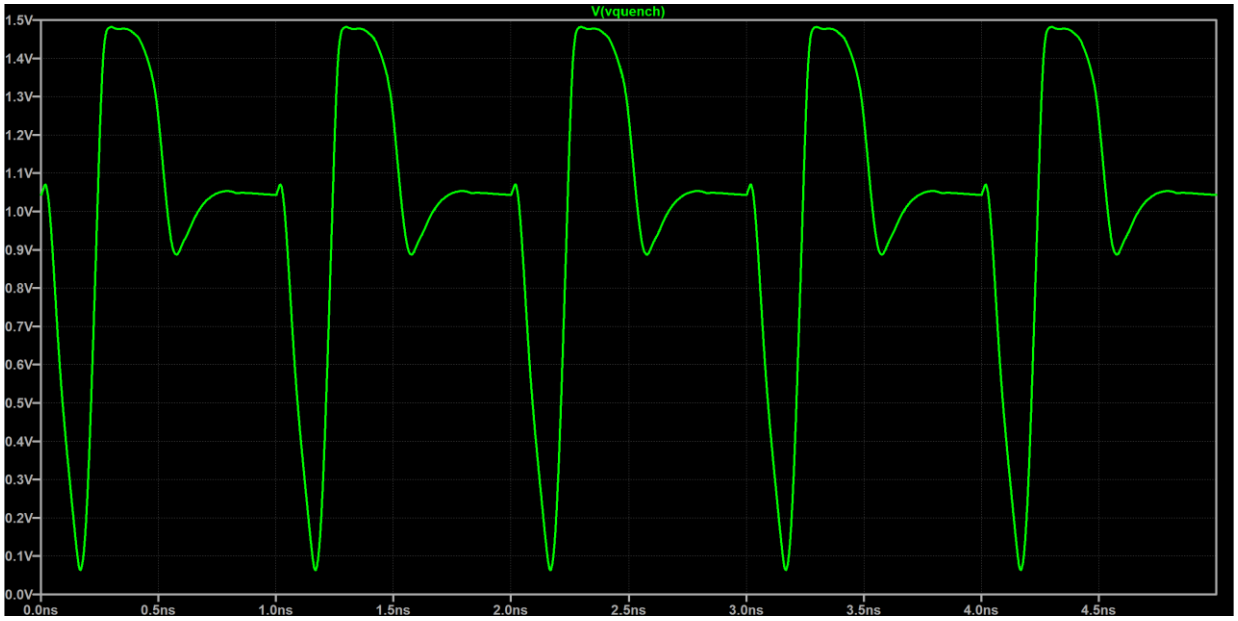


Figure 123: Abnormal quenching dynamics on Vquench due to Vinv being too high

Combining the latching AQC with the analog counter provides the system-level simulations shown in figures 124 and 125 using the same disable-reset-enable mode of operation used to simulate the variable-load AQC pixel.

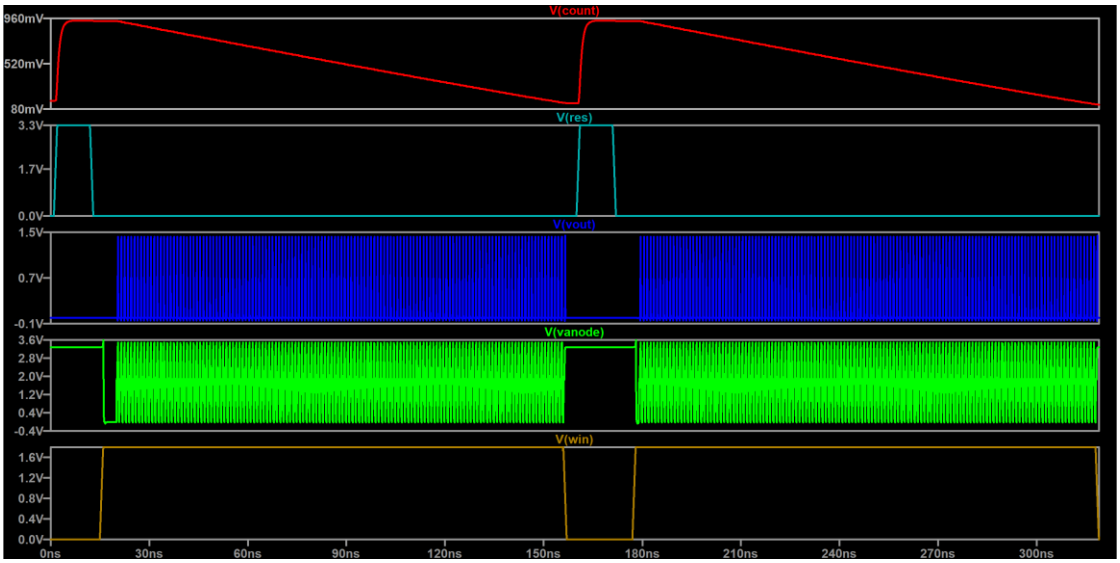


Figure 124: Complete latching AQC pixel simulation with analog counter

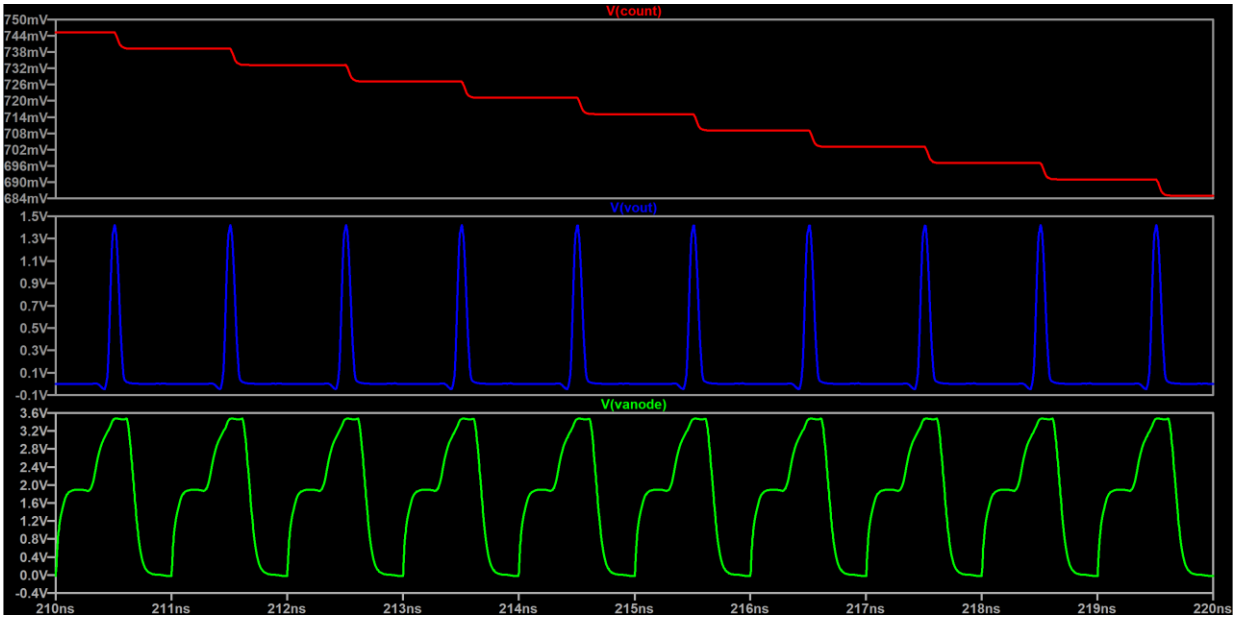


Figure 125: Zoomed system-level simulation of latching AQC showing anode voltage (green), photon-detection output signal (blue), and analog counter (red)

CHAPTER 8: ONGOING AND FUTURE WORK

8.1 Layout Progress

Similar to the AMS S35 process, the design of SiGe SPADs in TowerJazz's SBC18HA BiCMOS process involves the modification of traditional HBT NPN devices. In order to adhere to the design rules as much as possible, all of the necessary layers were laid out in a similar fashion to the NPN structures native to the PDK, with the only exceptions being the deletion of the emitter layers as well as the addition of blocking layers to prevent any metal, polysilicon, silicon, or passivation from covering the active photosensitive area of the SPAD. Staying true to the SPAD design that the active quenching circuits in this thesis were tailored for, a TowerJazz version of the AMS 5µm-by-5µm square SPAD was designed using Cadence and is shown in figure 127.

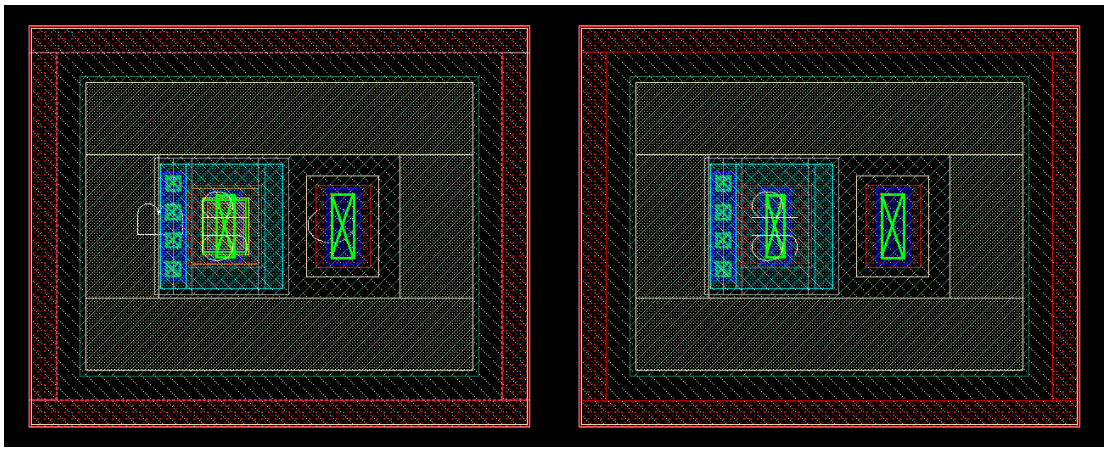


Figure 126: TowerJazz HBT NPN device before (left) and after (right) removal of emitter layers

Layer name(s)	Function
N_cell (draw)	Bipolar NPN marking layer
ablb (draw)	Analog block border
act (draw)	Active area layer
bpoly (draw)	Base poly layer
contact (draw)	Active and poly contacts to metal 1
csink (draw)	Collector sinker regions for connecting to buried N+ layers
dtrench (draw)	Deep trench isolation for NPNs
metal1 (draw)	First metal layer
metal1/2/3/4/5/6 (block)	Blocks the specified metal layers
nbur (draw)	Buried N+ layer for NPN collectors
nwell2 (draw)	Defines regions without field or well implants
poly (block)	Blocks any poly layers
sblk (draw)	Blocks silicide formation (used for poly resistors)
silox (draw)	Defines openings in the silicon-oxide passivation
slotct (draw)	Emitter poly and collector sinker contacts to metal 1 in NPNs
spacec (draw)	Spacer clear layer that defines where spacer dielectric is cleared to form NPN base

Table 13: TowerJazz layers used for 5µm-by-5µm no sub SPAD design

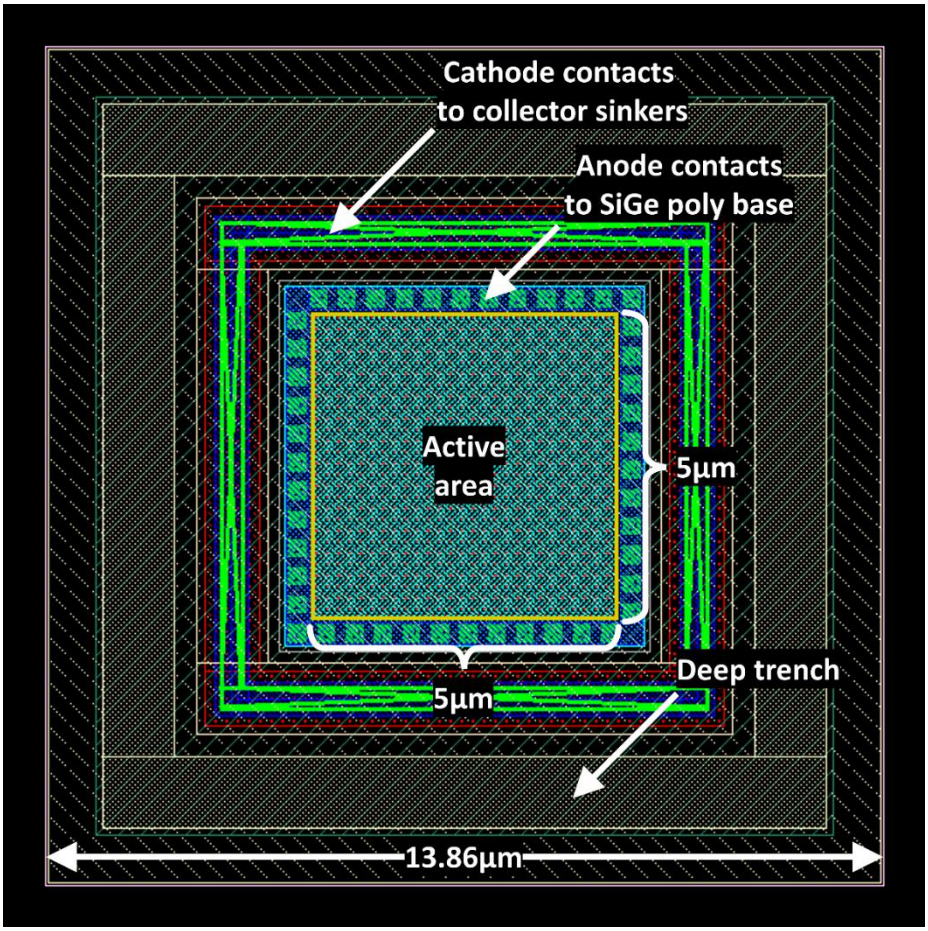


Figure 127: TowerJazz implementation of 5µm-by-5µm no sub SPAD

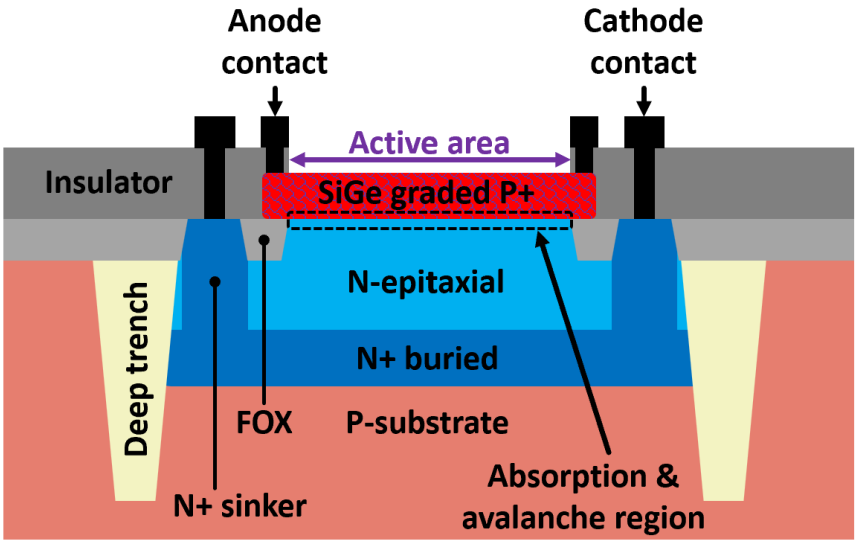


Figure 128: Cross-section of TowerJazz 5µm-by-5µm no sub SPAD

The resulting structure possesses a fill factor of $\frac{(5\mu m)^2}{(13.86\mu m)^2} \cdot 100\% \approx 13\%$, primarily due to the space taken up by the deep trench isolation layer, required NPN marking layer and analog blocking layer. With this SPAD layout, two pixel designs were developed for the variable-load and latching active quenching designs with both including the analog-counting electronics in-pixel. It is important to note that the layouts shown are only preliminary designs and the final products will likely be created using an alternative IC-design software (such as Silvaco) due to Cadence server licensing issues.

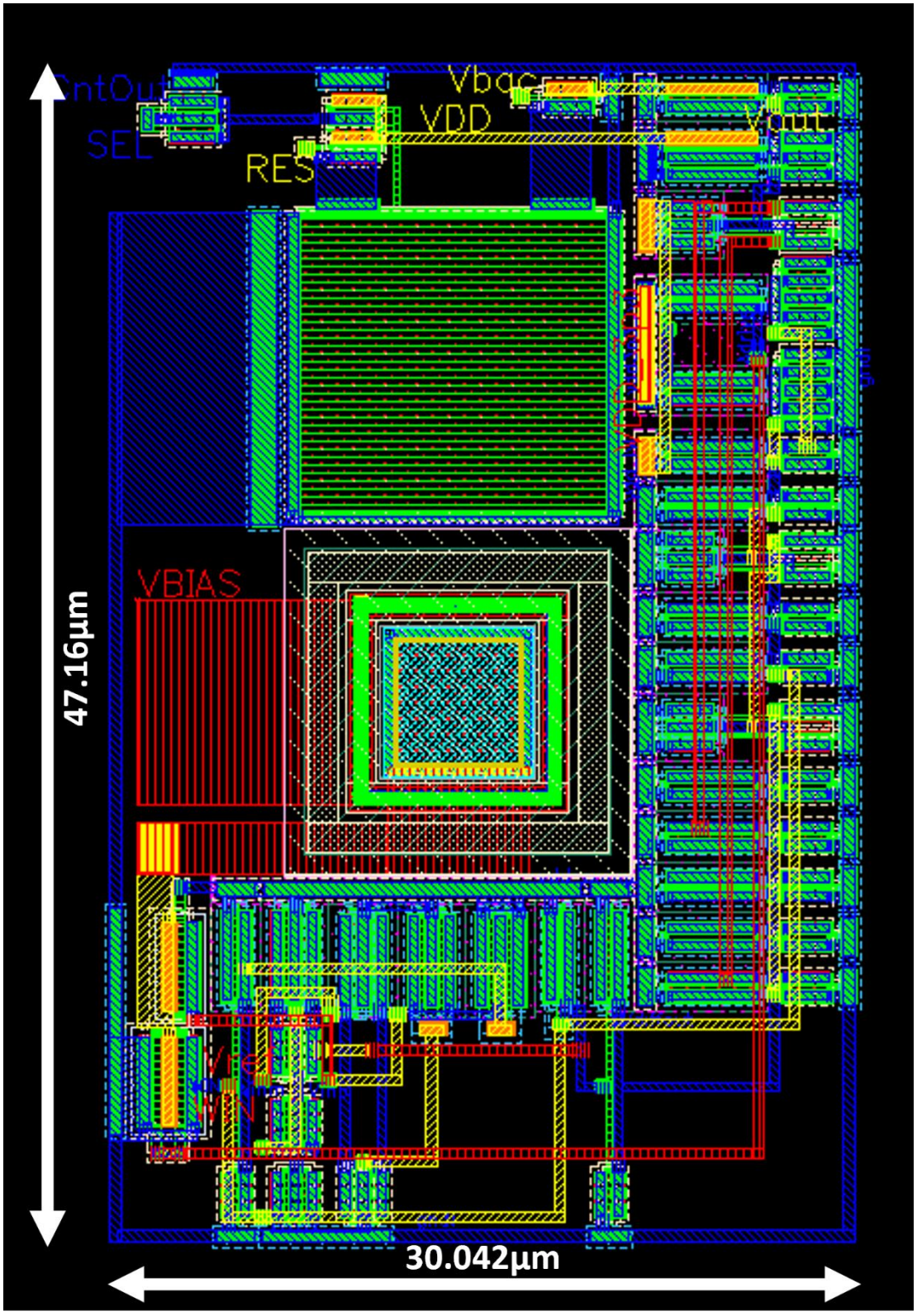


Figure 129: Variable-load active quenching pixel layout

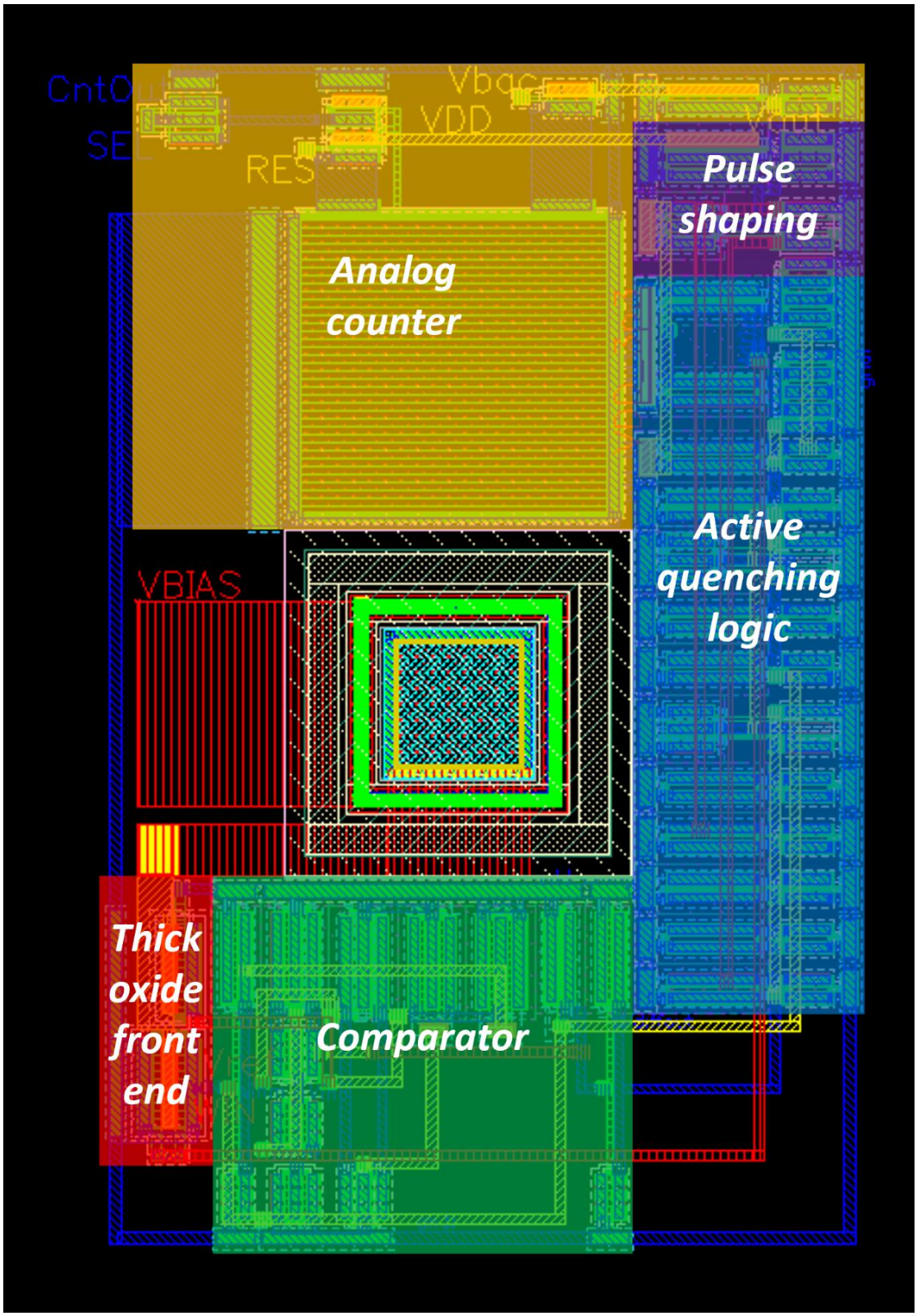


Figure 130: Sectional labeling of variable-load active quenching pixel

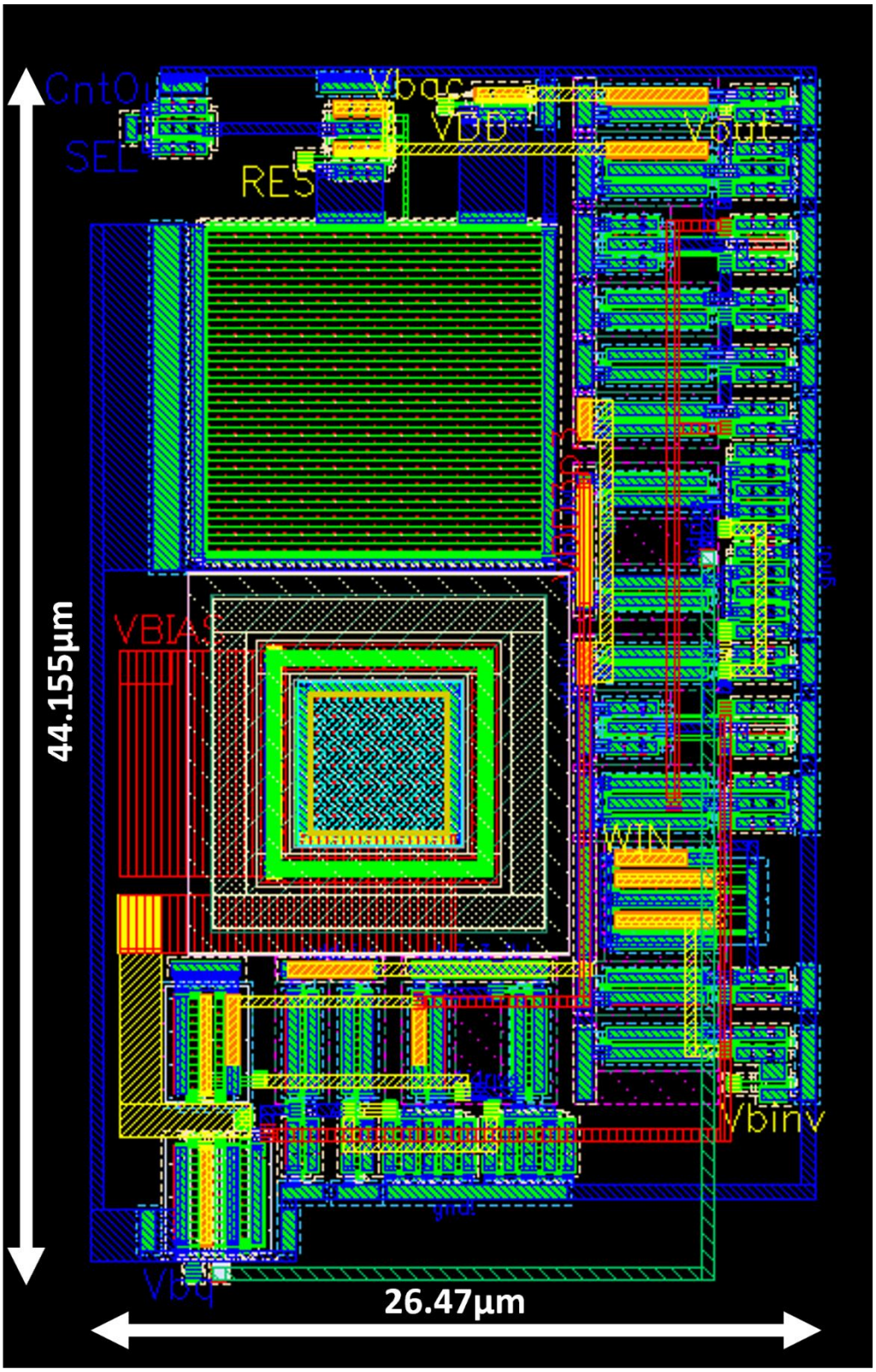


Figure 131: Latching active quenching pixel layout

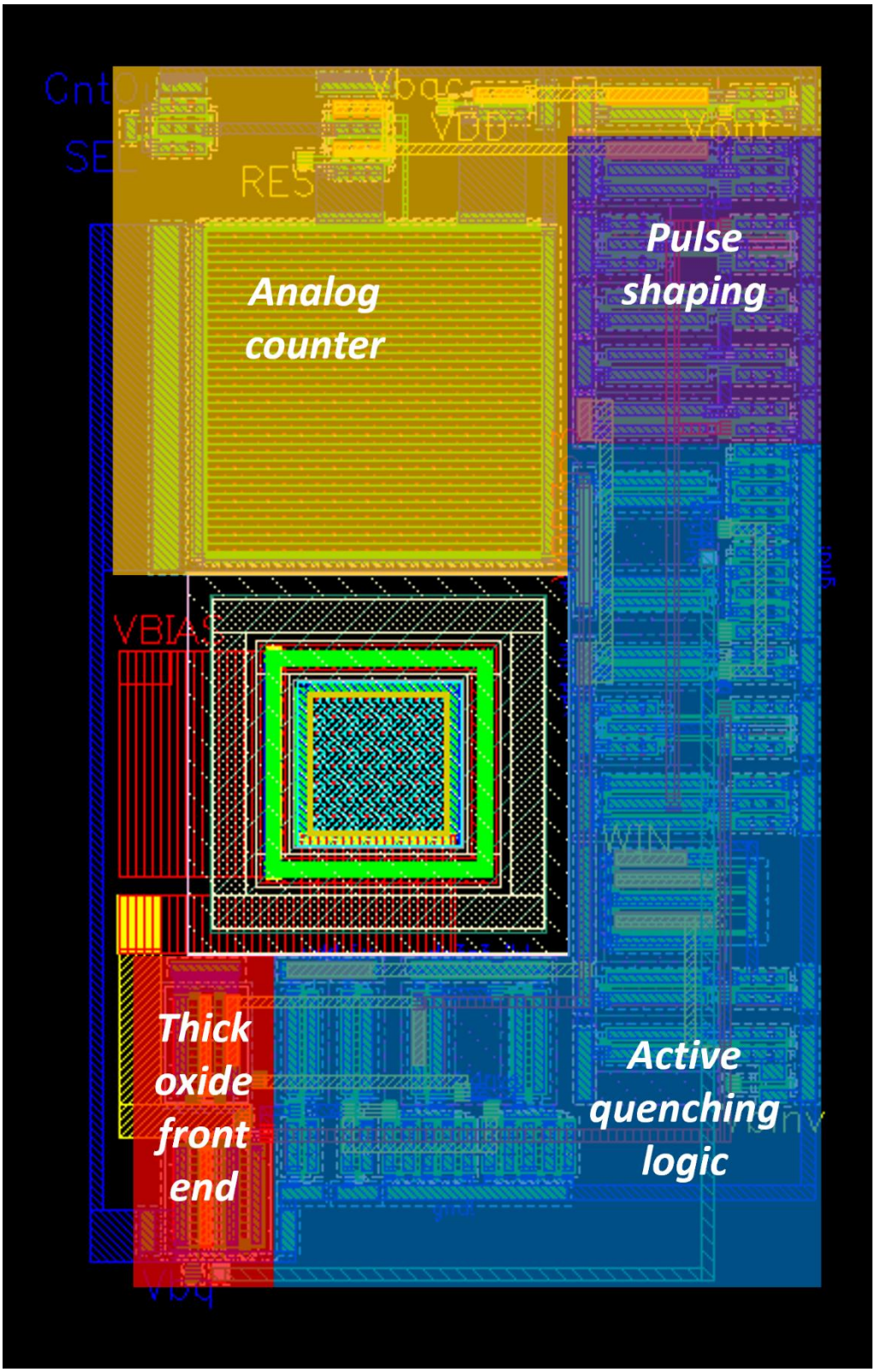


Figure 132: Sectional labeling of latching active quenching pixel

The fill factors of the pixel designs can be calculated using the formula:

$$\mathrm{FF} = \frac{\text{Active area}}{\text{Total pixel area}}$$

$$\mathrm{FF}_{\text{variable\_load}} = \frac{25\mu\mathrm{m}^2}{47.16\mu\mathrm{m} \cdot 30.042\mu\mathrm{m}} \times 100\% \approx 1.76\%$$

$$\mathrm{FF}_{\text{latching}} = \frac{25\mu\mathrm{m}^2}{44.155\mu\mathrm{m} \cdot 26.47\mu\mathrm{m}} \times 100\% \approx 2.14\%$$

Considering the relatively small size of the SPAD and the fact that the designs integrate both active quenching and on-pixel processing, fill factors of these quantities are not unreasonable.

8.2 Future Work

With two designs having been developed, simulated and characterized in LTspice (a choice mainly influenced by the simulation speeds LTspice offers), work in the near future may involve developing a Cadence compatible SPAD SPICE model to further simulate the designs in the actual TowerJazz 180nm BiCMOS process they will be incorporated in. Furthermore, in addition to finalizing the individual pixel layouts using a different IC-design software, the actual photon-counting SPAD array configuration will also need to be designed. As of the writing of this thesis, the current plan is to incorporate various 4-by-4 pixel arrays with each array using a different pixel type for the purpose of enabling easy comparison between various quenching techniques. Other approaches to performing in-pixel or off-pixel counting and read-out may also be investigated. If there is a need, SPAD structures that exhibited speeds close to that of SPAD

2H may be characterized and modeled as well to simulate how the quenching designs respond to different device parameters.

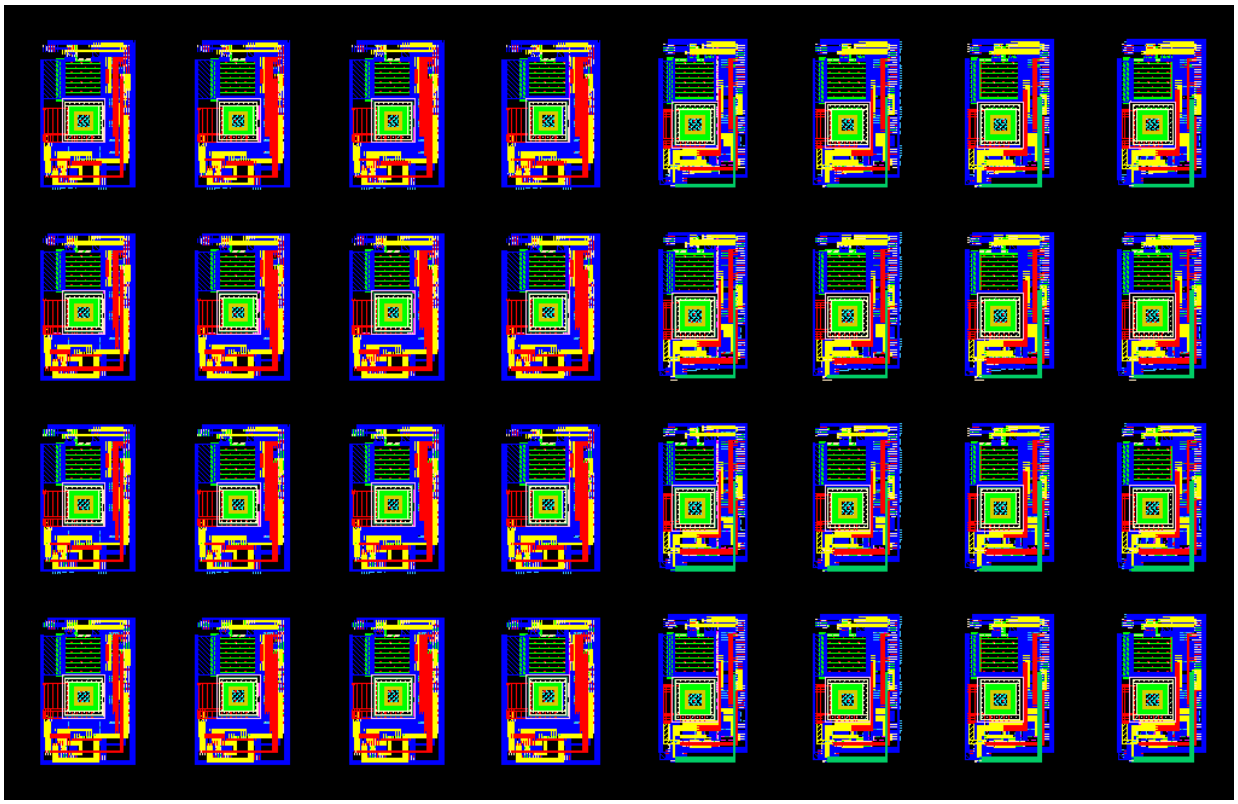


Figure 133: 4-by-4 arrays of variable-load AQC pixels (left) and latching AQC pixels (right)

CHAPTER 9: CONCLUSION

Single-photon avalanche diodes are devices that are as versatile as they are unpredictable. Provided their stochastic nature of operation, special quenching and read-out techniques must be applied to take full advantage of their single-photon-resolving capabilities. Their small form factor, scalability, and durability have made them a technology of interest for use in prompt gamma/neutron experiments, and their potential to serve as a substitute for traditional photomultiplier tubes is an ongoing study.

Building off of previous research efforts, the work outlined in this thesis has provided insight regarding the SPAD structure that yielded the fastest transient performance in a SiGe BiCMOS process and how it can be utilized in new pixel designs for time-gated photon counting. With the information gathered from current mode tests conducted on the fastest structure of interest, a behavioral SiGe SPAD SPICE model suitable for simulation was developed and used to guide the design of two active quenching circuit designs with differing modes of operation that both satisfy the metrics needed for the intended physics application. The variable-load active quenching design boasts stable operation across a wider range of user-controlled input voltages while the latching active quenching design offers the benefit of more intense quenching that can reduce after-pulsing effects within the SPAD. Both designs are capable of achieving sub-nanosecond reset times while providing digital photon-detection output signals with FWHM pulses 70-100ps wide. With the designs drafted and preliminary layouts made, future work will focus on finalizing the designs using TowerJazz's 180nm SiGe BiCMOS process and developing the pixel array configurations for the final photon-counting ASIC design.

APPENDIX A: SIGE SPAD BATCH TESTING DATA

Phase One Data (Original Quenching Resistor Values)

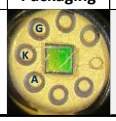
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
1	3	3E	24µ TUBBUR		930.884 ps	740.510 ps	772.778 ps	3.92 mV	x	150k

Table 14: SPAD 3E (board 1) phase 1 results

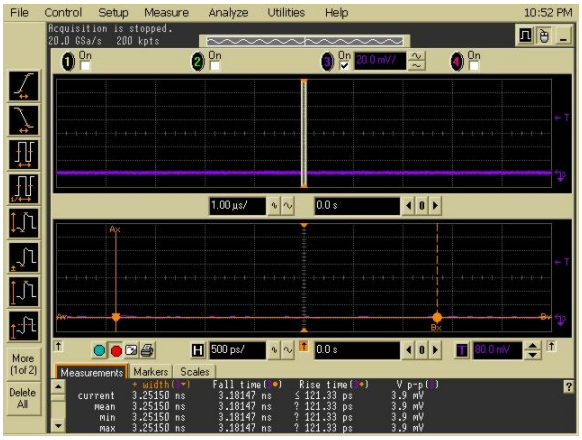


Figure 134: SPAD 3E (board 1) phase 1 waveform

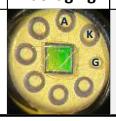
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
1	3	3J	24µ Striped BUR Half TUB		723.901 ps	889.319 ps	730.699 ps	3.88 mV	x	150k

Table 15: SPAD 3J (board 1) phase 1 results

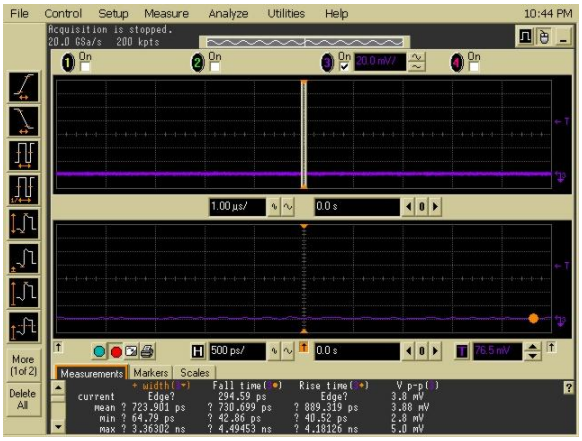


Figure 135: SPAD 3J (board 1) phase 1 waveform

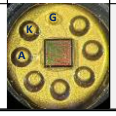
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
2	3	3U	50µ Striped TUBBUR		918.163 ps	627.035 ps	616.196 ps	4.13 mV	x	150k

Table 16: SPAD 3U (board 2) phase 1 results

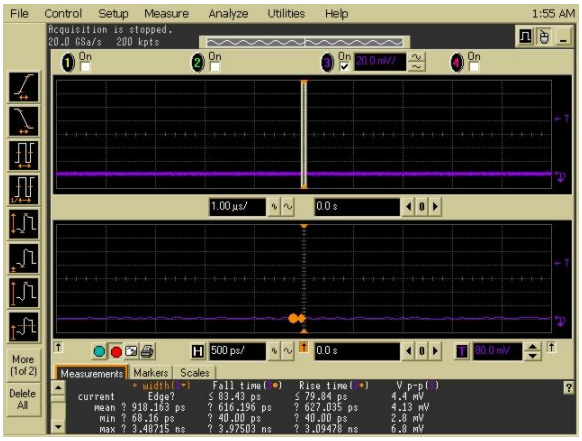


Figure 136: SPAD 3U (board 2) phase 1 waveform

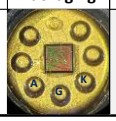
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
2	3	Cathode and ground of 3H but anode of 3I	Not discernable		879.606 ps	765.945 ps	665.187 ps	3.99 mV	x	150k

Table 17: SPAD 3H/I (board 2) phase 1 results

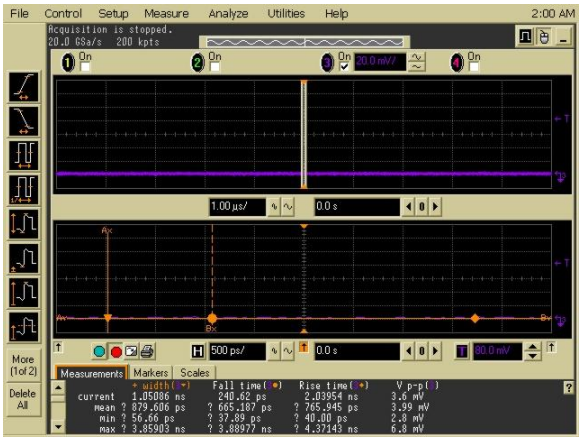


Figure 137: SPAD 3H/I (board 2) phase 1 waveform

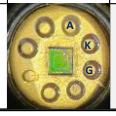
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
3	2	2B	24µ Elementary		387.043 ps	121.358 ps	634.176 ps	106.62 mV	✓	231k

Table 18: SPAD 2B (board 3) phase 1 results

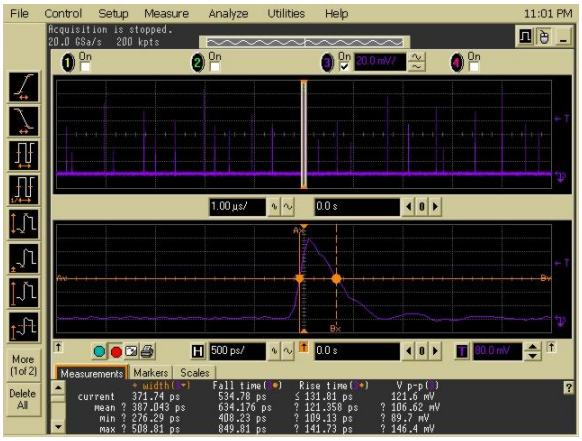


Figure 138: SPAD 2B (board 3) phase 1 waveform

Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
3	2	2K	24µ Standard		248.374 ps	123.388 ps	370.017 ps	124.09 mV	✓	153k

Table 19: SPAD 2K (board 3) phase 1 results

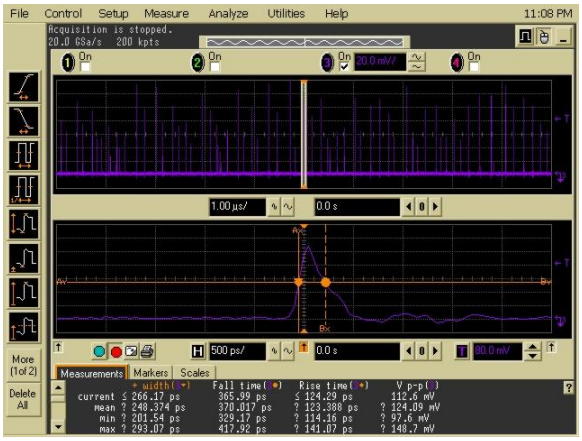


Figure 139: SPAD 2K (board 3) phase 1 waveform

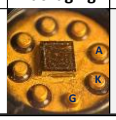
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
4	3	3G	24µ noBNTUB2		992.666 ps	710.555 ps	587.115 ps	3.99 mV	x	150k

Table 20: SPAD 3G (board 4) phase 1 results

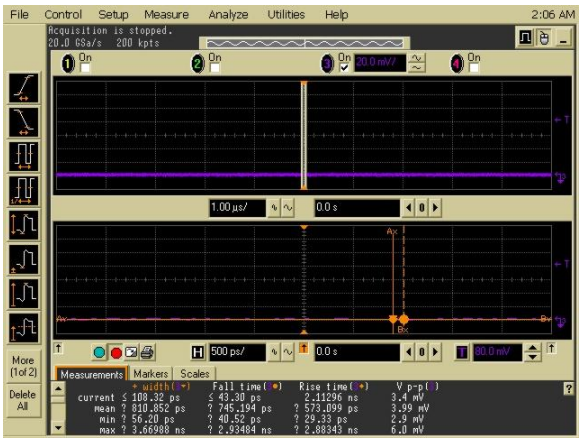


Figure 140: SPAD 3G (board 4) phase 1 waveform

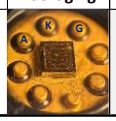
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
4	3	3B	5µ TUB		787.358 ps	636.978 ps	674.027 ps	4.02 mV	x	150k

Table 21: SPAD 3B (board 4) phase 1 results

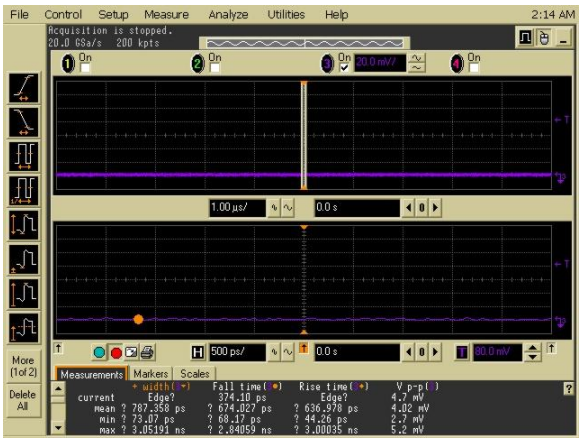


Figure 141: SPAD 3B (board 4) phase 1 waveform

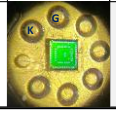
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
5	2	2F	5µ BPOLY/PPLUS		660.088 ps	746.709 ps	665.278ps	3.97 mV	x	153k

Table 22: SPAD 2F (board 5) phase 1 results

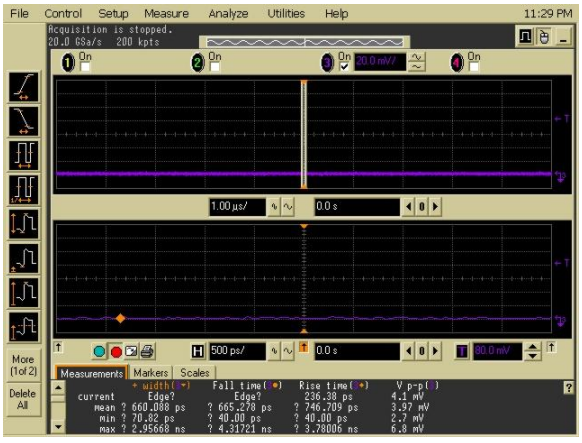


Figure 142: SPAD 2F (board 5) phase 1 waveform

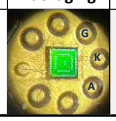
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
5	2	2A, but non-standard ground pin is used (40)	5µ Elementary		883.952 ps	749.439 ps	737.212 ps	3.91 mV	x	153k

Table 23: SPAD 2A (board 5) phase 1 results

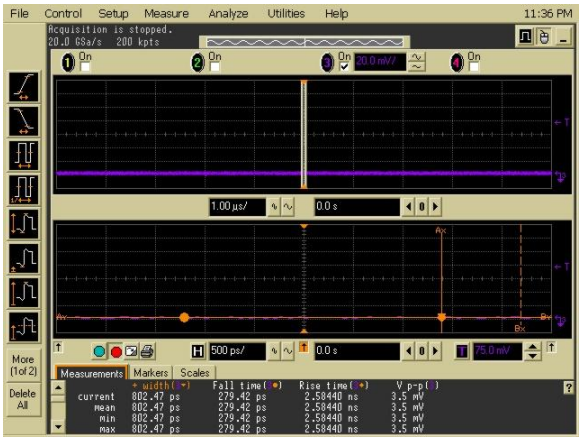


Figure 143: SPAD 2A (board 5) phase 1 waveform

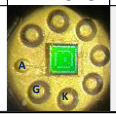
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
5	2	Cathode and ground of 2I and anode of 2J	Not discernible		840.495 ps	706.078 ps	646.406 ps	3.955 mV	x	153k

Table 24: SPAD 2I/J (board 5) phase 1 results

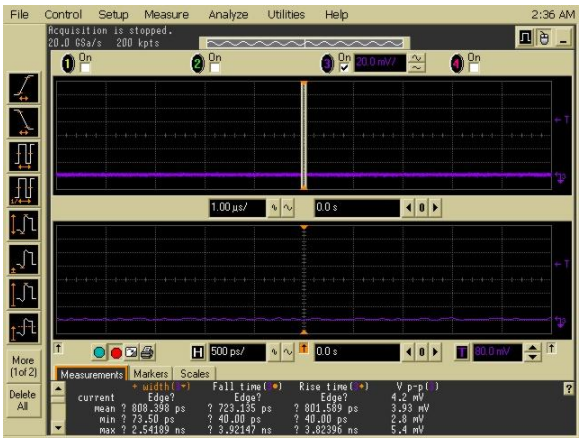


Figure 144: SPAD 2I/J (board 5) phase 1 waveform

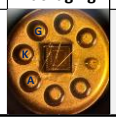
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
6	3	3E	24µ TUBBUR		888.932 ps	692.731 ps	680.505 ps	3.96 mV	x	50

Table 25: SPAD 3E (board 6) phase 1 results

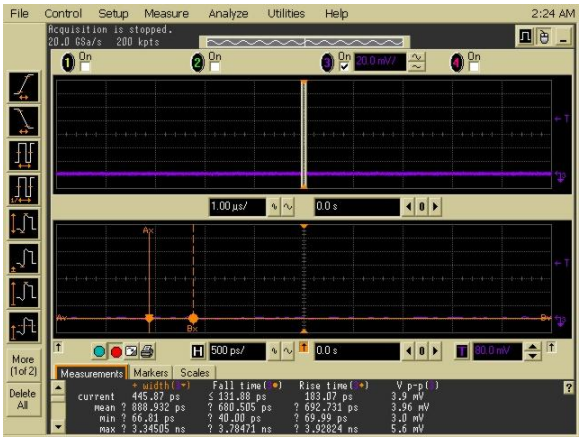


Figure 145: SPAD 3E (board 6) phase 1 waveform

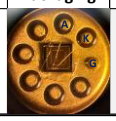
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
6	3	3J	24µ Striped BUR Half TUB		859.966 ps	711.671 ps	700.408	4.1 mV	x	150k

Table 26: SPAD 3J (board 6) phase 1 results

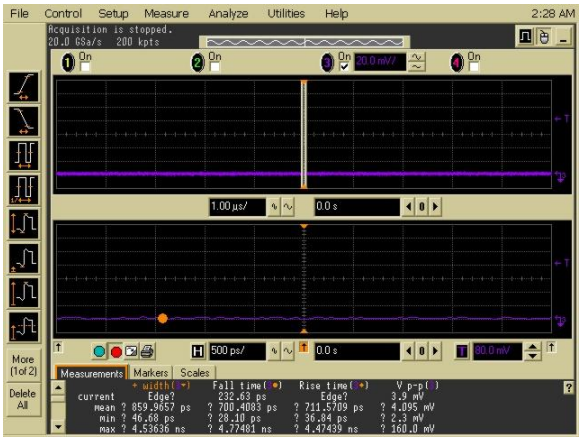


Figure 146: SPAD 3J (board 6) phase 1 waveform

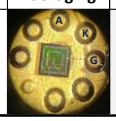
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
7	3	3Q	50µ noBNTUB2		238.453 ps	132.963 ps	244.656 ps	106.16 mV	✓	153k

Table 27: SPAD 3Q (board 7) phase 1 results

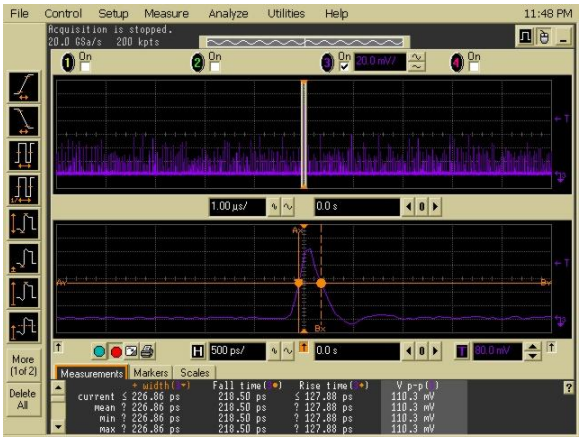


Figure 147: SPAD 3Q (board 7) phase 1 waveform

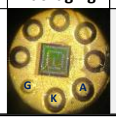
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
7	3	3R	50µ Striped BNTUB2		434.301 ps	165.018 ps	840.922 ps	100.82 mV	✓	154k

Table 28: SPAD 3R (board 7) phase 1 results

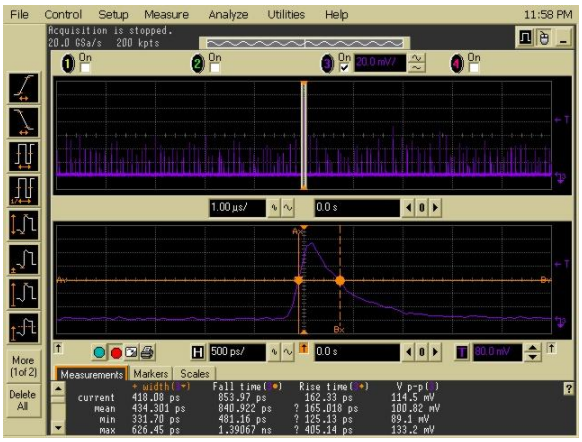


Figure 148: SPAD 3R (board 7) phase 1 waveform

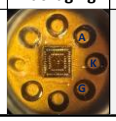
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
9	2	2D	5µ Standard		312.717 ps	116.750 ps	252.465 ps	140.27 mV	✓	153k

Table 29: SPAD 2D (board 9) phase 1 results

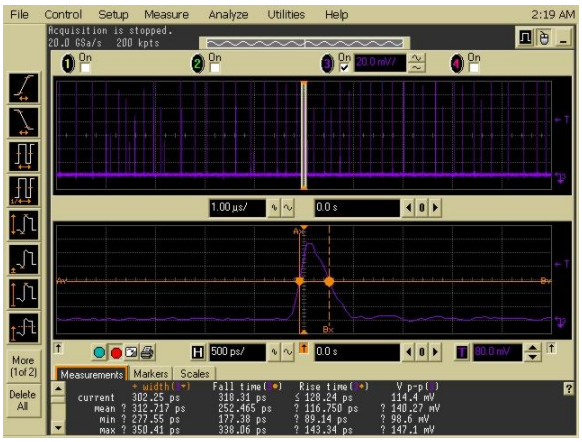


Figure 149: SPAD 2D (board 9) phase 1 waveform

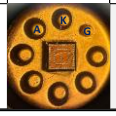
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
10	3	3F	24µ TUB		406.336 ps	134.847 ps	487.581 ps	103.65 mV	✓	150k

Table 30: SPAD 3F (board 10) phase 1 results

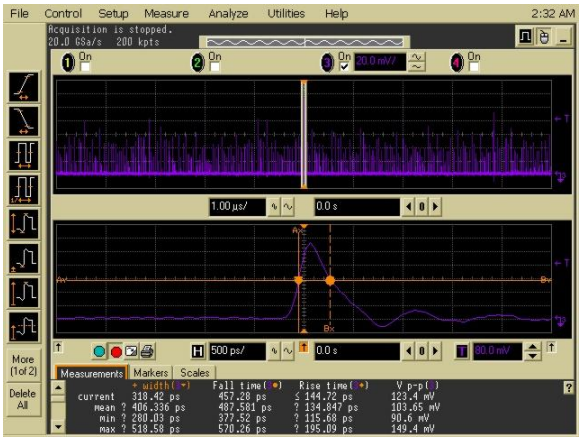


Figure 150: SPAD 3F (board 10) phase 1 waveform

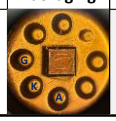
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
10	3	3A	5µ TUBBUR		808.398 ps	801.589 ps	723.135 ps	3.93 mV	x	150k

Table 31: SPAD 3A (board 10) phase 1 results

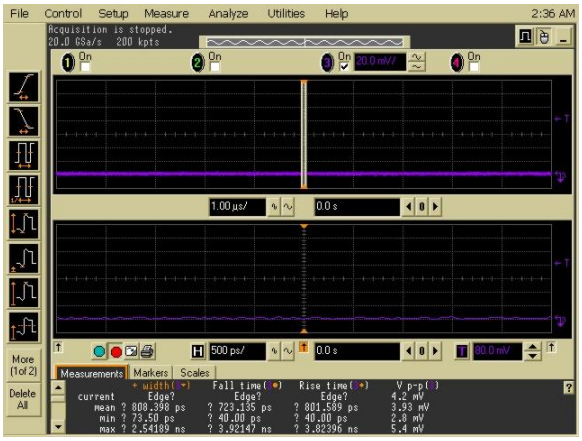


Figure 151: SPAD 3A (board 10) phase 1 waveform

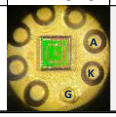
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
11	2	2I	5µ Circle		318.022 ps	104.367 ps	290.843 ps	158.815 mV	✓	153k

Table 32: SPAD 2I (board 11) phase 1 results

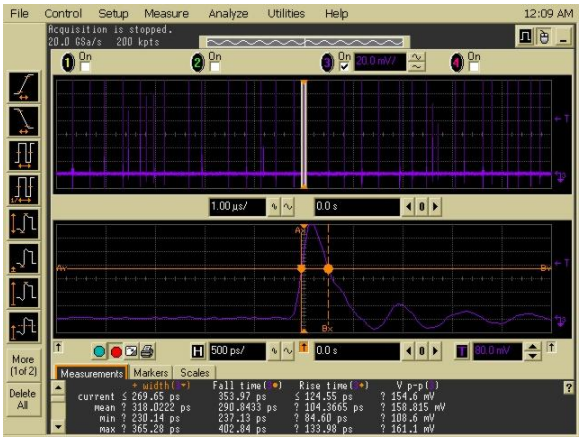


Figure 152: SPAD 2I (board 11) phase 1 waveform

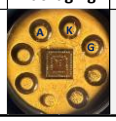
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
12	2	2P	24µ Circle		316.020 ps	124.191 ps	332.823 ps	137.990 mV	✓	157k

Table 33: SPAD 2P (board 12) phase 1 results

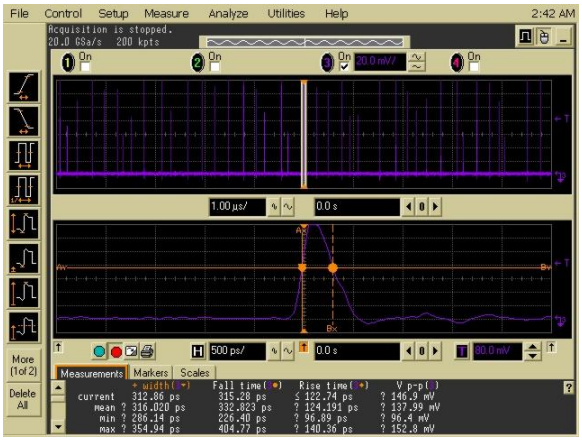


Figure 153: SPAD 2P (board 12) phase 1 waveform

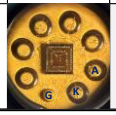
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
12	2	2W	50µ Circle		272.209 ps	133.637 ps	413.352 ps	131.47 mV	✓	158k

Table 34: SPAD 2W (board 12) phase 1 results

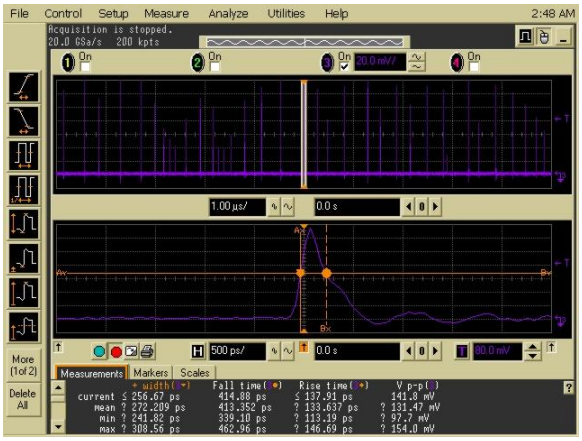


Figure 154: SPAD 2W (board 12) phase 1 waveform

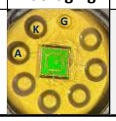
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
13	2	2R	50µ Standard		255.383 ps	132.159 ps	372.016 ps	115.046 mV	✓	158k

Table 35: SPAD 2R (board 13) phase 1 results

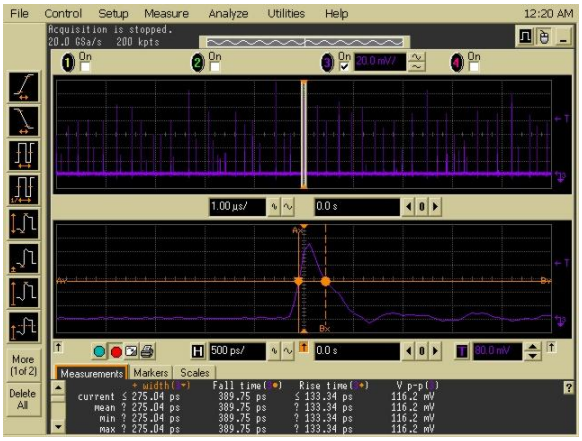


Figure 155: SPAD 2R (board 13) phase 1 waveform

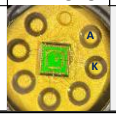
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
13	2	2X	50µ Circle No Sub		372.323 ps	156.985 ps	581.140 ps	137.23 mV	✓	157k

Table 36: SPAD 2X (board 13) phase 1 results

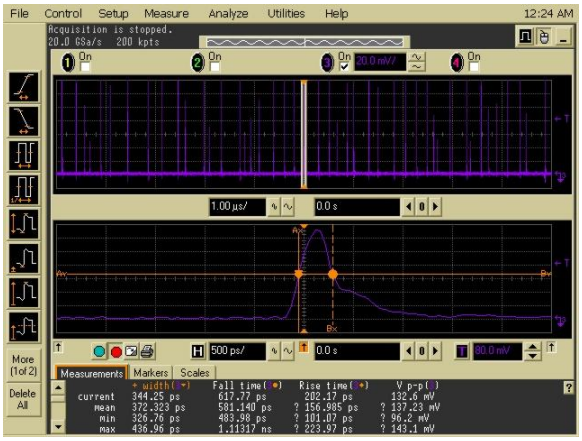


Figure 156: SPAD 2X (board 13) phase 1 waveform

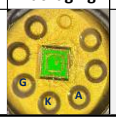
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
13	2	2U	50µ No EMITT		820.849 ps	655.906 ps	733.219 ps	4.04 mV	x	158k

Table 37: SPAD 2U (board 13) phase 1 results

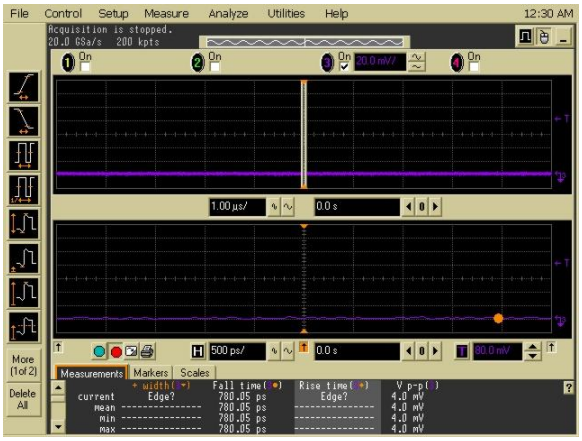


Figure 157: SPAD 2U (board 13) phase 1 waveform

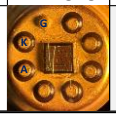
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
14	3	3I	24µ Striped BUR hTUB		882.208 ps	694.977 ps	701.196 ps	4.02 mV	x	150k

Table 38: SPAD 3I (board 14) phase 1 results

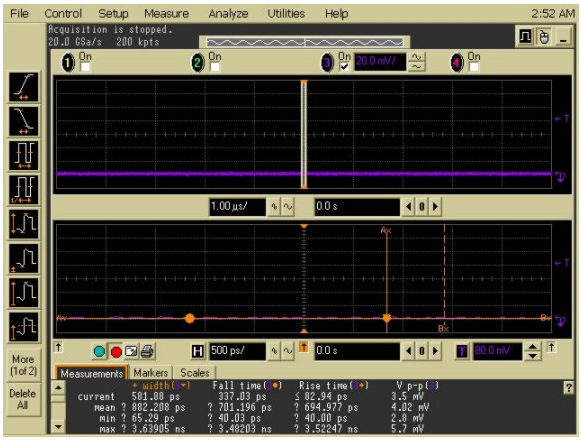


Figure 158: SPAD 3I (board 14) phase 1 waveform

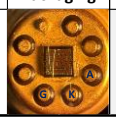
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
14	3	3D	24µ Cyl		350.424 ps	125.212 ps	470.646 ps	137.88 mV	✓	159k

Table 39: SPAD 3D (board 14) phase 1 results

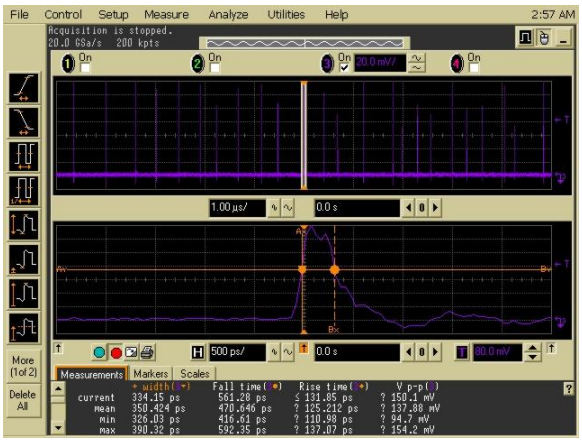


Figure 159: SPAD 3D (board 14) phase 1 waveform

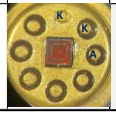
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
15	2	Cathode of 2D and the anode and cathode of 2B	Not discernible		985.037 ps	677.883 ps	665.767 ps	4.24 mV	x	short

Table 40: SPAD 2D/B (board 15) phase 1 results

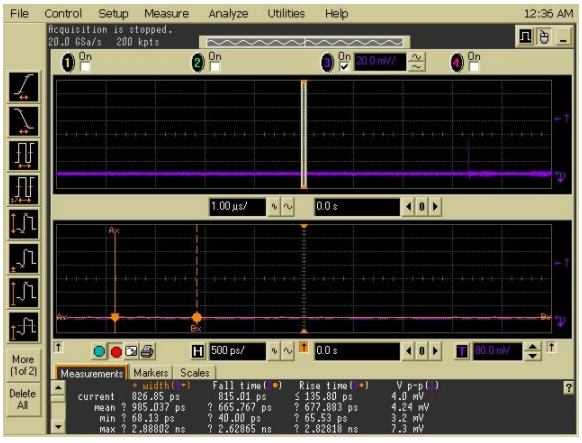


Figure 160: SPAD 2D/B (board 15) phase 1 waveform

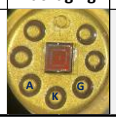
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
15	2	2L	24µ BPOLY/PPLUS Smaller		1.014 ns	694.24 ps	764.338 ps	5.47 mV	x	short

Table 41: SPAD 2L (board 15) phase 1 results

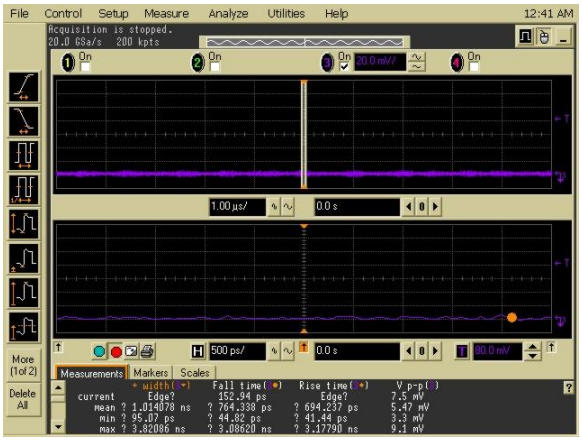


Figure 161: SPAD 2L (board 15) phase 1 waveform

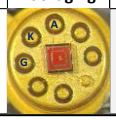
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
16	2	2S	50µ BPOLY/PPLUS Smaller		910.261 ps	785.709 ps	680.041 ps	4.90 mV	x	short

Table 42: SPAD 2S (board 16) phase 1 results

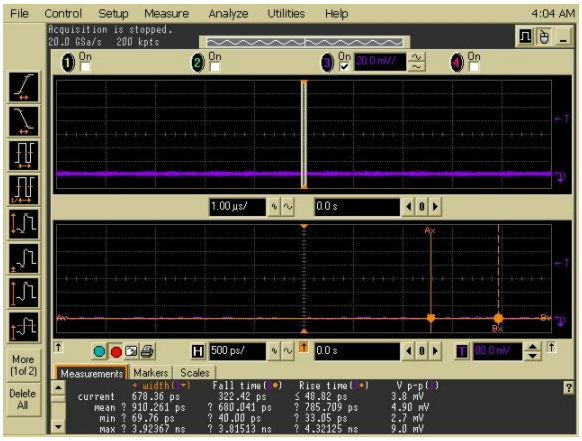


Figure 162: SPAD 2S (board 16) phase 1 waveform

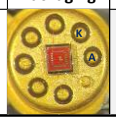
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
16	2	2X	50µ Circle No Sub		238.227 ps	133.525 ps	695.891 ps	108.13 mV	✓	short

Table 43: SPAD 2X (board 16) phase 1 results

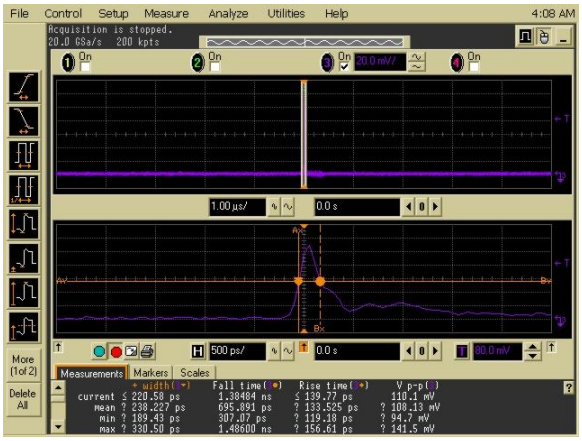


Figure 163: SPAD 2X (board 16) phase 1 waveform

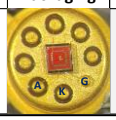
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
16	2	2K	24µ Standard		915.502 ps	702.738 ps	698.908 ps	4.43 mV	x	short

Table 44: SPAD 2K (board 16) phase 1 results

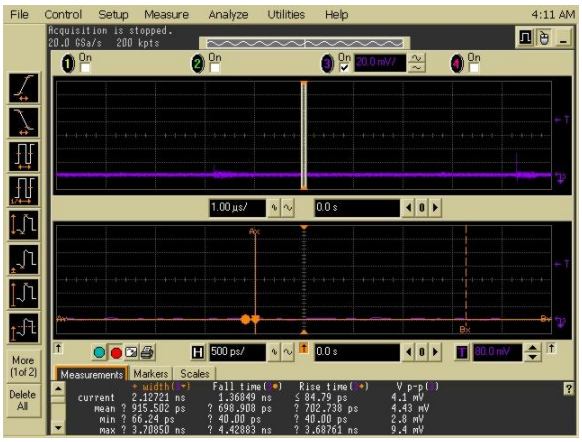


Figure 164: SPAD 2K (board 16) phase 1 waveform

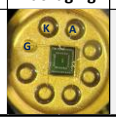
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
17	2	2D	5µ Standard		845.273 ps	715.941 ps	693.325 ps	4.89 mV	x	short

Table 45: SPAD 2D (board 17) phase 1 results

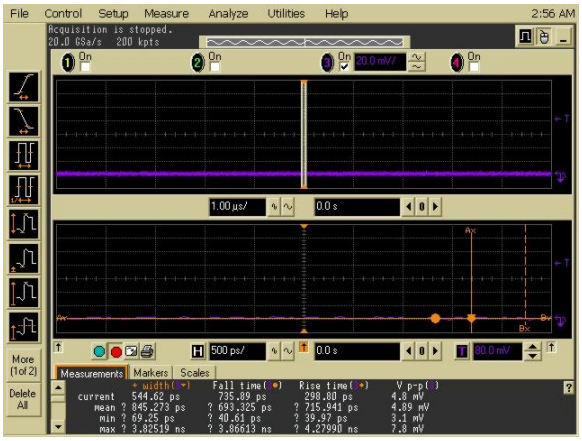


Figure 165: SPAD 2D (board 17) phase 1 waveform

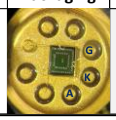
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
17	2	2N	24µ No EMITT		876.8704 ps	711.7051 ps	700.6933 ps	4.125 mV	x	short

Table 46: SPAD 2N (board 17) phase 1 results

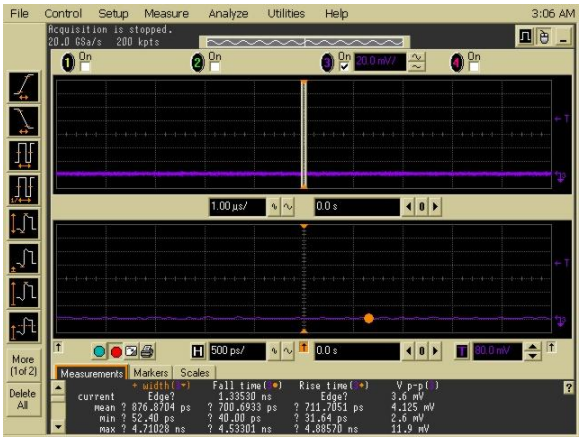


Figure 166: SPAD 2N (board 17) phase 1 waveform

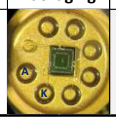
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
17	2	2H	5µ No Sub		207.44 ps	121.678 ps	299.540 ps	115.77 mV	✓	short

Table 47: SPAD 2H (board 17) phase 1 results

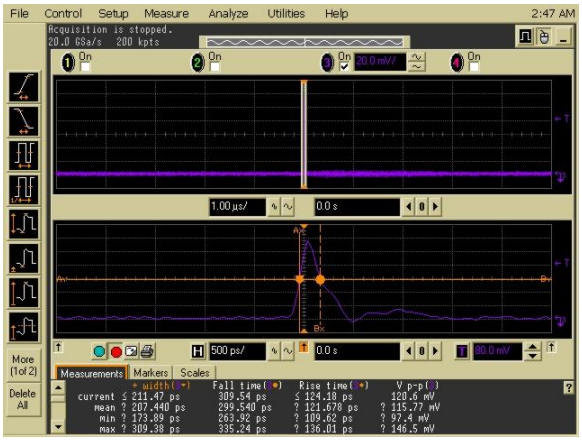


Figure 167: SPAD 2H (board 17) phase 1 waveform

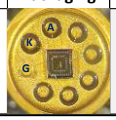
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
18	2	2R	50µ Standard		906.902 ps	780.617 ps	743.693 ps	4.29 mV	x	short

Table 48: SPAD 2R (board 18) phase 1 results

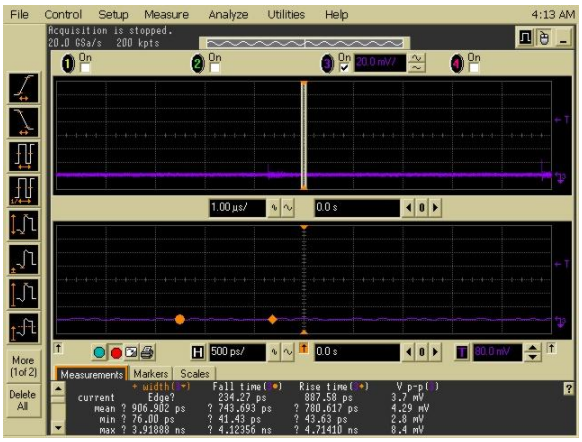


Figure 168: SPAD 2R (board 18) phase 1 waveform

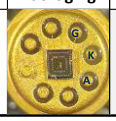
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
18	2	2A	5µ Elementary		866.339 ps	743.221 ps	672.853 ps	4.36 mV	x	short

Table 49: SPAD 2A (board 18) phase 1 results

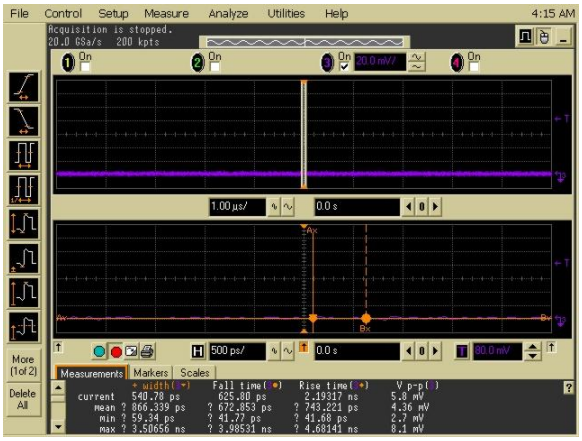


Figure 169: SPAD 2A (board 18) phase 1 waveform

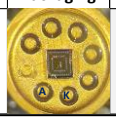
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
18	2	2J	5µ Circle No Sub		794.096 ps	767.751 ps	719.668 ps	4.7 mV	x	short

Table 50: SPAD 2J (board 18) phase 1 results

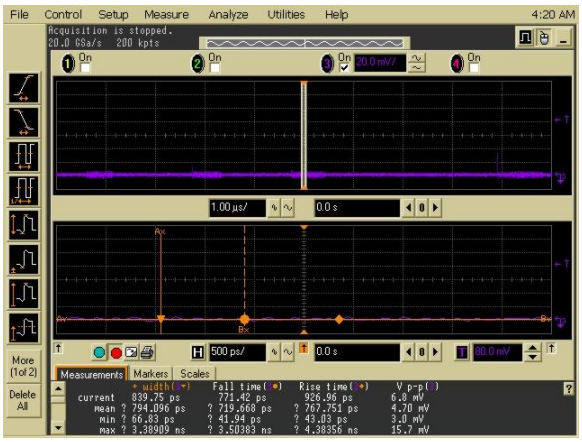


Figure 170: SPAD 2J (board 18) phase 1 waveform

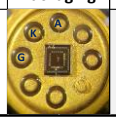
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
19	2	2E	5µ BPOLY/PPLUS Smaller		895.2516 ps	689.0267 ps	713.8976 ps	4.853 mV	x	short

Table 51: SPAD 2E (board 19) phase 1 results

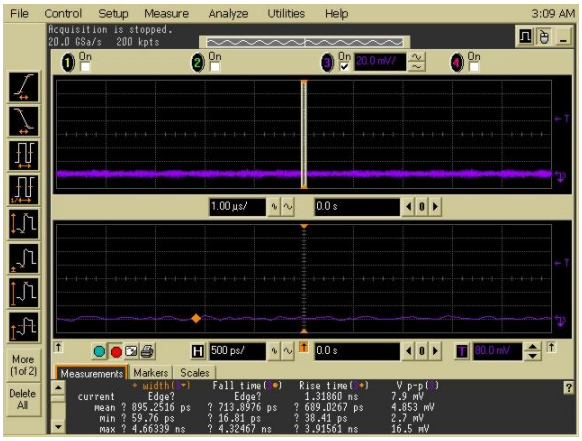


Figure 171: SPAD 2E (board 19) phase 1 waveform

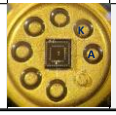
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
19	2	2O	24µ No Sub		243.250 ps	124.745 ps	672.991 ps	107.50 mV	✓	short

Table 52: SPAD 2O (board 19) phase 1 results

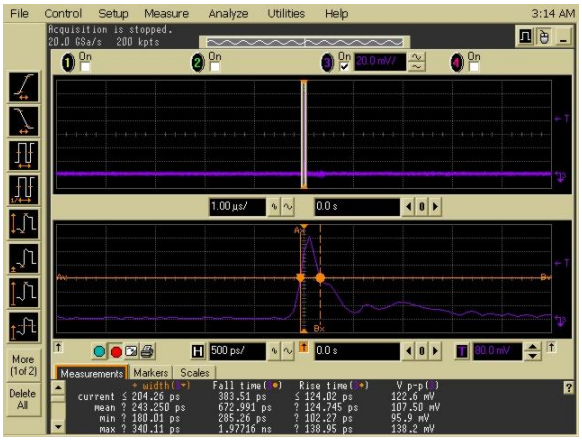


Figure 172: SPAD 2O (board 19) phase 1 waveform

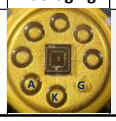
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
19	2	2U	50µ No EMITT		780.098 ps	845.548 ps	708.340 ps	4.09 mV	x	short

Table 53: SPAD 2U (board 19) phase 1 results

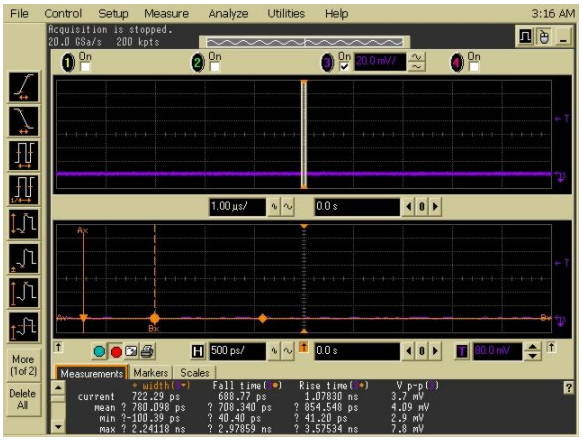


Figure 173: SPAD 2U (board 19) phase 1 waveform

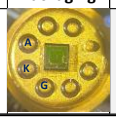
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
20	2	2T	50µ BPOLY/PPLUS		876.585 ps	712.082 ps	725.782 ps	4.86 mV	x	short

Table 54: SPAD 2T (board 20) phase 1 results

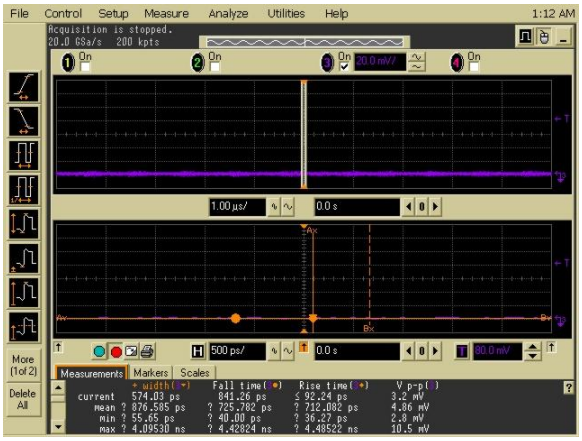


Figure 174: SPAD 2T (board 20) phase 1 waveform

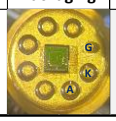
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
20	2	2W	50µ Circle		659.256 ps	659.256 ps	656.535 ps	4.33 mV	x	short

Table 55: SPAD 2W (board 20) phase 1 results

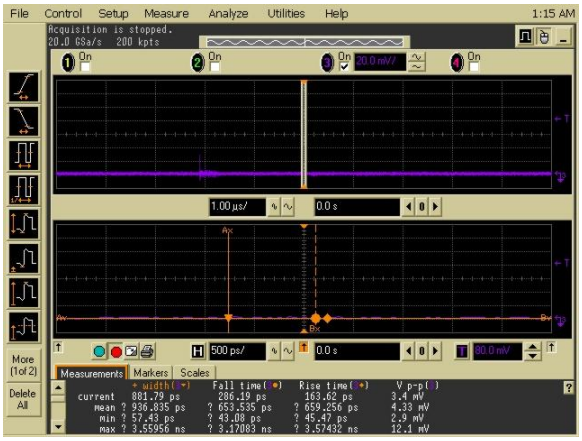


Figure 175: SPAD 2W (board 20) phase 1 waveform

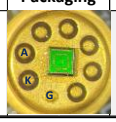
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
21	2	2I	5µ Circle		838.458 ps	648.225 ps	627.487 ps	4.74 mV	x	short

Table 56: SPAD 2I (board 21) phase 1 results

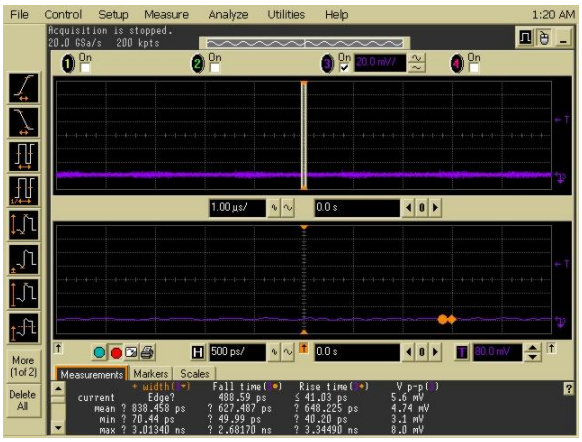


Figure 176: SPAD 2I (board 21) phase 1 waveform

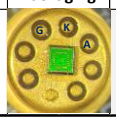
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
21	2	2C	50µ Elementary		718.536 ps	656.886 ps	650.908 ps	4.28 ps	x	short

Table 57: SPAD 2C (board 21) phase 1 results

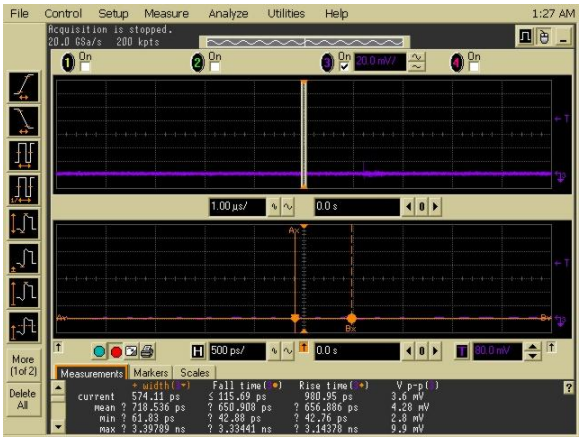


Figure 177: SPAD 2C (board 21) phase 1 waveform

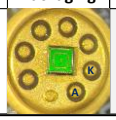
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
21	2	2V	50µ No Sub		915.233 ps	751.202 ps	720.494 ps	4.48 mV	x	short

Table 58: SPAD 2V (board 21) phase 1 results

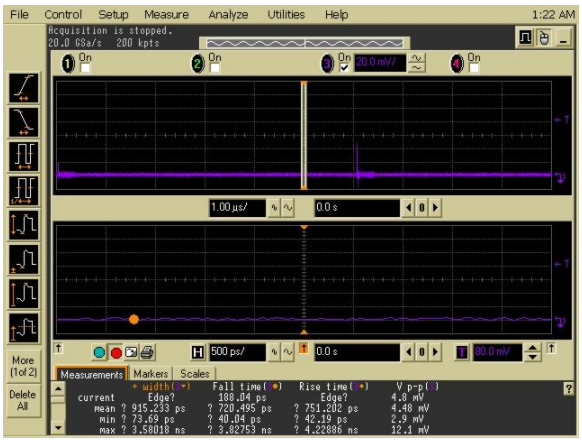


Figure 178: SPAD 2V (board 21) phase 1 waveform

Phase Two Data (976kΩ and 953kΩ Resistors)

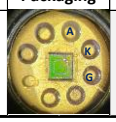
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
3	2	2B	24µ Elementary		331.941 ps	118.290 ps	563.061 ps	106.378 mV	✓	976k

Table 59: SPAD 2B (board 3) phase 2 results

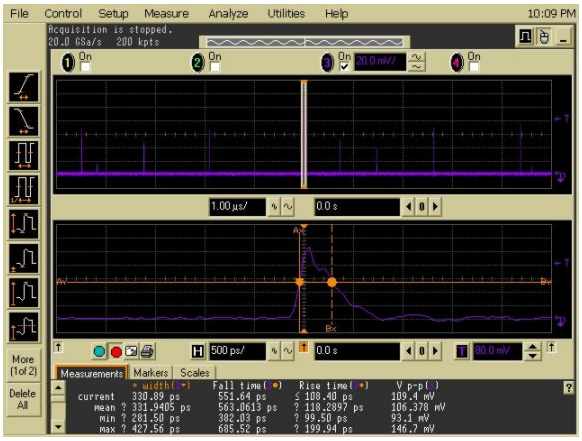


Figure 179: SPAD 2B (board 3) phase 2 waveform

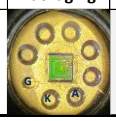
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
3	2	2K	24µ Standard		258.143 ps	121.173 ps	379.551 ps	106.07 mV	✓	976k

Table 60: SPAD 2K (board 3) phase 2 results

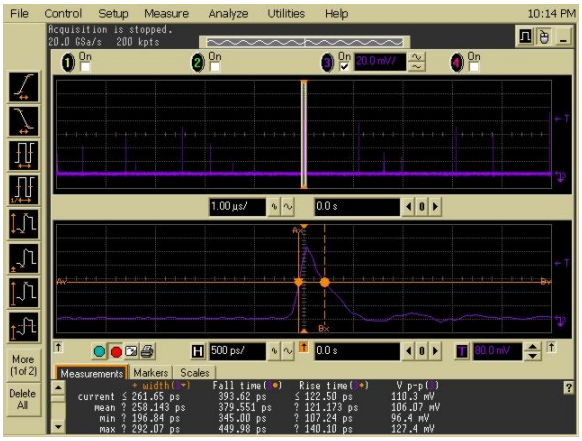


Figure 180: SPAD 2K (board 3) phase 2 waveform

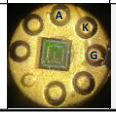
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
7	3	3Q	50µ noBNTUB2		281.018 ps	137.491 ps	300.311 ps	42.915 mV	✓	976k

Table 61: SPAD 3Q (board 7) phase 2 results

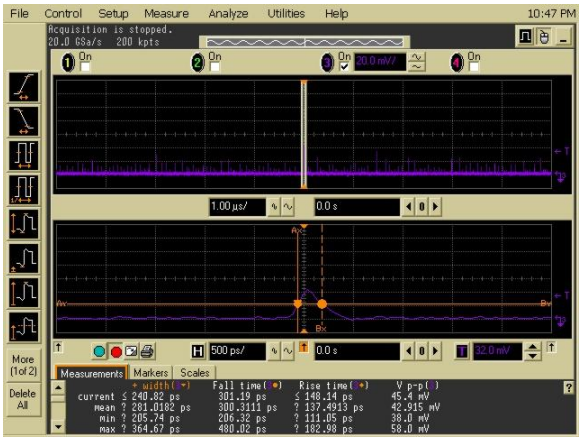


Figure 181: SPAD 3Q (board 7) phase 2 waveform

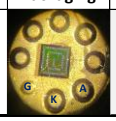
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
7	3	3R	50µ Striped BNTUB2		559.232 ps	145.421 ps	1.268 ns	45.876 mV	✓	976k

Table 62: SPAD 3R (board 7) phase 2 results

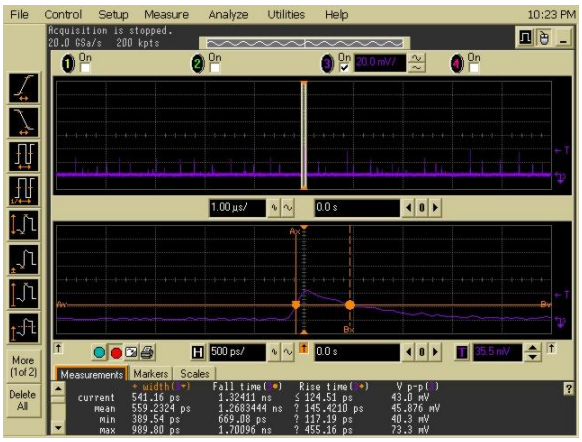


Figure 182: SPAD 3R (board 7) phase 2 waveform

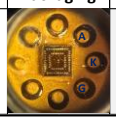
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
9	2	2D	5µ Standard		287.861 ps	119.402 ps	277.685 ps	144.687 mV	✓	976k

Table 63: SPAD 2D (board 9) phase 2 results

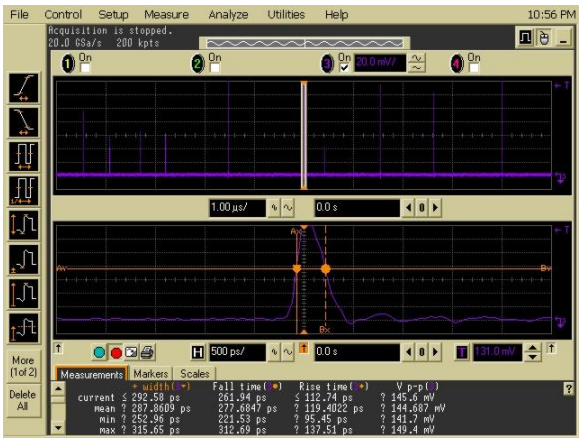


Figure 183: SPAD 2D (board 9) phase 2 waveform

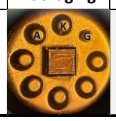
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
10	3	3F	24µ TUB		421.511 ps	132.951 ps	503.210 ps	59.292 mV	✓	976k

Table 64: SPAD 3F (board 10) phase 2 results

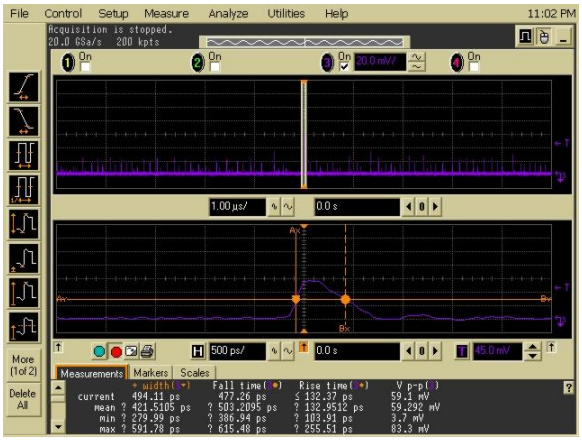


Figure 184: SPAD 3F (board 10) phase 2 waveform

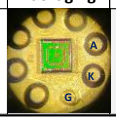
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
11	2	2I	5µ Circle		287.775 ps	112.774 ps	323.443 ps	156.25 mV	✓	976k

Table 65: SPAD 2I (board 11) phase 2 results

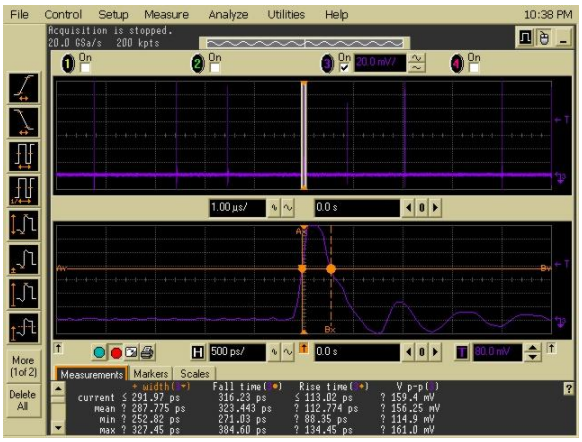


Figure 185: SPAD 2I (board 11) phase 2 waveform

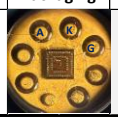
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
12	2	2P	24µ Circle		319.623 ps	126.556 ps	372.135 ps	114.514 mV	✓	976k

Table 66: SPAD 2P (board 12) phase 2 results

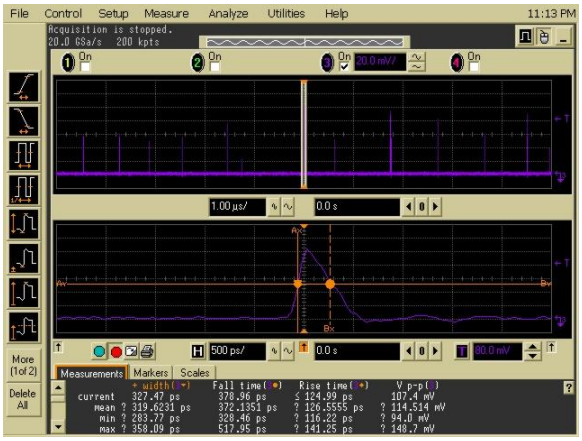


Figure 186: SPAD 2P (board 12) phase 2 waveform

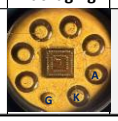
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
12	2	2W	50µ Circle		286.661 ps	133.715 ps	428.032 ps	107.460 mV	✓	976k

Table 67: SPAD 2W (board 12) phase 2 results

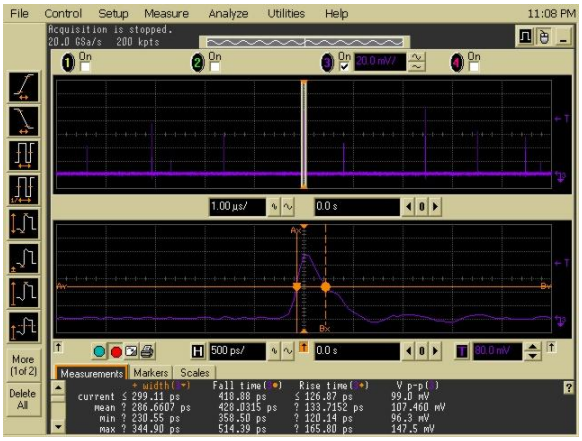


Figure 187: SPAD 2W (board 12) phase 2 waveform

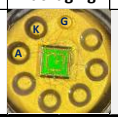
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
13	2	2R	50µ Standard		256.758 ps	131.057 ps	375.224 ps	105.42 mV	✓	976k

Table 68: SPAD 2R (board 13) phase 2 results

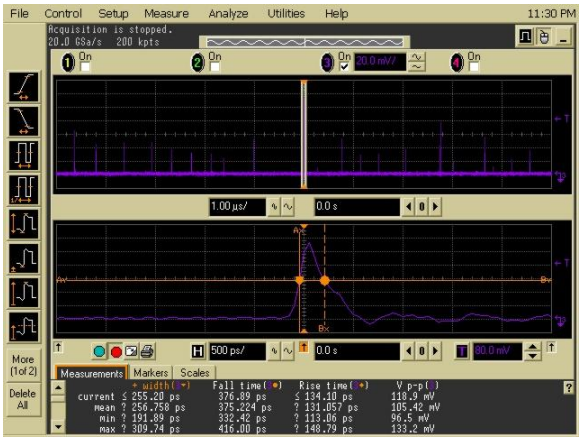


Figure 188: SPAD 2R (board 13) phase 2 waveform

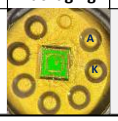
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
13	2	2X	50µ Circle No Sub		207.233 ps	134.300 ps	114.883 ps	123.360 mV	✓	976k

Table 69: SPAD 2X (board 13) phase 2 results

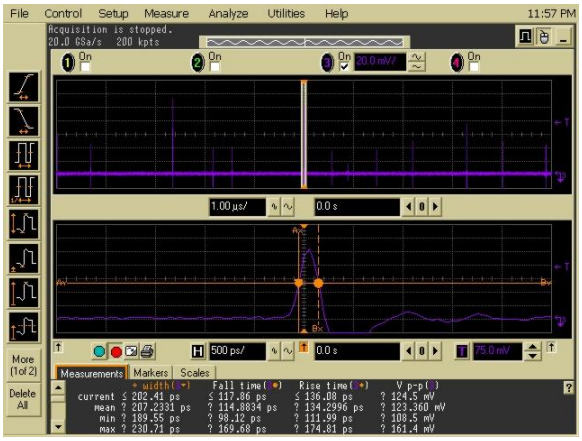


Figure 189: SPAD 2X (board 13) phase 2 waveform

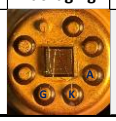
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
14	3	3D	24µ Cyl		364.370 ps	125.486 ps	449.828 ps	111.34 mV	✓	976k

Table 70: SPAD 3D (board 14) phase 2 results

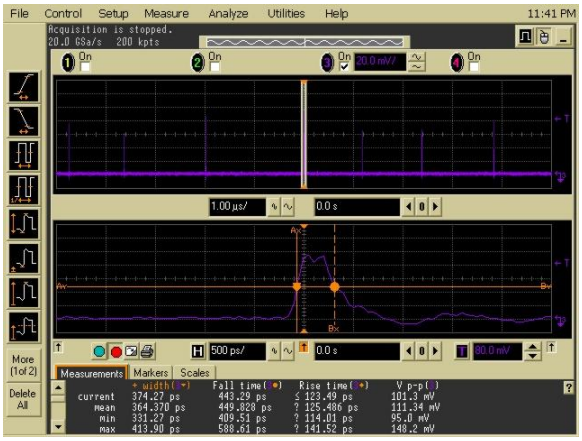


Figure 190: SPAD 3D (board 14) phase 2 waveform

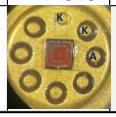
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
15	2	Cathode of 2D and the anode and cathode of 2B	Not discernible		292.390 ps	110.369 ps	423.658 ps	149.908 mV	✓	953k

Table 71: SPAD 2D/B (board 15) phase 2 results

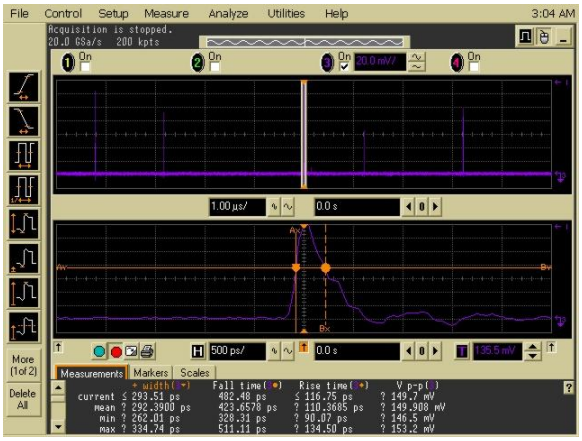


Figure 191: SPAD 2D/B (board 15) phase 2 waveform

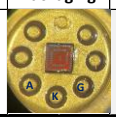
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
15	2	2L	24µ BPOLY/PPLUS Smaller		367.727 ps	242.210 ps	390.457 ps	24.282 mV	✓	953k

Table 72: SPAD 2L (board 15) phase 2 results

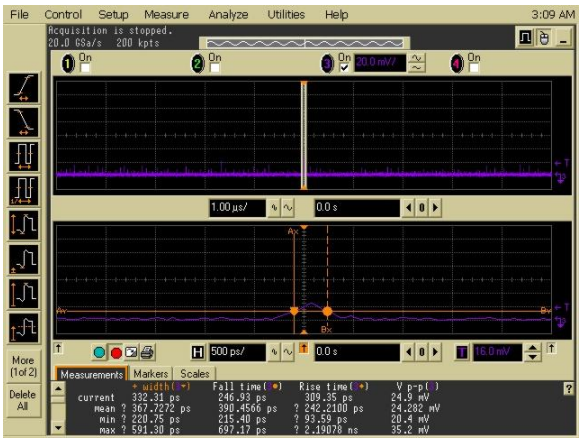


Figure 192: SPAD 2L (board 15) phase 2 waveform

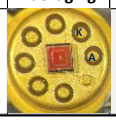
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
16	2	2X	50µ Circle No Sub		182.342 ps	126.907 ps	119.372 ps	127.283 mV	✓	976k

Table 73: SPAD 2X (board 16) phase 2 results

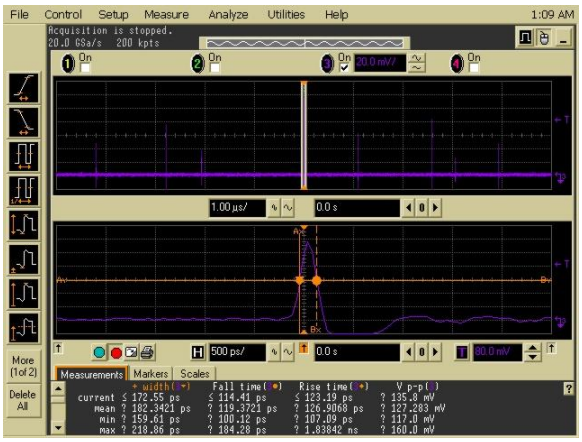


Figure 193: SPAD 2X (board 16) phase 2 waveform

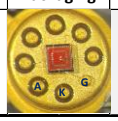
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
16	2	2K	24µ Standard		247.254 ps	122.799 ps	373.918 ps	112.477 mV	✓	953k

Table 74: SPAD 2K (board 16) phase 2 results

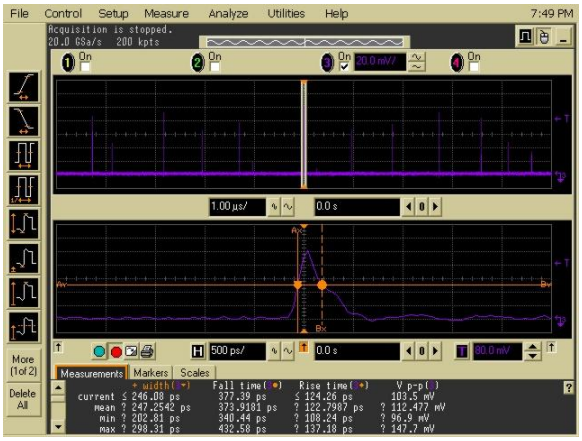


Figure 194: SPAD 2K (board 16) phase 2 waveform

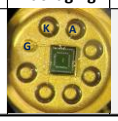
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
17	2	2D	5µ Standard		294.735 ps	120.522 ps	495.169 ps	55.259 mV	✓	953k

Table 75: SPAD 2D (board 17) phase 2 results

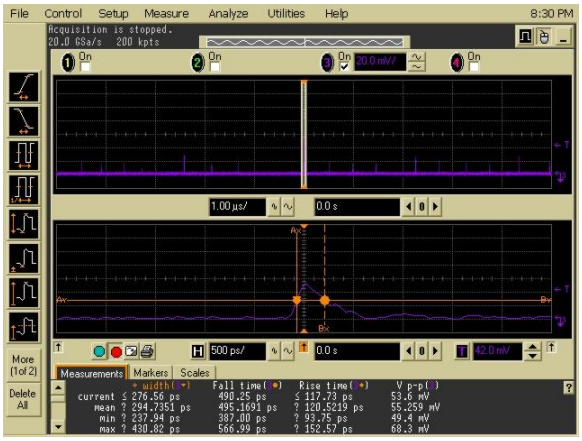


Figure 195: SPAD 2D (board 17) phase 2 waveform

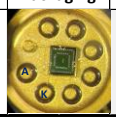
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
17	2	2H	5µ No Sub		170.965 ps	114.673 ps	113.297 ps	160.000 mV	✓	976k

Table 76: SPAD 2H (board 17) phase 2 results

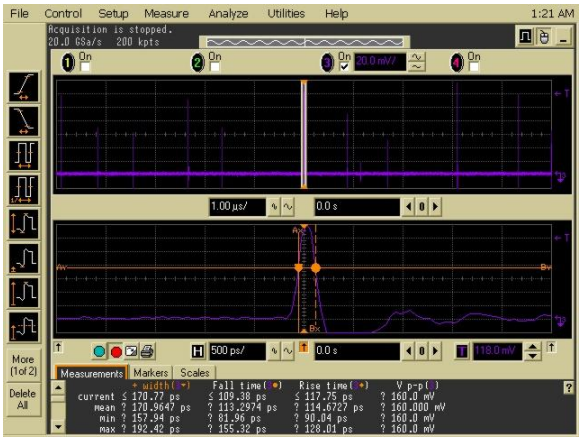


Figure 196: SPAD 2H (board 17) phase 2 waveform

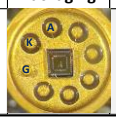
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
18	2	2R	50µ Standard		274.968 ps	135.666 ps	498.455 ps	101.278 mV	✓	953k

Table 77: SPAD 2R (board 18) phase 2 results

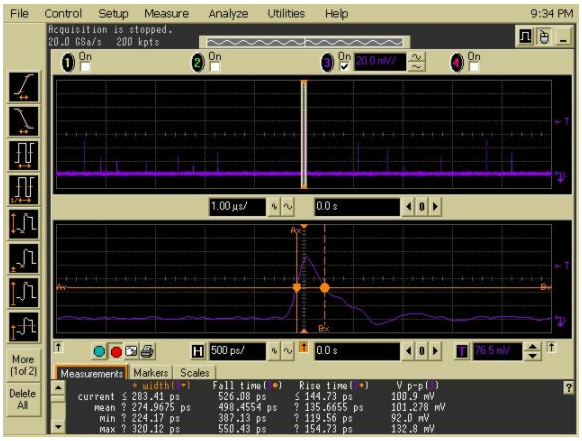


Figure 197: SPAD 2R (board 18) phase 2 waveform

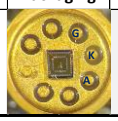
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
18	2	2A	5µ Elementary		302.769 ps	116.137 ps	731.763 ps	103.105 mV	✓	953k

Table 78: SPAD 2A (board 18) phase 2 results

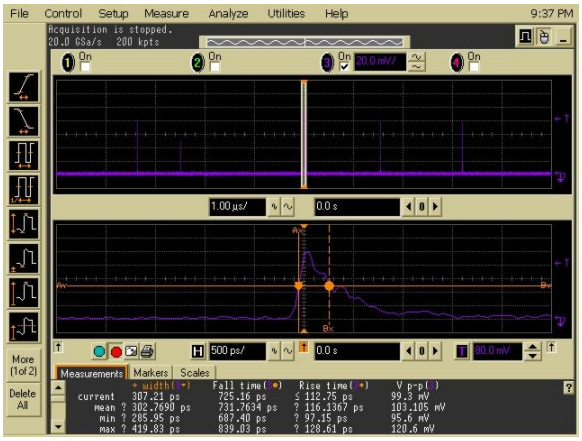


Figure 198: SPAD 2A (board 18) phase 2 waveform

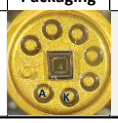
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
18	2	2J	5µ Circle No Sub		175.116 ps	115.546 ps	142.870 ps	126.372 mV	✓	953k

Table 79: SPAD 2J (board 18) phase 2 results

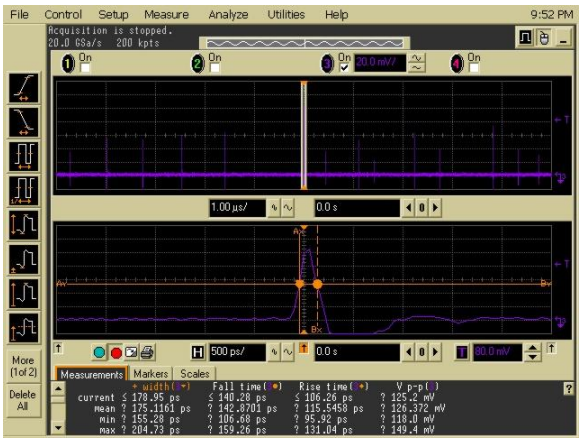


Figure 199: SPAD 2J (board 18) phase 2 waveform

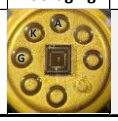
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
19	2	2E	5µ BPOLY/PPLUS Smaller		323.816 ps	140.531 ps	354.538 ps	55.41 mV	✓	953k

Table 80: SPAD 2E (board 19) phase 2 results

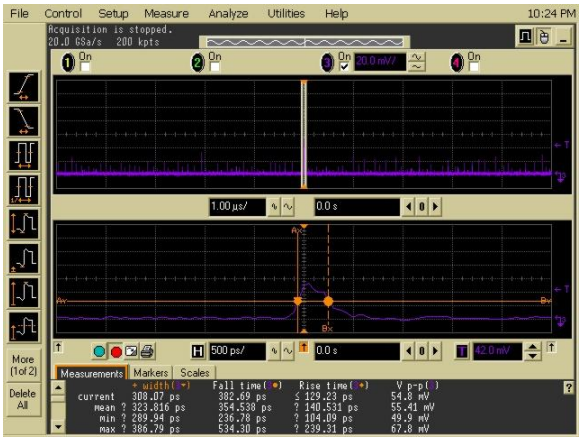


Figure 200: SPAD 2E (board 19) phase 2 waveform

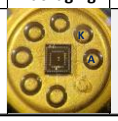
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
19	2	2O	24µ No Sub		185.957 ps	118.817 ps	155.806 ps	126.441 mV	✓	976k

Table 81: SPAD 2O (board 19) phase 2 results

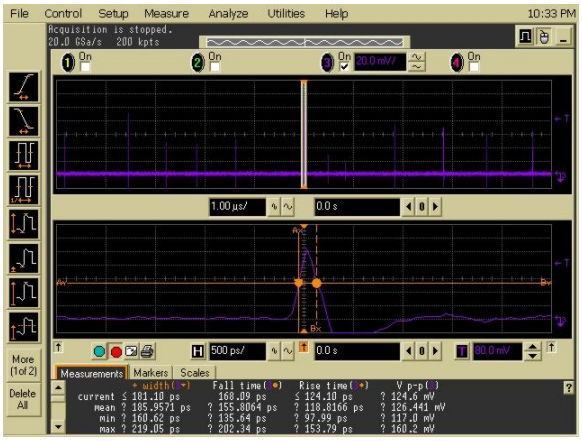


Figure 201: SPAD 2O (board 19) phase 2 waveform

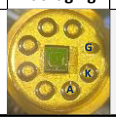
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
20	2	2W	50µ Circle		259.868 ps	130.641 ps	402.533 ps	121.731 mV	✓	953k

Table 82: SPAD 2W (board 20) phase 2 results

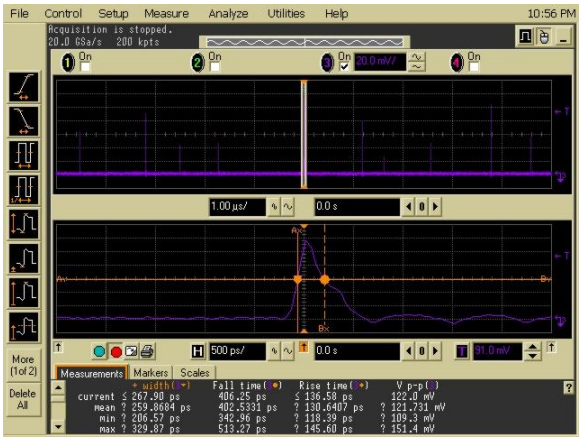


Figure 202: SPAD 2W (board 20) phase 2 waveform

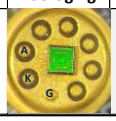
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
21	2	2I	5µ Circle		293.384 ps	120.599 ps	401.460 ps	74.254 mV	✓	953k

Table 83: SPAD 2I (board 21) phase 2 results

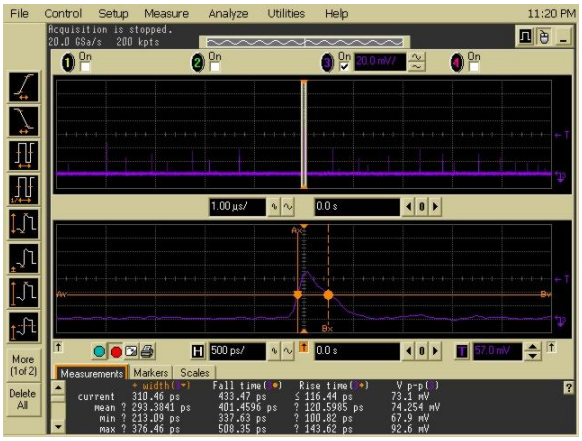


Figure 203: SPAD 2I (board 21) phase 2 waveform

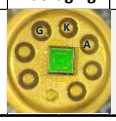
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
21	2	2C	50µ Elementary		327.142 ps	129.416 ps	491.028 ps	145.675 mV	✓	953k

Table 84: SPAD 2C (board 21) phase 2 results

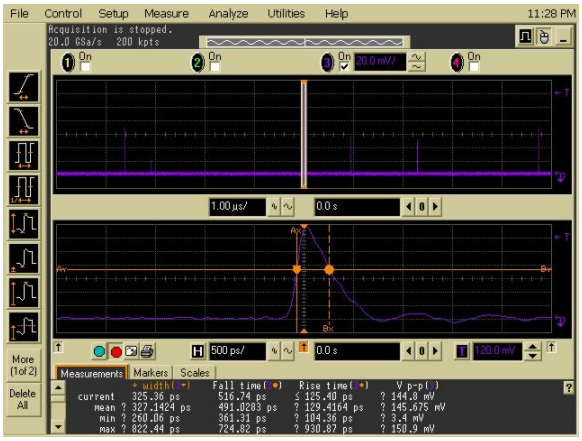


Figure 204: SPAD 2C (board 21) phase 2 waveform

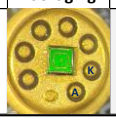
Board	Chip #	SPAD Identifier	SPAD	Packaging	Width	Rise Time	Fall Time	V p-p	Status	Quenching Resistor
21	2	2V	50µ No Sub		180.352 ps	126.781 ps	113.244 ps	119.060 mV	✓	953k

Table 85: SPAD 2V (board 21) phase 2 results

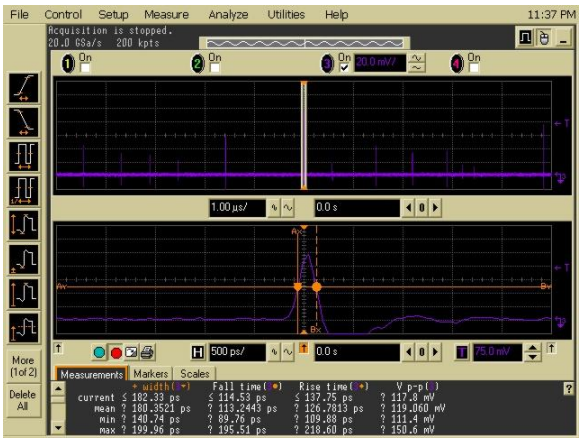


Figure 205: SPAD 2V (board 21) phase 2 waveform

APPENDIX B: SPAD 2H CURRENT MODE MATLAB CODE

```
close all
clear
clc

%load current mode testing data and initialize arrays
load('SPAD_current_data.mat');
x1 = cell2mat(thirtyk1(:,1));
x1N = zeros(length(x1),1);
y1 = cell2mat(thirtyk1(:,2));
x2 = cell2mat(sixtyk4(:,1));
x2N = zeros(length(x2),1);
y2 = cell2mat(sixtyk4(:,2));
x3 = cell2mat(one21k(:,1));
x3N = zeros(length(x3),1);
y3 = cell2mat(one21k(:,2));
x4 = cell2mat(two43k(:,1));
x4N = zeros(length(x4),1);
y4 = cell2mat(two43k(:,2));
x5 = cell2mat(four75k(:,1));
x5N = zeros(length(x5),1);
y5 = cell2mat(four75k(:,2));
x6 = cell2mat(nine53k(:,1));
x6N = zeros(length(x6),1);
y6 = cell2mat(nine53k(:,2));

%plot data
figure (1)
scatter(x1,y1,30,'red','filled')
hold on
scatter(x2,y2,30,'green','filled')
scatter(x3,y3,30,'blue','filled')
scatter(x4,y4,30,'magenta','filled')
scatter(x5,y5,30,[0.54, 0.81, 0.94],'filled')
scatter(x6,y6,30,[1, 0.5, 0],'filled')
title('SPAD Current Pulse Magnitudes vs Reverse Bias')
xlabel('Reverse Bias (V)')
ylabel('Current Pulse Magnitude (mA)')
legend('30.1k','60.4k','121k','243k','475k','953k',Location='northwest')
hold off

%normalize the data
for i = 1:length(x1)
    x1N(i) = x1(i) - x1(1);
end

for i = 1:length(x2)
    x2N(i) = x2(i) - x2(1);
end

for i = 1:length(x3)
    x3N(i) = x3(i) - x3(1);
```

```
end

for i = 1:length(x4)
    x4N(i) = x4(i) - x4(1);
end

for i = 1:length(x5)
    x5N(i) = x5(i) - x5(1);
end

for i = 1:length(x6)
    x6N(i) = x6(i) - x6(1);
end

%plot normalized data
figure (2)
scatter(x1N,y1,30,'red','filled')
hold on
scatter(x2N,y2,30,'green','filled')
scatter(x3N,y3,30,'blue','filled')
scatter(x4N,y4,30,'magenta','filled')
scatter(x5N,y5,30,[0.54, 0.81, 0.94],'filled')
scatter(x6N,y6,30,[1, 0.5, 0],'filled')
title('SPAD Current Pulse Magnitudes vs Normalized Excess Bias')
xlabel('Excess Bias (V)')
ylabel('Current Pulse Magnitude (mA)')
legend('30.1k','60.4k','121k','243k','475k','953k',Location='northwest')
hold off

%instantiate matricies for normal equation implementation to perform linear
%regression
xall = [x1N; x2N; x3N; x4N; x5N; x6N];
yall = [y1; y2; y3; y4; y5; y6];
X = [ones(length(xall),1), xall];

theta = inv(X' * X) * X' * yall;

xrange = linspace(0,2.5,1000);
yline = theta(1) + xrange*theta(2);

%plot normalized data with regression line
figure (3)
scatter(x1N,y1,30,'red','filled')
hold on
scatter(x2N,y2,30,'green','filled')
scatter(x3N,y3,30,'blue','filled')
scatter(x4N,y4,30,'magenta','filled')
scatter(x5N,y5,30,[0.54, 0.81, 0.94],'filled')
scatter(x6N,y6,30,[1, 0.5, 0],'filled')
plot(xrange,yline,'k',"LineWidth",2)
title('SPAD Current Pulse Magnitudes vs Normalized Excess Bias')
xlabel('Excess Bias (V)')
ylabel('Current Pulse Magnitude (mA)')
legend('30.1k','60.4k','121k','243k','475k','953k',Location='northwest')
hold off
```

```
%output SPAD internal resistance and breakdown voltage estimates to
%terminal
R = 1/(theta(2)*0.001);
Vbreak = (x1(1)+x2(1)+x3(1)+x4(1)+x5(1)+x6(1))/6;
fprintf('The estimated internal resistance is %.4f\n', R);
fprintf('The average breakdown voltage is %.4f\n', Vbreak);
```

REFERENCES

[1] "Our History," Nevada National Security Site, [Online]. Available: https://nnss.gov/about-the-nnss/nnss-history/. [Accessed 2025].

[2] R. Buckles, A. Sudderth, J. Bellow and S. Gardner, "Next-Generation Photomultiplier Detectors Using Transmissive III-Nitride Semiconductor Electrodes NLV-049-16, Year 3 of 3," Nevada National Security Site, 2018. [Online]. Available: https://www.osti.gov/servlets/purl/1476363. [Accessed 2025].

[3] R. Paschotta, "Photon Counting," RP Photonics Encylopedia, [Online]. Available: https://www.rp-photonics.com/photon_counting.html. [Accessed 2025].

[4] M. Wahl, "Time-Correlated Single Photon Counting," 2014. [Online]. Available: https://www.picoquant.com/images/uploads/page/files/7253/technote_tcspc.pdf. [Accessed 2025].

[5] M. Perenzoni, "Single-Photon Avalanche Diode-Based Detection and Imaging: Bringing the Photodiode Out of Its Comfort Zone," *IEEE Solid-State Circuits Magazine,* pp. 26-34, 2018.

[6] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, John Wiley & Sons, 2019.

[7] M. C. T. Bahaa E. A. Saleh, Fundamentals of Photonics, John Wiley & Sons, 2019.

[8] Hamamatsu, "Si Photodiodes," October 2023. [Online]. Available: https://www.hamamatsu.com/content/dam/hamamatsu-photonics/sites/documents/99_SALES_LIBRARY/ssd/si_pd_kspd9001e.pdf. [Accessed 2024].

[9] Wavelength Electronics, "Photodiode Basics: Selection and Operation," January 2020.

[Online]. Available: https://www.teamwavelength.com/download/applicationtechnotes/an-ld17.pdf?srsltid=AfmBOoopaDqItokIg6UAy8A53LQykbMqzTkjVE4jZT6klbbWwOI1SOJE. [Accessed 2024].

[10] A. A. E. V. A. D. Anna Vilà, "Geiger-Mode Avalanche Photodiodes in Standard CMOS Technologies," in *Photodetectors*, InTech, 2012.

[11] Hamamatsu, "Si APD," October 2021. [Online]. Available: https://www.hamamatsu.com/content/dam/hamamatsu-photonics/sites/documents/99_SALES_LIBRARY/ssd/si-apd_kapd9007e.pdf. [Accessed 2025].

[12] M. D. P. D. Bernicy S. Fong, "Timing resolution and time walk in super low K factor single-photon avalanche diode—measurement and optimization," *Journal of Nanophotonics,* vol. 12, no. 1, 2018.

[13] G. F. Knoll, Radiation Detection and Measurement, John Wiley & Sons, 2010.

[14] K. S.-H. H. Z. Michael Hofbauer, Single-photon Detection for Data Communication and Quantum Systems, IOP Publishing Ltd, 2021.

[15] Austriamicrosystems, "0.35um HBT BiCMOS Process Parameters," 2009.

[16] D. Gentry, *Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process,* University of Nevada, Las Vegas, 2018.

[17] M. G. A. L. C. S. F. Z. S. Cova, "Avalanche photodiodes and quenching circuits for single-photon detection," *Applied Optics,* pp. 1956-1976, 1996.

[18] R. H. Haitz, "Mechanisms Contributing to the Noise Pulse Rate of Avalanche Diodes," *Journal of Applied Physics,* vol. 36, no. 10, p. 3123–3131, 1965.

[19] R. H. B. S. T. F. L. G. J. R. W. F. Andreas Eisele, "185 MHz Count Rate, 139 dB Dynamic Range Single-Photon Avalanche Diode with Active Quenching Circuit in 130 nm CMOS Technology," in *IISW Session 10: Invited Presentation and Avalanche Diode Sensors*, Hokkaido, Japan, 2011.

[20] N. M. D. S. Lucio Pancheri, "SPAD Image Sensor With Analog Counting Pixel for Time-Resolved Fluorescence Detection," *IEEE Transactions on Electron Devices,* vol. 60, no. 10, pp. 3442-3449, 2013.

[21] F. G. F. Z. Simone Tisa, "Variable-Load Quenching Circuit for single-photon avalanche diodes," *Optics Express*, vol. 16, no. 3, pp. 2232-2244, 2008.

CURRICULUM VITAE

Abraham Castaneda
acasta1138@gmail.com

Education

University of Nevada, Las Vegas 2023 - 2025 (expected)
Master of Science in Electrical Engineering (GPA: 4.0)

University of Nevada, Las Vegas 2019 - 2023
Bachelors of Science in Electrical Engineering (GPA: 3.85)
Honors College / Magna Cum Laude

Research/Experience:

Intern/Graduate Research Assistant January 2024 – Present
NNSS | Mission Support and Test Services | UNLV | Dr. Baker Research Group

- Tested and characterized pulse widths and recovery times of single-photon avalanche diode (SPAD) structures to inform the design of a SPAD array for the Digitized Nanosecond Silicon-Germanium Photo-Multipliers for Prompt Radiation Detection project (Site-Directed R&D)
- Created bond plans and wirebonded SPAD integrated circuit test fixtures to various packages
- Designed and 3D printed receptacles for interfacing chips with integrating spheres for testing
- Assisted in setting up photon counting equipment that incorporates GPIB
- Redesigned a chip-on-board PCB to house a CQFJ-28 packaged 350nm photon counting integrated circuit for testing
- Incorporated old AustriaMicroSystems 350nm process designs for SPAD quenching circuits, analog counters, and mono-stable gating circuits into the TowerJazz 180nm SiGe BiCMOS process and performed simulations in Cadence and LTspice to determine feasibility and to debug issues with the original 350nm chip
- Designed behavioral SPAD SPICE models from real testing data to more accurately simulate new quenching circuits
- Designed, simulated, and developed layouts for out two new pixel designs featuring high dynamic range, actively quenched SiGe SPADs with sub-nanosecond reset times and 70-100ps pulse widths as well as in-pixel analog counters

Electrical Engineering OSTEM Intern/Research Assistant/Fellow June 2022 – Present
NASA | Goddard Space Flight Center

- Modified existing electrical designs for scientific instruments that will be used for measuring electric fields and charged particles in space
- Developed single- and dual-output, PC/104 form factor, space-grade, EMI filtered DC-to-DC converter boards from design and simulation to layout in support of the Black and Diffuse Aurora Science Surveyor (BaDASS) sounding rocket mission planned to be launched at Poker Flat Research Range

- Developed a multiple-rail low-dropout regulator board to interface with a dual output power converter
- Supported the PCB ordering and fabrication process remotely through documentation and tested the prototype hardware to ensure proper operation and EMI compliance in accordance with GSFC technical standards
- Calibrated makeshift RF current probes for conducted emissions testing
- Staked PCBs for flight
- Participated in payload integration for the Ground Imaging to Rocket investigation of Auroral Fast Features (GIRAFF) sounding rocket mission as well as sequence testing of BaDASS at Wallops Flight Facility
- Assisted in radiated EMI testing of a sounding rocket payload inside an anechoic chamber
- Served as EMI testing, communications and ground systems lead for the SPEID CubeSat team, which aimed to design a fleet of CubeSats capable of taking video of the OSAM-1 satellite reservicing mission and perform 3D reconstruction
- Generated plans and procedures for EMI pre-compliance testing of CubeSat avionics
- Created a Near Earth Network based ground system architecture that fit CubeSat mission demands and constraints
- Conducted a trade study to identify the best communication hardware appropriate for the SPEID CubeSat mission
- Served as a subject matter expert and mentor for high-school interns

Graduate Teaching Assistant August 2023 – December 2024
University of Nevada, Las Vegas | Department of Electrical and Computer Engineering

- Served as TA for EE 421L Digital Integrated Circuit Design Laboratory, ECG 721 Memory Circuit Design, and ECG 722 Mixed-Signal Circuit Design
- Responsible for grading quizzes, exams, lab reports, and homework assignments as well as updating grade sheets
- Conducted office hours to provide mentoring and instruction to students in need

Undergraduate Research Assistant May 2021 – August 2022
University of Nevada, Las Vegas | Dr. Baker Research Group

- Temperature tested bandgap reference voltage on chips for NASA contract pertaining to the development of Tiled Silicon Photomultiplier Array Read-Out Integrated Circuits
- Soldered SMD and through-hole components to PCBs
- Wire-bonded chips onto QFP-44 and SOIC-28 packages
- Designed and 3D printed PCB holders and covers for newly designed boards
- Aided in the wiring of IC schematics and design of custom footprints using DipTrace

Undergraduate Researcher June 2021 – August 2021
University of Nevada, Las Vegas | REU Smart Cities Program

- Benchmarked an open source, low-power, configurable, high-performance RISC-V microprocessor to see how it compares performance-wise with other processors on the market
- Learned how to write abstracts, analyze research papers/studies, collect data, and present findings through a research poster at UNLV's Summer Research Symposium

Activities

Avionics/Power Team Lead January 2022 - August 2022

University of Nevada, Las Vegas | RebelSat

- Managed a team of electrical and computer engineering students to help develop the electrical systems of UNLV's first SmallSat/CubeSat
- Led the search for substitutes for critical electrical components amid a chip shortage
- Oversaw the design of circuit boards for sensor modules, connector boards, and solar panel modules

Projects:

Project NEMO | Devil's Invent: Hardening of Soft Targets Hackathon Spring 2021

- Worked as a team to propose a layered cybersecurity approach to protect municipal water facilities from hackers using measures such as employee credential validation, air gapping, and improved integrity of firewalls (3rd place)

Switched Mode Power Supply Design Fall 2022

- Using LTspice, designed and simulated a flyback switched mode power supply capable of converting 100-130VAC to 5VDC at 1A for USB 2.0 charging using off-the-shelf components

Solar Powered AC Relay System Fall 2022 - Spring 2023

- Designed a relay system that directs extra solar power not used by a solar compatible air conditioning unit to a lithium-ion battery bank

Third Order Lowpass Butterworth Filter Spring 2023

- Designed, simulated, implemented, and tested a third order lowpass Butterworth filter given a transfer function using op-amps, resistors, and capacitors

CMOS Synchronous Buck Converter Fall 2023

- Using Cadence, designed and laid out a synchronous buck converter capable of regulating a 4V-5.5V VDD input to a 3.125V output capable of supplying 0mA-100mA of current using Micron's C5 600nm process

Digital Pixel Averaging Circuit Spring 2024

- Using LTspice and a standard 50nm process, designed and simulated an eight-pixel averaging circuit tailored for delta-sigma modulators through the use of CMOS counters and arithmetic circuits

Continuous Time K-Delta-1-Sigma Analog-to-Digital Converter Fall 2024

- Using LTspice and Micron's C5 600nm process, designed and simulated a continuous time 8-path KD1S second-order noise shaping ADC with a nominal 43.50dB SNR, 14MHz bandwidth and effective parallel resolution of 6.71 bits (serial resolution of 6.93 bits). An 8-bit linear serial feedback register noise dither was also designed for improved performance in DC sensing applications.