INDIRECT FEEDBACK COMPENSATION TECHNIQUES FOR MULTI-STAGE OPERATIONAL AMPLIFIERS

by

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A thesis

submitted in partial fulfillment

of the requirements for the degree of

Masters of Science in Electrical Engineering

Boise State University

October 2007

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The thesis presented by Vishal Saxena entitled “Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers” is hereby approved:

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DEDICATION

This work is dedicated to Shri Narayana - the eternal witness beyond the manifest, Shri Sharada - the knowledge personified, and to the timeless masters of the Advaita Vedanta (Non-dualistic Idealism) philosophy.

ACKNOWLEDGEMENT

I would like thank my advisor Dr. Jake Baker for teaching a series of wonderful courses on Analog and Mixed Signal Circuit Design and for encouraging me to engage in creative research through his continued support and fraternal guidance. His alacritous responses to my ideas have been of invaluable help to me in obtaining significant advances in circuit design. I have learned immensely from his diligent work ethics, his phenomenal teaching and his strikingly humane approach. I would also like to thank my teachers and colleagues at Indian Institute of Technology Madras for instilling an attitude of academic excellence in me. Further, I would like to thank Dr. Jeff Jessing, Dr. Stephen Parke and Dr. John Chiasson for teaching valuable courses at BSU and Dr. Kris Campbell for being on my thesis committee. Immense thanks to my parents, siblings Divya and Akshay for their unfettered affection and support.

Special thanks to Mahesh Balasubramaniam for the chip layouts. I would also like to single out Jagdish Narayan Pandey, Ajay Taparia and Rajesh T.K. for their long-distance philosophic discussions. Thanks are due aplenty to Rahul Mhatre, Sanghyun Park, Nirav Dharia, Scott Koehler, Gary VanAkern, Todd Plum, Shantanu Gupta, Prashanth Busa, Hemanth Ande, Armand Bregaj and Rushi Rathod for being a good company at Boise.

ABSTRACT

Introduction

To achieve high gain with continued scaling in CMOS fabrication processes, use of three-stage op-amps has become indispensable. In the progression of CMOS technology development, the supply voltage has been decreasing while the transistor threshold voltages do not effectively scale. Also the inherent gain available from the transistors has been decreasing with downsizing of the transistor gate length. The traditional techniques for achieving high gain by vertically stacking up (i.e. cascoding) the transistors, to achieve high gain are becoming difficult to realize in the modern sub-100nm processes as the threshold voltage doesn't scale well. Thus the paradigm of vertical cascoding of transistors needs to be replaced by the horizontal cascading in order to design op-amps in low supply voltage processes.

This thesis presents novel multi-stage topologies for singly ended as well as fully differential op-amps with the highest performance ever reported. We have also explored and comprehensively developed the indirect feedback compensation theory for the two-stage as well as the multi-stage op-amps. The proposed indirect compensated op-amps exhibit significant improvements in speed over the traditional Miller compensated op-amps and result in much smaller layout size and lower power consumption.

Contributions in this Thesis

•Indirect feedback compensation for two and higher stage op-amps have been analyzed for all known topologies. Analysis for novel indirect feedback compensation method employing split-length devices is presented. Split-length device indirect feedback compensation is useful in high speed compensation of low-voltage op-amp topologies. The split-length indirect compensation lays the foundation for the development of ultra low power and high performance multi-stage op-amps. A test chip containing the various two-stage topologies has been fabricated in a $0.5\mu m$ CMOS process and tested for the same load conditions. The split-length indirect compensated op-amps displayed a ten times enhancement in the gain-bandwidth and four times faster transient settling compared to the traditional Miller compensated op-amp topologies. The tested performance of the op-amps is in close accordance with the simulated results as we have used a relatively long channel CMOS process where the process variations and random offsets are negligible.

•Stable and low power three-stage op-amps can also be designed by using indirect feedback compensation, in conjunction with pole-zero cancellation, to achieve excellent phase margins close to $90°$. A theory for the compensation of three and multi-stage op-amps has been presented which matches well with simulations and experiments. The three-stage op-amps documented in this thesis achieve highest simulated figures-of-merit (FoMs) compared to the state-of-art and can be directly used in integrated systems to achieve higher performance. A second chip containing various three-stage singly-ended op-amps has been designed in $0.5\mu m$ CMOS process and is presently in fabrication.

•We have presented a discussion on the impractical and incorrect multi-stage biasing schemes which are commonly found in literature. It has been demonstrated that diff-amps must be used for the internal gain stages for robust biasing of the multi-

stage op-amp. The theory for three-stage op-amp design has been extended to a generalized n-stage op-amp case and can be used to build higher order multi-stage op-amps.

•Novel multi-stage fully-differential op-amp topologies are presented which amend the impractical topologies widely reported in literature. The fully differential topologies proposed in this work combine improvised biasing schemes and novel common-mode feedback techniques to obtain op-amp topologies which are robust to large offsets. The simulated performance of the fully-differential three-stage op-amps improves by at least three times in performance over the state-of-the-art. A third test chip containing numerous fully-differential op-amps has been designed in the same 0.5μm CMOS process and is getting fabricated. The test results for all three-stage op-amps are expected to be close to the simulated performance for this process.

List of Publications

1. Saxena, V., and Baker, R. J., "Indirect Feedback Compensation of CMOS Op-Amps," Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), pp. 3-4, April, 2006.

Submitted and in preparation

1. Saxena, V., and Baker, R. J., "Compensation of CMOS Op-Amps using Split-Length Transistors," submitted to International Conference for Circuits and Systems, 2008.

2. Saxena, V., and Baker, R. J., "Indirect Feedback Compensation for Three-Stage CMOS Operational Amplifiers," to be submitted to IEEE Journal of Solid State Circuits, 2008.

3. Saxena, V., and Baker, R. J., “Indirect Feedback Compensation Techniques for Multi-Stage CMOS Operational Amplifiers,” to be submitted to IEEE Transactions on Circuits and Systems-I, 2008.

4. Saxena, V., and Baker, R. J., “Multi-Stage Fully-Differential Operational Amplifiers using Indirect Feedback Compensation,” to be submitted to IEEE Journal of Solid State Circuits, 2008.

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INTRODUCTION

OPERATIONAL Amplifiers are one of the indispensable blocks of modern integrated systems and are used in wide varieties of circuit topologies like data converters, filters, references, clock and data recovery circuits. However, continued scaling in CMOS processes has continuously challenged the established paradigms for operational amplifier (op-amp) design. As the feature size of CMOS devices keeps shrinking, enabling yet faster speeds, the supply voltage is scaled down to enhance device reliability and to reduce power consumption. The expressions for a short channel MOSFET transition frequency (f_T) and open-loop gain ($g_m \cdot r_o$) are given as [1]

$$f_T \propto \frac{V_{ov}}{L} \tag{1.1}$$

$$g_m r_o \propto \frac{L}{V_{ov}} \tag{1.2}$$

where V_{ov}, L, g_m and r_o are the overdrive voltage, channel length, transconductance and output resistance respectively for a MOSFET.

From Equations 1.1 and 1.2, it can be observed that downward scaling in gate length results in a larger f_T, and hence faster transistors. But the higher speed comes at the cost of a reduction in transistor's open loop gain. Hence the amplifiers designed with scaled processes exhibit larger bandwidths but lower open loop gains.

Also with device scaling the supply voltage has also been continually reduced. However, the threshold voltage of transistors doesn't scale well in order to keep transistor leakage under control. This will eventually preclude gain enhancing techniques like cas-

coding (vertically stacking transistors to increase gain) of transistors and gain-enhancement by employing amplifiers in cascode configuration [1].

Figure 1-1 displays the trend in scaling of transistor supply voltage (VDD) and digital and analog threshold voltages with process technology or production year. The trends have been compiled by combining data from the 2006 ITRS report update [2] and the predictive sub-45nm device modeling [3].

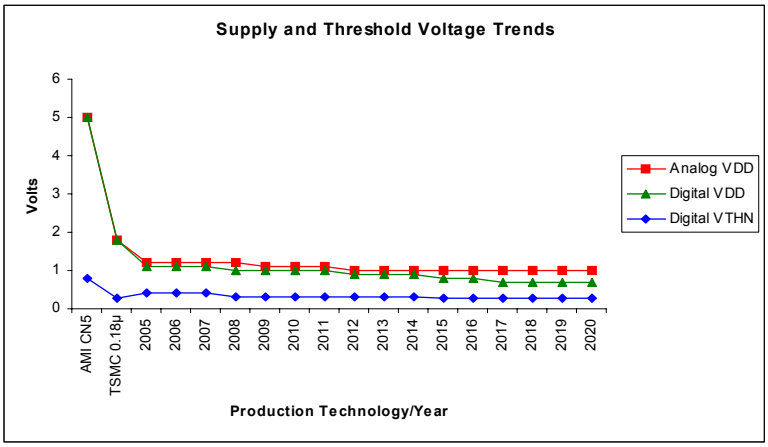

Figure 1-1. Trends for transistor supply and threshold voltage scaling with advancement in CMOS process technology [2],[3].

From Figure 1-1, it can be observed that the NMOS transistor threshold voltage (V_{THN}) is not projected to scale while the VDD will scale down continually. Also the VDD for digital process is set to scale more than the analog VDD, which will make seamless integration of analog circuits difficult in digital processes.

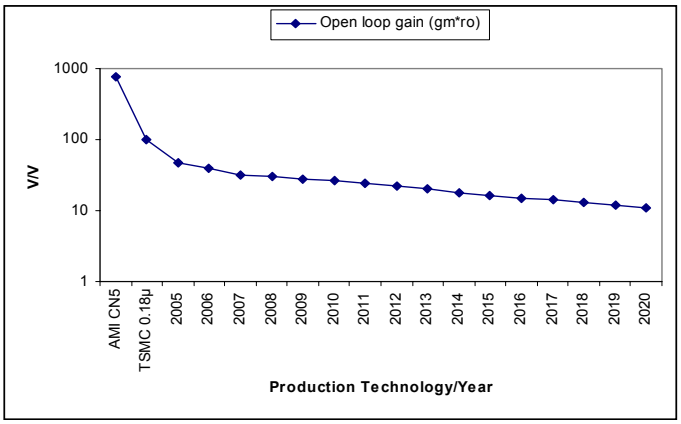

Figure 1-2. Trends for transistor open-loop gain with CMOS process technology progression [2],[3].[1]

Figure 1-2 shows the reduction in open-loop gain with process scaling. The open loop gain value of around to value in 100's in AMI's $0.5\mu m$ process has dropped to 10's in the sub-100 nm processes. Also with scaling, the process variations become more pronounced as indicated by the expression for the threshold-voltage mismatch ($\sigma_{\Delta VTH}$) given by [2]

$$\sigma_{\Delta VTH} \propto \frac{1}{L \cdot W} \tag{1.3}$$

This leads to significant random offsets in op-amps due to the device mismatches.

1. The ITRS report [2] proposes that the open-loop gain for the Analog CMOS process will be maintained at 30 for designs with $5 \times L_{min}$, L_{min} being the minimum gate length for the corresponding digital process. However in the figure a gradual decline in open loop gain is assumed for realistic design estimates.

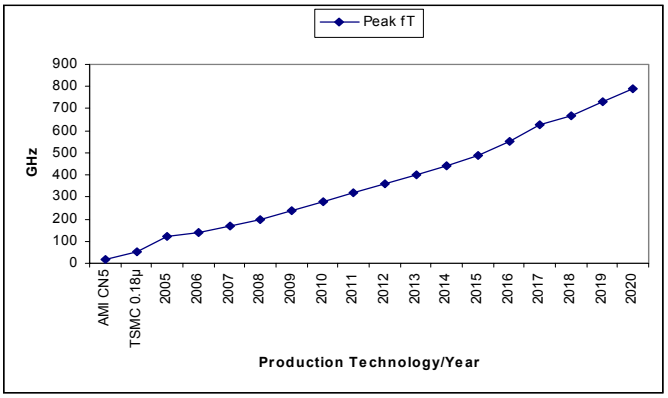

Figure 1-3. Trends for transistor transition frequency (f_T) with CMOS process technology progression [2],[3].

Figure 1-3 shows the projected enhancement in the peak f_T of the devices in upcoming CMOS process technologies, which is a desirable progression.

Now, for an N bit resolution ADC, the open loop DC gain (A_{OLDC}) of the op-amp required is given as

$$\left|A_{OLDC}\right| \geq \frac{1}{\beta} \cdot 2^{N+1} \tag{1.4}$$

where β is the feedback factor in the op-amp topology. For $\beta = 1/2$, which is the case in a R-2R data-converter, the required loop gain is given as [5]

$$\left|A_{OLDC}\right| \geq 2^{N+2} \tag{1.5}$$

Thus for 10 and 14 bit resolution ADC/DACs, the required open loop DC gains are 4K and 16K respectively. Figure 1-4 illustrates the number of cascaded stages required to design a 10 bit ADC/DAC. Also wide-swing cascoded op-amp designs have been illustrated in [1] for a 50nm CMOS process model (VDD=1V). Thus Figure 1-4 also depicts the

number of stages required when the internal stages are wide-swing cascoded for N=14. The swing for a wide-swing cascoded is given as $(2V_{DS,\,sat},\ VDD - 2V_{DS,\,sat})$, where $V_{DS,sat}$ is the saturation voltage for the transistors for the given bias. Also since $V_{DS,sat}$ is not really scaling down with VDD, the wide-swing cascoding technique may not be a suitable option in future.

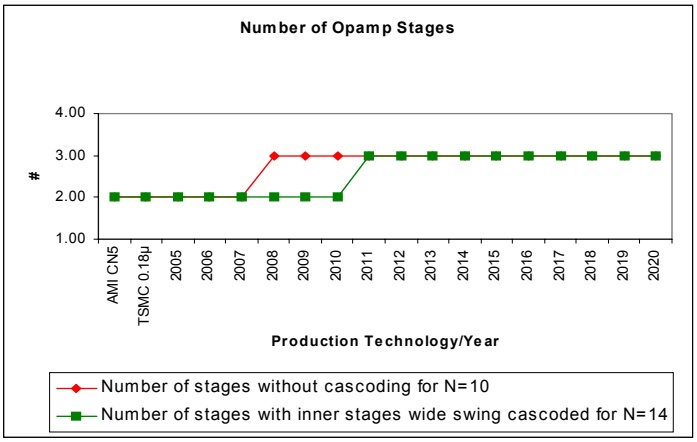

Figure 1-4. Number of stages required to design op-amp with gain required for N bit ADC settling. The figure shows numbers of cascaded stages required without employing any cascoding for 10 bit ADC settling. Also it shows the number of stages required when the internal stages are wide swing cascoded for 14 bit ADC settling [2],[3].

As it can be observed in Figure 1-4, three or higher stage op-amp topologies are going to become a pressing need in the near future if not already. Also there is a growing interest in development of low-voltage and low-power analog circuit techniques for wireless and sensor applications, which operate on batteries or by energy scavenging. As demonstrated later, the low-voltage op-amp topologies can provide the required open loop gain,

only when three or higher number of gain stages are used in the contemporary sub-micron CMOS processes.

Moreover, high-gain, multi-stage op-amps find exhaustive application in high precision flash and pipelined data converters, delta-sigma modulators, cell-phone speaker drivers (which require low harmonic distortion), regulators, sensors and displays [4]. This thesis presents development of novel high-speed, low-voltage, low-power, multi-stage op-amp topologies which tremendously progress the state-of-art. Also the improved op-amp frequency compensation scheme, called indirect feedback compensation, introduced in [1] is amply developed and presented. The indirect feedback compensation, when applied to multi-stage op-amp design solves many problems with the techniques proposed in literature, and enables realization of extremely low-power op-amp topologies.

The rest of the thesis is organized as follows. Chapter 2 provides a background on the compensation for two-stage op-amps and then details the development of indirect feedback compensation technique for two stage op-amps.

Chapter 3 expounds on biasing techniques for multi-stage op-amp. Then a brief background on the contemporary three-stage op-amp design techniques proposed in literature is presented. This is followed by a detail discussion on application of indirect feedback compensation to the three-stage op-amp design. Novel low-power cascaded three-stage op-amp topologies are proposed which provide substantial improvement over the contemporary designs. Finally a generalized theory for design of N-stage, indirect compensated op-amp is proposed.

Chapter 4 presents the application of the multi-stage op-amp design techniques to develop their fully-differential counterparts. The novel multi-stage fully-differential op-amp topologies proposed will facilitate development of low-power, low-voltage data converters and other analog signal processing systems.

Chapter 5 demonstrates the test chips developed for the op-amp topologies proposed in this thesis. Test results for the first fabricated chip are illustrated along with the chip micrographs and layout pictures.

Chapter 6 delineates the conclusions drawn from the work presented in this thesis along with the directions for further research on this topic.

TWO-STAGE OPERATIONAL AMPLIFIER FREQUENCY COMPENSATION

TWO-STAGE op-amps have been the dominant amplifier topologies used in analog system design due their simple frequency compensation and relaxed stability criterions. The two-stage op-amps have conventionally been compensated using *Miller compensation* or Direct Compensation technique. Figure 2-1 the shows block diagram of a two-stage op-amp. The op-amp consists of a diff-amp as the input stage. The second (gain) stage is biased by the output of the diff-amp which is followed by an output buffer. The optional output buffer is used to provide a current gain when driving a large capacitive or resistive load [1].

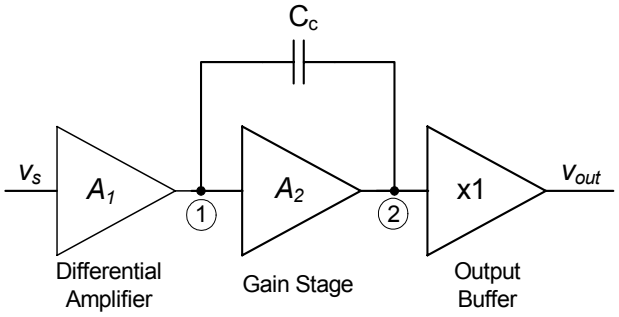

Figure 2-1. Block diagram showing general structure of a two-stage op-amp [1].

Miller Compensation

Before compensation, the poles of the two-stage cascade are given as, $p_1 = \frac{1}{R_1 C_1}$, and $p_2 = \frac{1}{R_2 C_2}$, where R_k, C_k are the resistances and capacitances respectively at nodes

k=1,2. In order to achieve dominant pole stabilization of the opamp, Miller compensation is employed to achieve pole splitting. In this technique, the compensation capacitor (C_c) is connected between the output of the first and second stages. The compensation capacitor splits the input and output poles apart thus obtaining the dominant and non-dominant poles which are spaced far away from each other [1],[6]. However, Miller compensation also introduces a right-half-plane (RHP) zero due to the feed-forward current from the output of the first stage to the op-amp's output. Figure 2-2 shows the small signal model for two-stage opamp used for nodal analysis.

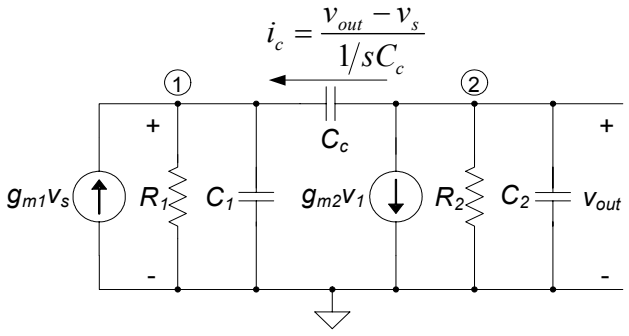

Figure 2-2. Small signal model for nodal analysis of Miller compensation of a two-stage op-amp.

The small signal transfer function for a Miller compensation two-stage opamp is given as,

$$\frac{v_{out}}{v_s} = g_{m1}R_1 g_{m2}R_2 \frac{\left(1 - \frac{s}{z_1}\right)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)} \tag{2.1}$$

The RHP zero is located at

$$z_1 = \frac{g_{m2}}{C_c} \tag{2.2}$$

The dominant pole is located at

$$p_1 = -\frac{1}{g_{m2}R_2R_1C_c} \tag{2.3}$$

and the non-dominant pole is located at

$$p_2 = -\frac{g_{m2}C_c}{C_cC_1 + C_1C_2 + C_cC_2} \approx -\frac{g_{m2}}{C_1 + C_2} \tag{2.4}$$

The open-loop gain of the op-amp is given as $A_v = g_{m1}R_1g_{m2}R_2$, while the unity-gain frequency (or gain-bandwidth) is given as $f_{un} = \frac{g_{m1}}{2\pi C_c}$.

The pole splitting for the two-stage op-amp due to Miller compensation is illustrated in Figure 2-3. The frequency locations corresponding to poles and zeros can be evaluated as $f_{p_k} = \frac{|p_k|}{2\pi}$ and $f_{z_k} = \frac{|z_k|}{2\pi}$ respectively [1].

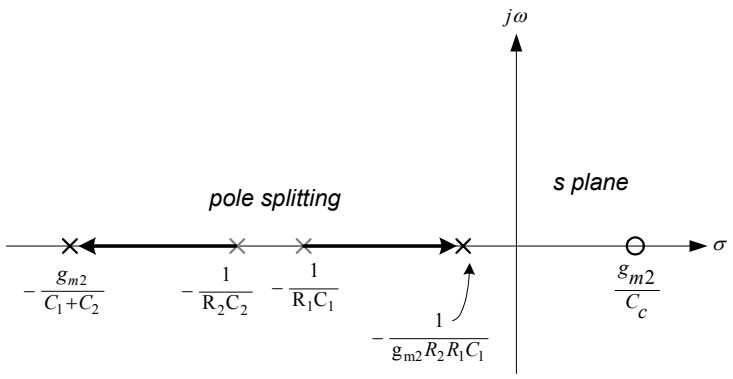

Figure 2-3. Pole-zero plot for a two-stage op-amp demonstrating pole splitting due to the Miller capacitor [1].

Figure 2-4 shows the frequency response of the Miller compensated two-stage op-amp. Since the phase contribution due to the RHP zero is given as $-\tan^{-1}\left(\frac{f}{f_{z1}}\right)$, it degrades phase margin of the op-amp from $90°$ and leads to instability when the second pole moves

closer to the unity-gain frequency (f_{un}). Hence, not only the RHP zero flattens out the magnitude response by cancelling the dominant pole roll-off, which is required to stabilize the op-amp, it also decreases the phase margin which makes the op-amp stabilization difficult [1].

Upon closer analysis of the origin of the RHP zero, the compensation current (i_c), flowing across the compensation capacitor (C_c) from output node to node-1, is given as $i_c = sC_c(v_{out} - v_1) = sC_c v_{out} - sC_c v_1$. The feed-forward component of this current, $i_{ff} = sC_c v_1$, flows from node-1 to the output, and the feed-back component, $i_{fb} = sC_c v_{out}$, flows from the output to node-1. The feed-forward current, i_{ff}, depends upon voltage v_1, and so does the current at the output ($=(g_{m2} - sC_c)v_1$). When the total current at the output equals zero (i.e. frequency corresponding to $z_1=g_{m2}/C_c$), a RHP zero appears in the transfer function. This RHP zero can be eliminated by blocking the feed-forward compensation current, while allowing the feed-back component of the compensation current to achieve pole splitting [6].

Several methods have been suggested in [1] and [6] to cancel the RHP zero in the two-stage op-amp and are described in the following sub-sections.

A Miller compensated two-stage op-amp has been implemented on the test chip with schematic as shown in Figure 2-5. The op-amps on the test chip have been designed to drive a typical load of 30pF, which is presented by the probe cables in the test setup. The test chip is designed using MOSIS's AMI C5N 0.5um process and serves as a platform to

compare the performance of various op-amp topologies discussed in this chapter. Specific details on chip layout and testing are presented later in chapter 5.

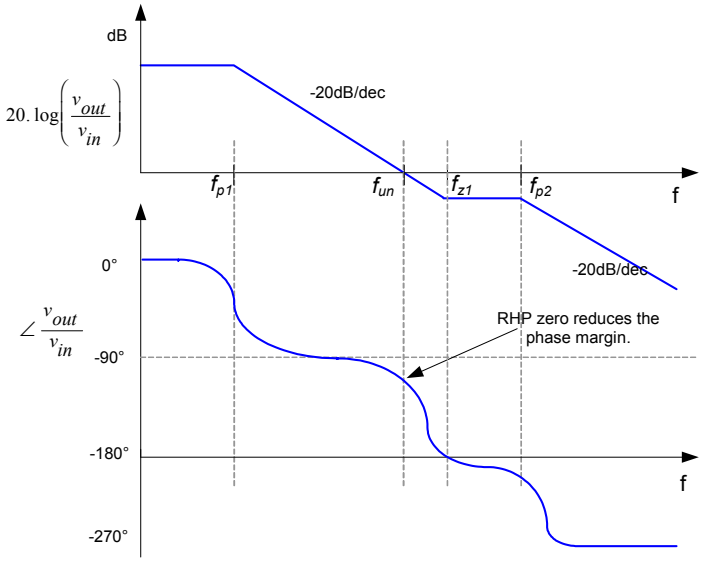

Figure 2-4. Frequency response of the Miller compensation two-stage op-amp[6].

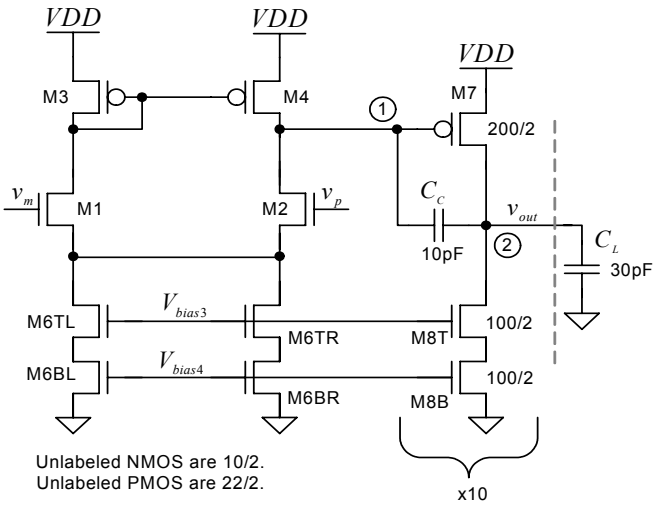

Figure 2-5. A Miller compensated two-stage op-amp designed on the test chip.

The op-amps have been designed for high speed with an overdrive equal to 5% of the VDD and use minimum length devices i.e. L=2. Table 2-1 summarizes the transistor parameters for the selected biasing and device sizes.

The designed op-amps can be biased using a beta-multiplier reference (BMR) circuit shown in Figure 2-6 and the cascoding bias voltages are generated using the wide-swing cascoding circuit shown in Figure 2-7. A detailed explanation on the working of these biasing circuits is provided in [1].

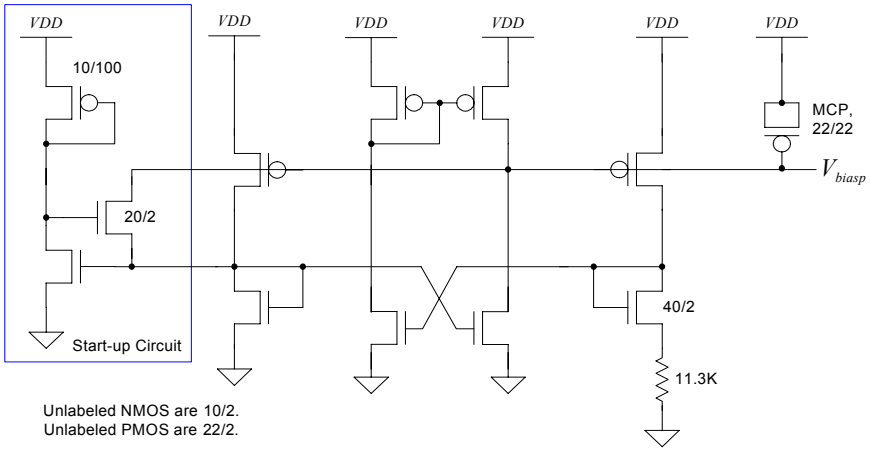

Figure 2-6. The self-biased beta multiplier reference (BMR) circuit for biasing the op-amps.

Table 2-1. AMI C5N process MOSFET parameters for the op-amp designs introduced in this work.

Mosfet parameter for design with VDD=5V and a scale factor of 300nm (scale=300nm).			
Parameter	NMOS	PMOS	Comments
Bias Current, I_D	20μA	20μA	Selected in order to drive 30pF load.
W/L	10/2	22/2	Selected based on I_D and V_{ov}
Actual W/L	3μm/600nm	6.6μm/600nm	Minimum L is 600nm.
$V_{DS,sat}$ and $V_{SD,sat}$	150mV	140mV	Saturation voltages. The point where output resistance starts to decrease.
V_{ovn} and V_{ovp}	350mV	350mV	7% voltage overdrive.
V_{GS} and V_{SG}	1V	1.185V	Bias voltages.
V_{THN} and V_{THP}	650mV	835mV	Threshold voltages.
$\partial V_{TH(N,P)}/(\partial T)$	$-0.7\text{mV}/°\text{C}$	$-0.7\text{mV}/°\text{C}$	Temperature coefficients.
v_{satn} and v_{satp}	$193\times10^3\,\text{ms}^{-1}$	$152\times10^3\,\text{ms}^{-1}$	Saturation velocity, from BSIM model.
t_{ox}	14.1nm	14.1nm	Gate Oxide thickness, from BSIM model.
$C'_{ox} = \varepsilon_{ox}/t_{ox}$	$2.51\ \text{fF}/\mu\text{m}^2$	$2.51\ \text{fF}/\mu\text{m}^2$	Gate Oxide capacitance.
C_{oxn} and C_{oxp}	1.13 fF	2.49 fF	$C_{ox} = C'_{ox}WL(\text{scale})^2$
C_{gsn} and C_{sgp}	0.754 fF	1.66 fF	$C_{gs} = (2/3)C_{ox}$
C_{gdn} and C_{dgp}	0.642 fF	1.41 fF	C_{gd}=CGDO.W.scale
g_{mn} and g_{mp}	168 μA/V	160 μA/V	For I_D=20μA
r_{on} and r_{op}	249 KΩ	272 KΩ	Approx. at I_D=20μA
$g_{mn}r_{on}$ and $g_{mp}r_{op}$	41.83 V/V	43.52 V/V	Open circuit gain.
λ_n and λ_p	0.024	0.023	L=2
f_{Tn} and f_{Tp}	7.1 GHz	3.6 GHz	Transition frequency for L=2.

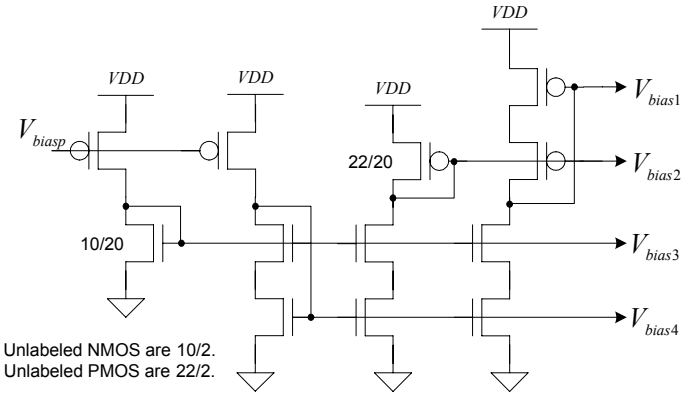

Figure 2-7. The wide-swing cascoding circuit to generate the bias voltages for the op-amp.

Figure 2-8 shows the wide-swing cascode bias reference levels generated by the circuit shown in Figure 2-7.

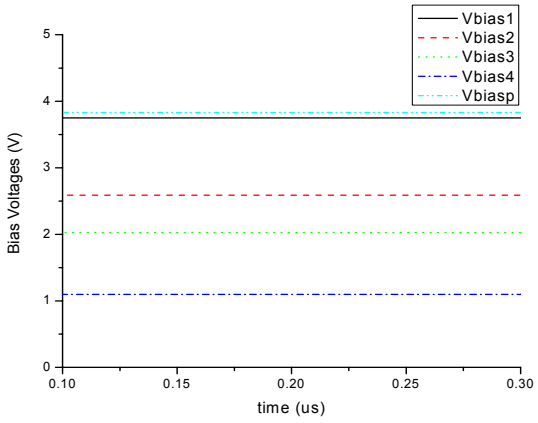

Figure 2-8. Wide swing cascode bias voltages for the designed two-stage op-amps.

The simulation results for the Miller compensated op-amp are shown in Figure 2-9.

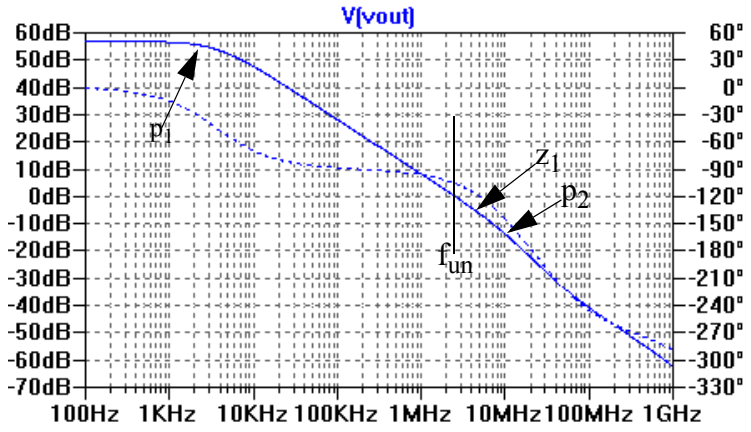

Figure 2-9. Frequency response of the Miller compensated two-stage op-amp. Here f_{un}=2.5MHz and PM=75° . In this and all the subsequent SPICE simulated frequency response plots, the solid and dotted lines represent the transfer function magnitude and phase respectively.

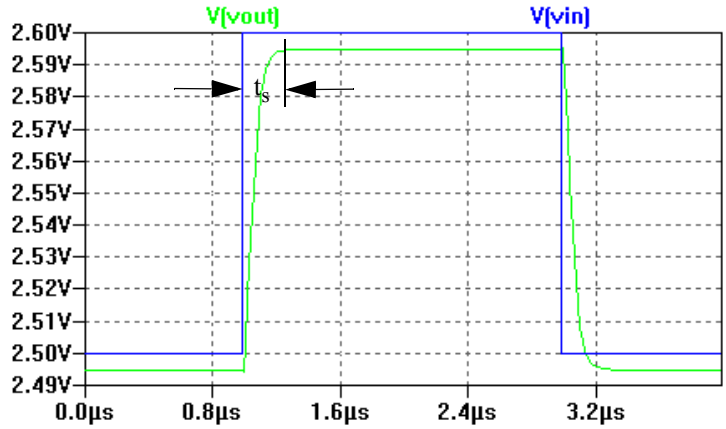

Figure 2-10. Small step input response of the Miller compensated two-stage op-amp. Here the settling time (t_s) is approximately equal to 350ns.

As the gain-bandwidth product or the unity-gain frequency is a Figure of Merit (FoM) of the designed op-amp in frequency domain, the settling time is a FoM for the time domain characteristics of the op-amp. For an op-amp with 90° phase margin with non-

dominant poles and zeros being far away from f_{un} (i.e. an R-C circuit like response), the relation between 99.9% settling time (t_s) and f_{un} is given as

$$t_s = \frac{0.35}{f_{un}} \tag{2.5}$$

Table 2-2 lists the required unity-gain frequency to achieve the target op-amp settling times for an op-amp with 90° phase margin.

Table 2-2. Required Op-amp unity-gain frequency for settling time specifications.

Settling time (t_s)	unity-gain frequency (f_{un})
1ns	350MHz
10ns	35MHz
100ns	3.5MHz
1μs	350KHz
10μs	35KHz
1ms	350Hz

The following sub-sections discuss methods widely used to eliminate the detrimental effects of the RHP zero on the phase margin in the Miller compensated op-amps.

Zero Nulling Resistor

A common method to cancel the RHP zero is to use a zero nulling resistor in series with the compensation capacitance, as shown in Figure 2-11. With the zero nulling resistor (R_z), the location of the zero is given as

$$z_1 = \frac{1}{\left(\frac{1}{g_{m2}} - R_z\right)C_c} \tag{2.6}$$

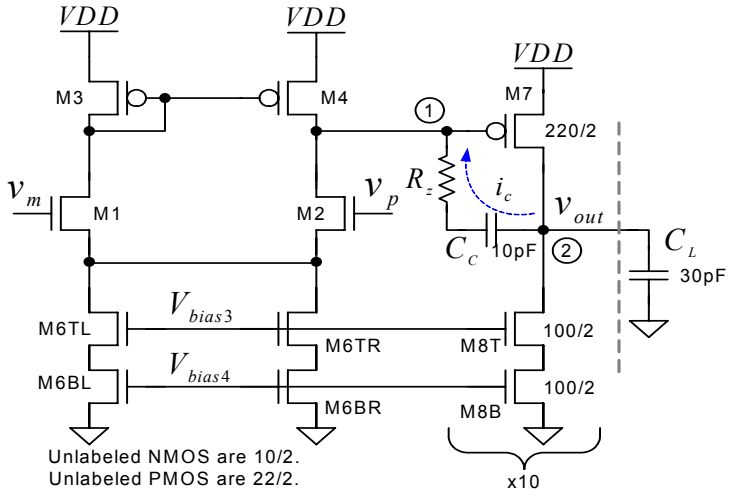

Figure 2-11. Miller compensated op-amp with zero nulling resistor, R_z=750Ω [1].

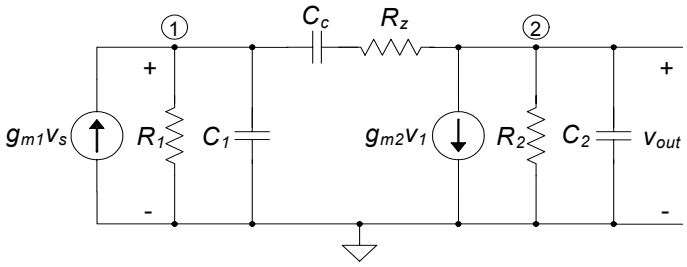

Figure 2-12. Small signal model for a Miller compensated op-amp with a zero nulling resistor.

For $R_z=1/g_{m2}$, the zero is pushed to infinity and for $R_z>1/g_{m2}$, the zero appears in the left half plane (LHP). Thus for $R_z=2/g_{m2}$, the RHP zero is converted to an LHP zero of the same frequency location as that of the RHP zero. A LHP zero helps in improving the phase margin of the opamp and enhances stability. Nodal analysis on the model in Figure 2-

12 leads to the locations of the poles and zeros. The first and second poles are at the same location as in the Miller compensation case, i.e. $p_1 = -\frac{1}{g_{m2}R_2R_1C_c}$ and $p_2 \approx -\frac{g_{m2}}{C_1 + C_2}$.

A third pole is introduced at $p_3 \approx -\frac{1}{R_zC_1}$ which is far away from the second pole, p_2, as $C_1 \ll C_2$ and $R_z \approx \frac{1}{g_{m2}}$ [6]. The location of the zero may vary depending upon the process variations in the resistor R_z, but this scheme is effective enough to keep the RHP zero from degrading the phase margin. The resistor R_z can be implemented using a transistor in triode region, and can be made to track the value of $1/g_{m2}$ and cancel the RHP zero. However the biasing of this triode transistor may require additional power [1].

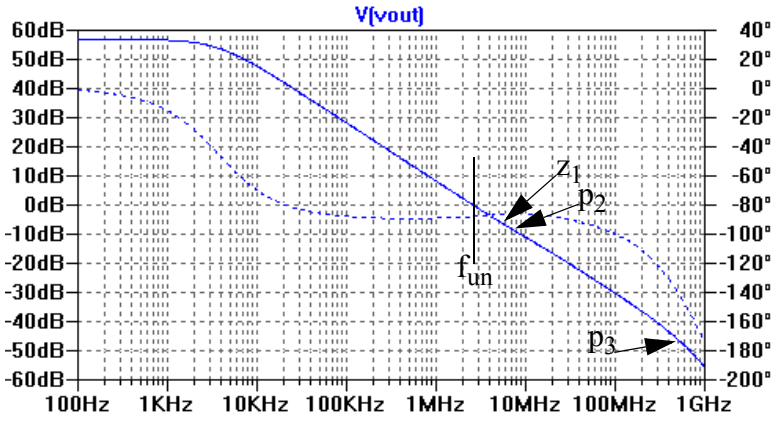

Figure 2-13. Frequency response of the Miller compensated two-stage op-amp with zero nulling resistor Here, f_{un}=2.6MHz and PM=89°.

The small signal frequency response for this circuit is shown in Figure 2-13, while Figure 2-14 displays the step input response of the op-amp. Here we can observe the improvement in phase margin (PM) from 75° to 89° by using the zero nulling resistor.

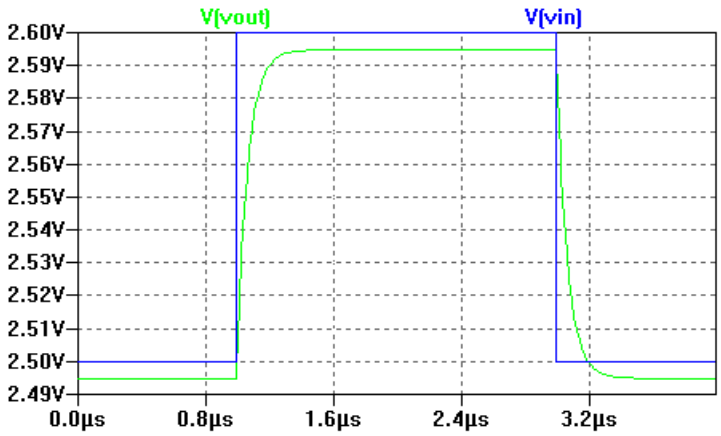

Figure 2-14. Small step input response of the Miller compensated two-stage op-amp with zero nulling resistor. Here ts = 300ns.

Voltage Buffer

A source follower can be used to block the feedforward compensation current and allow the feedback compensation current to flow from the output to the node-1. Figure 2-15 shows an op-amp topology with an NMOS source follower while Figure 2-16 shows the op-amp with a PMOS source follower. Notice the way the compensation current is fed back from the output to the node-1 in these op-amps. These topologies eliminates the RHP zero although at the cost of additional power and transistors. Also due to the use of a source follower, there exists a fixed DC voltage drop, equal to V_{GS} (or V_{SG} for the PMOS buffer case) in the feedback signal path. This voltage drop reduces the output swing, as a high output swing may triode the source follower device and break down the compensation. The location of the first pole remains the same as in the case of Miller compensation, and the second pole also remains relatively unchanged at $p_2 \approx -\frac{g_{m2}}{C_2}$ [6].

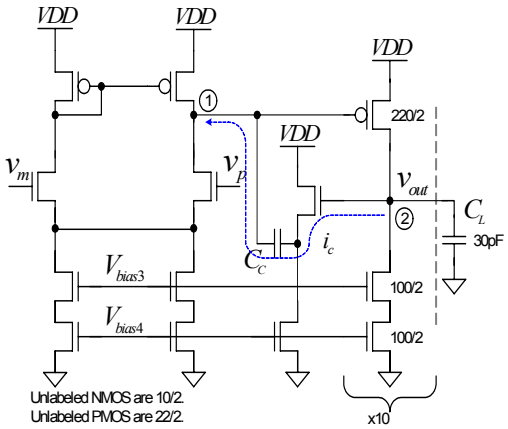

Figure 2-15. Op-amp with an NMOS Voltage Buffer.

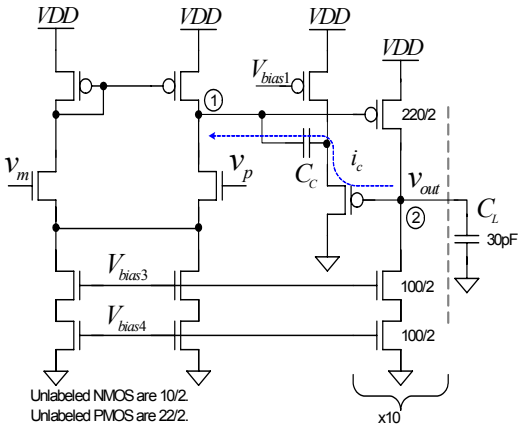

Figure 2-16. Op-amp with a PMOS Voltage Buffer.

Common-Gate Stage

A common-gate stage can also be used to block the feedforward current from node-1 to the output node-2 [8]. Figure 2-17 shows a two-stage op-amp which is indirect compensated using a common-gate stage. The transistor M_{CG} acts as a common-gate amplifier which blocks the feed-forward compensation current and allows the feedback compensation current to flow indirectly from the output to the internal node-1. Such topologies are analyzed in the next section, and they significantly improve the performance of the op-amps designed. As the compensation current is fed back indirectly from the node-2 (i.e. output node) to the node-1 in order to achieve pole splitting (and hence dominant pole compensation), the class of compensation technique is called *Indirect Feedback Frequency*

Compensation or simply indirect compensation. An analysis of the common-gate stage indirect compensated op-amp topology is provided in the next section.

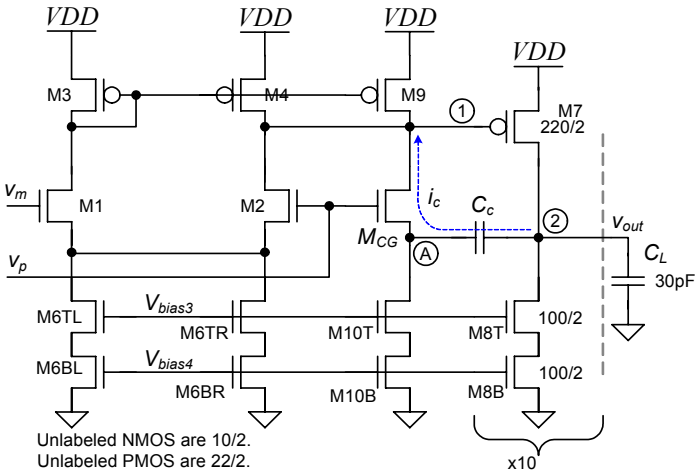

Figure 2-17. A two-stage op-amp with a common-gate stage to feedback the compensation current.

Indirect Feedback Frequency Compensation

As introduced in the last section, the class of compensation in which the compensation current is fed back indirectly from the output to the internal high impedance node, is called *Indirect Feedback Frequency Compensation*. Here, the compensation capacitor is connected to an internal low impedance node in the first stage, which allows an indirect feedback of the compensation current from the output node-2 to the internal high impedance node-1. Figure 2-18 shows the block diagram of an indirect feedback compensated two-stage opamp. Here, the effective small signal resistance attached to the low impedance node is denoted as R_c.

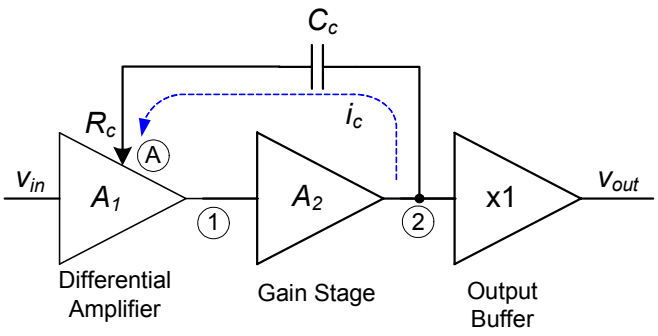

Figure 2-18. Block diagram of an indirect feedback compensated two-stage op-amp. The compensation current is indirectly fed to the high impedance node-1 from the output node. The compensation capacitor, C_c, is connect between the output and an internal low impedance node in the first stage. The effective resistance attached to the low-Z node is denoted as R_c.

Exact Analysis

In order to develop an insight into indirect feedback compensation, the op-amp topology indirectly compensated with common-gate stage is analyzed. The small signal model for the common-gate stage op-amp topology is shown in Figure 2-19 [7].

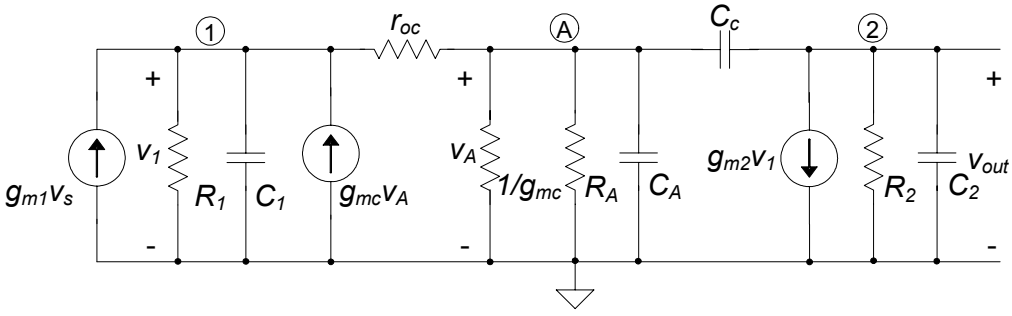

Figure 2-19. Small signal analytical model for common-gate stage indirect compensated two-stage op-amp [7].

The model used for exact analysis has three nodes and hence three dependent variables, v_1,v_A and v_{out}. Also in the model $v_s = v_p - v_m$. A T-type small signal model is used to represent the common-gate device M_{CG} [6]. Here, the transconductance and output resistance of the common-gate device (M_{CG}) are denoted as g_{mc} and r_{oc} respectively. Also R_A and C_A are the resistance and capacitance at the low impedance node-A. On applying nodal analysis on the model shown in Figure 2-21, we obtain the following set of equations [7].

$$-g_{m1}v_s + \frac{v_1}{R_1} + v_1 sC_1 - g_{mc}v_a + \frac{(v_1 - v_A)}{r_{oc}} = 0 \tag{2.7}$$

$$g_{m2}v_1 + \frac{v_{out}}{R_2} + v_{out}sC_2 + sC_c(v_{out} - v_A) = 0 \tag{2.8}$$

$$\frac{(v_A - v_1)}{r_{oc}} + g_{mc}v_A + v_A sC_A + \frac{v_A}{R_A} + sC_c(v_A - v_{out}) = 0 \tag{2.9}$$

On simultaneously solving Equations 2.7, 2.8 and 2.9, we obtain the following small signal transfer function.

$$\frac{v_{out}}{v_s} = -A_v\left(\frac{b_0 + b_1 s}{a_0 + a_1 s + a_2 s^2 + a_3 s^3}\right) \tag{2.10}$$

The third order transfer function given by Equation 2.10 consists of a real LHP zero and three poles. The exact values of the transfer function coefficients are

$$A_v = g_{m1}R_1 g_{m2}R_2 \tag{2.11}$$

$$b_0 = (1 + g_{mc}R_A)r_{oc} + R_A \tag{2.12}$$

$$b_1 = R_A[r_{oc}(C_c + C_A) + g_{mc}r_{oc} - C_c/g_{m2}] \tag{2.13}$$

$$a_0 = (1 + g_{mc}R_A)r_{oc} + R_A + R_1 \tag{2.14}$$

$$\begin{aligned} a_1 = {} & g_{m2}R_2g_{mc}R_1r_{oc}C_cR_A + g_{m2}R_2R_1C_cR_A \\ & + g_{mc}R_Ar_{oc}(R_1C_1 + R_2(C_2 + C_c)) + R_1R_A(C_c + C_A) \\ & + R_A(R_1C_1 + R_2C_2) + R_1R_2(C_2 + C_c) + r_{oc}(R_2C_c + R_A(C_c + C_A)) \end{aligned} \tag{2.15}$$

$$\begin{aligned} a_2 = {} & (g_{mc}R_A + 1)R_2C_1R_1r_{oc}(C_2 + C_c) + R_2r_{oc}R_AC_c(C_2 + C_A) \\ & + R_1R_2C_cR_AC_A + R_2C_2R_A(R_1(C_1 + C_c + C_A) + r_{oc}C_A) \\ & + R_1C_1R_A(r_{oc}(C_c + C_A) + R_2C_2) \end{aligned} \tag{2.16}$$

$$a_3 = R_1C_1R_2r_{oc}R_A(C_2C_A + C_2C_c + C_cC_A) \tag{2.17}$$

Applying the approximations $g_{mk}R_k \gg 1$, $C_2 \approx C_L; C_c$, $C_2 \gg C_1, C_A$, we obtain the following modified transfer function coefficients,

$$b_0 \approx g_{mc}R_Ar_{oc} \tag{2.18}$$

$$b_1 \approx R_Ar_{oc}(C_c + C_A) \tag{2.19}$$

$$a_0 \approx (g_{mc}R_A + 1)r_{oc} \tag{2.20}$$

$$a_1 \approx g_{m2}R_2R_1r_{oc}C_c(g_{mc}R_A + 1) \tag{2.21}$$

$$\begin{aligned} a_2 \approx {} & (g_{mc}R_A + 1)R_2C_1R_1r_{oc}(C_2 + C_c) \\ & + R_2C_2R_A[r_{oc}(C_c + C_A) + R_1(C_c + C_A + C_1)] \end{aligned} \tag{2.22}$$

$$a_3 \approx R_1C_1R_2r_{oc}R_A(C_2C_A + C_2C_c + C_cC_A) \tag{2.23}$$

Using the numerator expression, we obtain the location of the zero to be at

$$z_1 \approx -\frac{b_0}{b_1} = -\frac{g_{mc}}{C_c + C_A} \tag{2.24}$$

which is evidently an LHP zero. With the assumption that $|p_1| \gg |p_2|, |p_3|$, the dominant real pole is given as

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m2}R_2R_1C_c} \tag{2.25}$$

Now for $s \gg p_1$, the denominator of the transfer function, D(s), can be approximated as

$$D(s) \approx \left(1 - \frac{s}{p_1}\right)\left(1 + \frac{a_2}{a_1}s + \frac{a_3}{a_1}s^2\right) \tag{2.26}$$

From Equation 2.26, the non-dominant poles p_2 and p_3 are real and spaced wide apart when $\left(\frac{a_2}{a_1}\right)^2 \gg 4\left(\frac{a_3}{a_1}\right)$, or

$$(a_2)^2 \gg 4a_3a_1 \tag{2.27}$$

The above condition is satisfied when

$$g_{mc} \gg \frac{4g_{m2}C_c(C_2 \parallel C_c + C_A)}{C_1(C_2 + C_c)} \tag{2.28}$$

This implies that the g_m of the common-gate device (M_{CG}) in Figure 2-17 should be large. When the condition given by Equation 2.28 is satisfied, the non-dominant poles are given as

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2}C_c}{C_1(C_c + C_2)} \approx -\frac{g_{m2}C_c}{C_1C_L}, \text{ and} \tag{2.29}$$

$$\begin{aligned} p_3 \approx -\frac{a_2}{a_3} &= -\frac{g_{mc}}{(C_A + C_2 \parallel C_c)} - \frac{C_2/C_1}{R_1 \parallel r_{oc}(C_2 + C_c \parallel C_c)} \\ &\approx -\left[\frac{g_{mc}}{C_2 \parallel C_c} + \frac{1}{(R_1 \parallel r_{oc})C_1}\right] \end{aligned} \tag{2.30}$$

The unity-gain frequency of the op-amp is given as

$$f_{un} = \frac{|p_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_c} \tag{2.31}$$

From Equation 2.29 the second pole, when using indirect compensation, is located at $-\frac{g_{m2}C_c}{C_L C_1}$ while the second pole for Miller (or direct) compensation was located at $-\frac{g_{m2}}{C_1 + C_L}$. By comparing the two expressions, we can observe that the second pole, p_2, has moved further away from the dominant pole by a factor of approximately C_c/C_1. This factor of C_c/C_1 comes to be around 10's in AMI C5N 0.5µm process employed in this thesis work. Also the LHP zero adds to the phase response in the vicinity of f_{un}, and enhances the phase margin.

This implies that we can achieve pole splitting with a much lower value of compensation capacitor (C_c) and lower value of second stage transconductance (g_{m2}). Lower value of g_{m2} translates into low power design as the bias current in second stage can be much lower. Alternatively, we can set higher value of unity-gain frequency (f_{un}) for the op-amp without affecting stability and hence achieving higher bandwidth and speed. Moreover, the load capacitor can be allowed to be much larger for a given phase margin [1],[9], [10]. The higher value of $|p_2|$ can be explained by the fact that the first stage's output (i.e. node-1) is not loaded by the compensation capacitor [6]. In short, in can be trivially concluded that indirect feedback compensation can lead to the design of op-amps with significantly lower power, higher speed and lower layout area.

Also on observing Equation 2.30, the third pole (p_3) doesn't move to lower frequency and interact with the second pole (p_2) as long as g_{mc} is large and $R_{1,}C_1$ are smaller in value. In modern sub-100nm processes, the values of R_1 and C_1 are much smaller than in the long channel processes and the third pole doesn't affect the stability as much.

Looking at the case when the non-dominant poles are close and form a conjugate pole pair when

$$g_{mc} < \frac{4g_{m2}C_c(C_2 \parallel C_c + C_A)}{C_1(C_2 + C_c)} \tag{2.32}$$

The real part of the conjugate pole pair ($p_{2,3}$) is given as

$$\mathrm{Re}(p_{2,3}) = -\sqrt{\frac{a_1}{a_3}} = -\sqrt{\frac{g_{m2}g_{mc}}{C_1[C_2 + (1 + C_2/C_c)C_A]}} \approx \sqrt{\frac{g_{m2}g_{mc}}{C_1C_2}} \tag{2.33}$$

and the damping factor (ξ) is given as

$$\xi = \frac{a_2}{2\sqrt{a_1a_3}} \approx \frac{1}{2C_c}\sqrt{\frac{C_1C_2}{g_{m2}}} \tag{2.34}$$

Also, we can observe that

$$\left|\mathrm{Re}(p_{2,3})\right| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mc}C_L}{g_{m2}C_1}} > \frac{g_{m2}}{C_L} \tag{2.35}$$

which again re-affirms the fact that the values of $1/g_{mc}$ and C_1 should be small in order to move $p_{2,3}$ away from p_1 as farther as possible.

Simplified Analytical Model

In the preceding section, a detailed analysis for indirect compensation using a common-gate stage was presented. However, a simpler analytical model for indirect compensation will be of greater utility in analyzing more complex topologies employing indirect compensation. Figure 2-20 shows the sequence of deriving a simpler analytical model

for indirect compensation. In the Figure 2-20 (b), node-1 and node-A are de-coupled using the assumption that the resistance r_{oc} is large and the variation in node voltage v_A is less. Figure 2-20c is obtained by using the Norton equivalent of the voltage source v_A.

Figure 2-20 (d) shows the simplified analytical model with only two dependent nodes 1 and 2. Now since $g_{mc} \gg \frac{1}{r_{oc}}, \frac{1}{R_A}$ and $C_c \gg C_A$, the feedback compensation current can be approximated as

$$i_c \approx \frac{v_{out}}{R_c + \frac{1}{sC_c}} \tag{2.36}$$

and the impedance Z_c can be approximated as $1/g_{mc}$ for frequencies less than the f_T of the transistors used in the topology, and thus neglecting the $\frac{1}{sC_A}$ term. These simplifying assumptions lead to the model shown in Figure 2-21. In the model here, $R_c = \frac{1}{g_{mc}} \| R_A$ is the resistance attached to node-A.

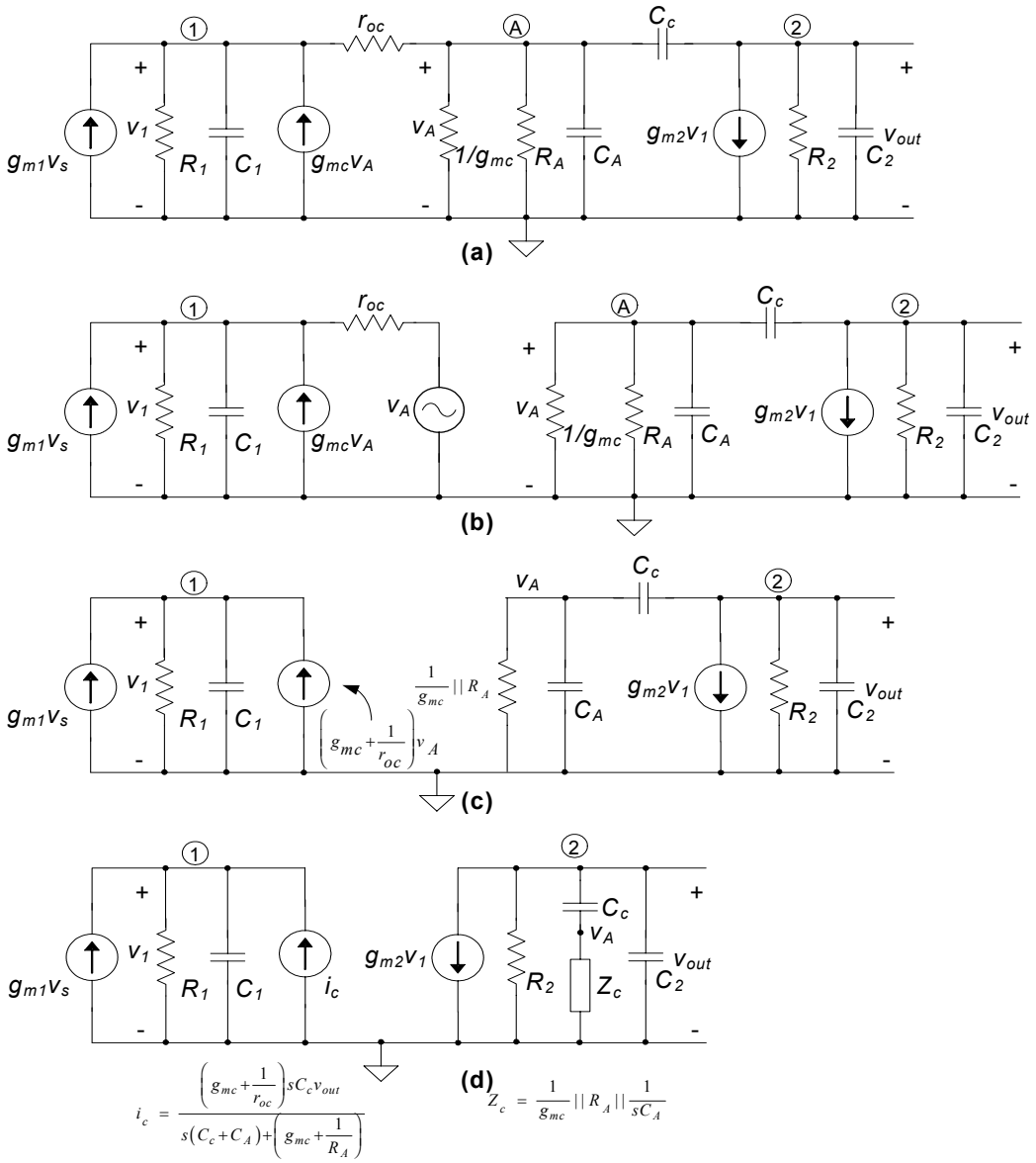

Figure 2-20. Derivation of a simpler analytical model for indirect compensation by making appropriate simplifying assumptions.

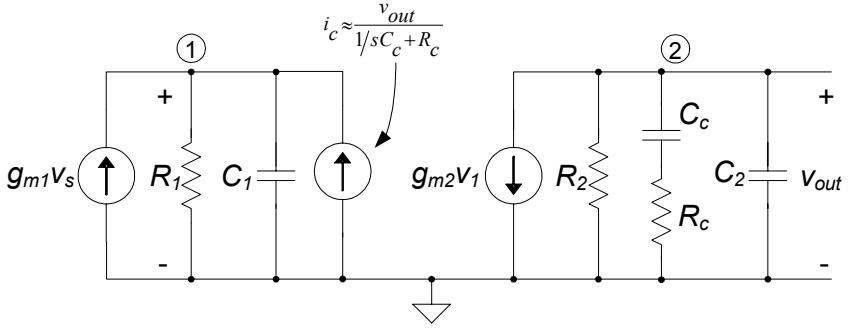

Figure 2-21. Simplified analytical model for indirect feedback compensation of two-stage op-amps.

We can employ nodal analysis to derive the and verify the pole and zero locations corresponding to the simplified model presented in Figure 2-21. The nodal analysis equations for this model are

$$-g_{m1}v_s + \frac{v_1}{R_1} + sC_1v_1 - \frac{v_{out}}{1/sC_c + R_c} = 0 \tag{2.37}$$

$$g_{m2}v_1 + \frac{v_{out}}{R_2} + \frac{v_{out}}{1/sC_c + R_c} + sC_2v_{out} = 0 \tag{2.38}$$

On solving Equations 2.37 and 2.382.38, we obtain the following small signal transfer function.

$$\frac{v_{out}}{v_s} = -A_v\left(\frac{1 + b_1s}{1 + a_1s + a_2s^2 + a_3s^3}\right) \tag{2.39}$$

The third order transfer function given by Equation consists of a real zero and three poles. The exact values of the transfer function coefficients are

$$A_v = g_{m1}R_1 g_{m2}R_2 \tag{2.40}$$

$$b_1 = R_c C_c \tag{2.41}$$

$$a_1 = g_{m2}R_2 g_{mc}R_c R_1 C_c + R_1 C_1 + R_2 C_2 + R_2 C_c + R_c C_c \tag{2.42}$$

$$a_2 = R_1 C_1 (R_2 + R_c) C_c + R_2 C_2 (R_1 C_1 + R_c C_c) \tag{2.43}$$

$$a_3 = R_1 C_1 R_2 C_2 R_c C_c \tag{2.44}$$

Applying the approximations $g_{mk}R_k \gg 1, k = 1, 2; C_2 \approx C_L; C_c, C_2 \gg C_1$, we obtain the location of the zero and poles.

The LHP zero location is given as

$$z_1 \approx -\frac{1}{R_c C_c} \tag{2.45}$$

The dominant real pole is located at

$$p_1 \approx -\frac{1}{a_1} = -\frac{1}{g_{m2}R_2 R_1 C_c} \tag{2.46}$$

The non-dominant poles, p_2 and p_3, are real and spaced wide apart when

$$G_c = \frac{1}{R_c} \gg \frac{4g_{m2}C_c^2}{C_1 C_2} \tag{2.47}$$

which implies that the resistance, R_c, should be small or, in other words, G_c should be very large. When the condition given by Equation 2.47 is satisfied, the non-dominant poles are given as

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2}R_1 C_c}{C_2(R_c C_c + R_1 C_1)} \approx -\frac{g_{m2}C_c}{C_L C_1}, \text{ and} \tag{2.48}$$

$$p_3 \approx -\frac{a_2}{a_3} = -\left[\frac{1}{R_c C_c} + \frac{1}{R_1 C_1}\right] \tag{2.49}$$

The unity-gain frequency of the op-amp is

$$f_{un} = \frac{|p_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_c} \tag{2.50}$$

By comparing Equations 2.24-2.31 with Equations 2.45-2.50, the simplified model shown in Figure 2-21 represents indirect feedback compensation with reasonable accuracy.

It can be observed that as $R_c \to 0$ (i.e $G_c \to \infty$,) $|p_3| \to \infty$ and $|z_1| \to \infty$. Then the op-amp transfer function has only two real poles and the phase margin is $90°$.This again leads to the limiting condition when the g_m of the common-gate stage (seen in Figure 2-17) is very large.

The following sub-sections illustrate the application of the generalized indirect feedback compensation theory to specific indirect compensated op-amp topologies.

Common-gate Stage

An elaborate procedure for designing two-stage op-amps using a current buffer (common-gate stage) is available in [11]. In designs such as in [11], the location of the zero is manipulated to cancel either of the poles (p_2 or p_3) in order to achieve better phase margin. Since a perfect pole-zero cancellation is hard to achieve with process and temperature variations, such attempts lead to a pole-zero doublet in the frequency response. Even so the frequency response due to a pole-zero doublet is approximately the same as the pole-zero cancelled frequency response. A p_2-z_1 doublet is obtained by setting $g_{mc} = \frac{g_{m2}C_c^2}{C_1C_2}$, and a p_3-z_1 doublet is obtained by using $g_{mc} = \frac{R_cC_c + R_1C_1}{R_cR_1C_1}$.

However, such designs lead to higher power consumption as they try to move the LHP zero higher in frequency and cancel either of the poles, p_2 or p_3, by using higher values of g_{mc}.

Cascoded Loads

Cascoded op-amps have traditionally been used to achieve high open-loop gain with two gain stages. When using a cascoded diff-amp as the first stage, a low impedance internal node is easily realized. This low impedance node can be used for indirect compensation of the op-amp by connecting the compensation capacitor to that node. Figure 2-22 shows a two-stage op-amp with a cascoded current mirror load.

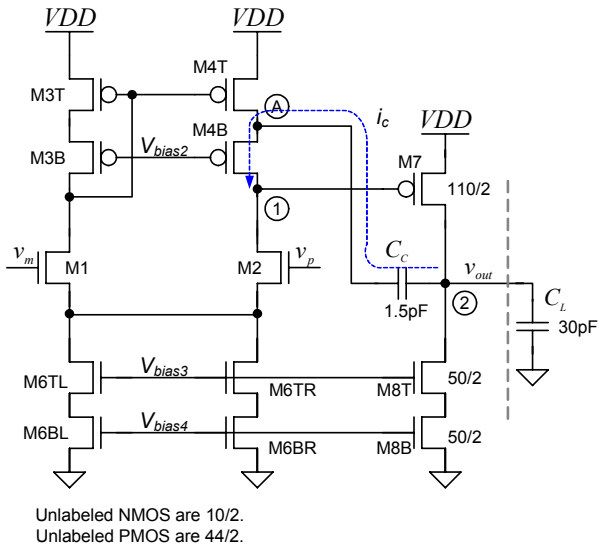

Figure 2-22. A two-stage opamp with a cascoded current mirror load in the first stage.The compensation capacitor is connected to the low impedance node-A.

Here, in this topology the common-gate stage is ‘embedded’ in the current mirror load itself as denoted in [7]. The small signal model for this topology is analogous to the one shown in Figure 2-19 and the LHP zero and the two pole locations are given by Equations 2.24-2.31. Here g_{mc} is equivalent to the g_m of M4B transistor seen in Figure 2-16, which emulates the common-gate device. The cascoded load indirect compensation topologies result in reduction in power when compared to the common-gate topology in Figure 2-17. However the reduction in power comes at a cost of reduced flexibility in choosing the value of g_{mc}, and hence the location of the LHP zero [7]. The small signal frequency response for this op-amp topology is shown in Figure 2-23.

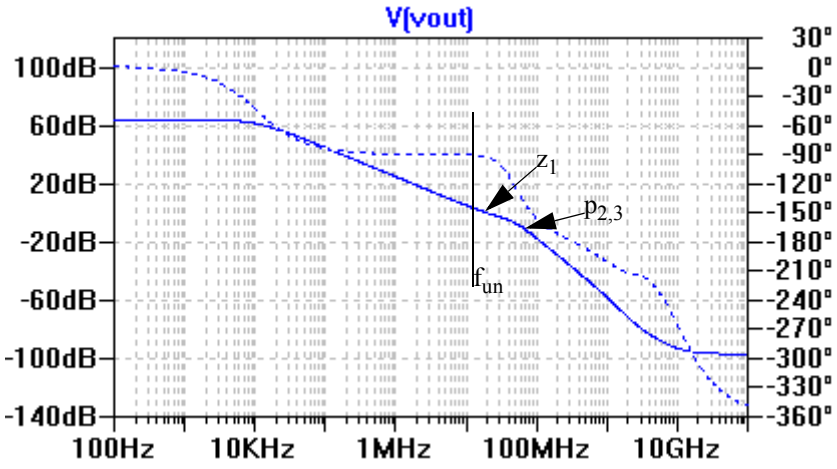

Figure 2-23. Small signal frequency response for the op-amp with indirect compensation using cascoded load. Here, f_{un}=12MHz and PM=86° .

Cascoded Differential Stage

Other than using a cascoded current mirror load, a cascoded differential pair can also be used in op-amp designs. Figure 2-24 shows a two-stage op-amp with a cascoded differential pair. Here the device M2T acts as an 'embedded' common-gate device [7]. The source of M2T is a low impedance node which can be used for feeding back the compensation current. However, the indirect compensation using cascoded differential pair is not same as using the embedded common-gate in cascoded load. Here the node-A has a finite signal swing proportional to the input, which feeds forward through C_c to the output. This leads to a Miller compensation like situation along with indirect compensation as the embedded common-gate device is not isolated from the input, as in the model in Figure 2-19. The feedforward compensation current path can only be eliminated if all the current from the source of M2T is forced to pass through M2T and is not allowed to flow through C_c. This can be only achieved when transconductance of M2T is infinite [7].

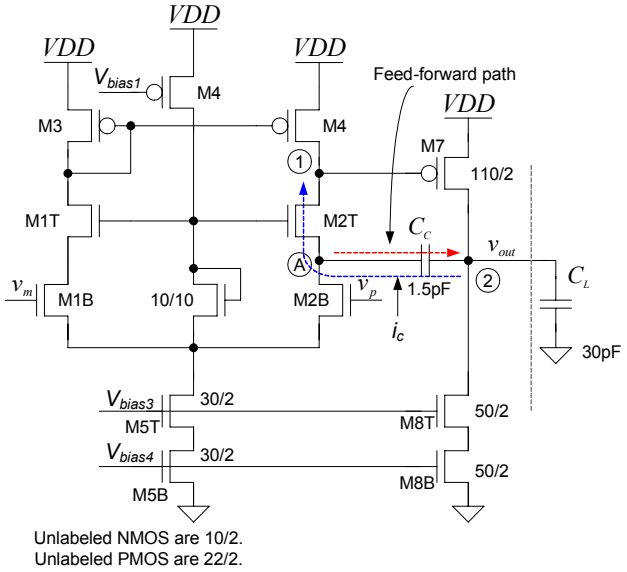

Figure 2-24. A two-stage opamp with a cascoded differential pair in the first stage.The compensation capacitor is connected to the low impedance node-A.

Figure 2-25 shows the small signal model for analysis of the op-amp shown in Figure 2-24.

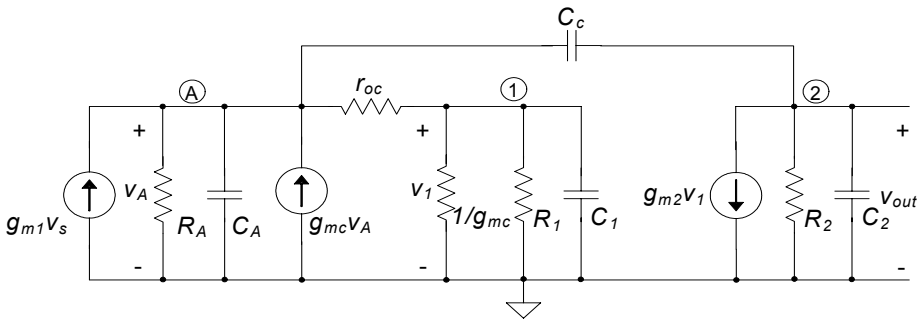

Figure 2-25. Small signal analytical model for the op-amp with indirect compensation using cascoded diff-pair[7].

On applying nodal analysis on the model shown in Figure 2-25, we obtain the following set of equations [7]

$$-g_{m1}v_s + \frac{v_A}{R_A} + v_A sC_A + g_{mc}v_a + \frac{(v_A - v_1)}{r_{oc}} + sC_c(v_A - v_{out}) = 0 \tag{2.51}$$

$$-g_{mc}v_A + v_1 sC_1 + \frac{v_1}{R_1} + \frac{(v_1 - v_A)}{r_{oc}} = 0 \tag{2.52}$$

$$g_{m2}v_1 + \frac{v_{out}}{R_2} + v_{out}sC_2 + sC_c(v_{out} - v_A) = 0 \tag{2.53}$$

On solving Equations 2.51, 2.53 and 2.52, we obtain the following small signal transfer function.

$$\frac{v_{out}}{v_s} = -A_v\left(\frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2 + a_3 s^3}\right) \tag{2.54}$$

with the coefficients given as

$$A_v = g_{m1}R_1 g_{m2}R_2 \tag{2.55}$$

$$b_0 = (1 + g_{mc}r_{oc})R_A \tag{2.56}$$

$$b_1 = -(R_A C_c(r_{oc} + R_1))/(g_{m2}R_1) \tag{2.57}$$

$$b_2 = -(R_A r_{oc} C_c C_1)/g_{m2} \tag{2.58}$$

$$a_0 = (1 + g_{mc}R_A)r_{oc} + R_A + R_1 \tag{2.59}$$

$$\begin{aligned} a_1 = {} & g_{m2}R_2 g_{mc}R_1 r_{oc}C_c R_A + g_{m2}R_2 R_1 C_c R_A \\ & + g_{mc}R_A r_{oc}(R_1 C_1 + R_2(C_2 + C_c)) + R_1 R_A(C_c + C_A) \\ & + R_A(R_1 C_1 + R_2 C_2) + R_1 R_2(C_2 + C_c) \\ & + r_{oc}(R_2 C_c + R_A(C_c + C_A) + R_1 C_1 + R_2 C_2) \end{aligned} \tag{2.60}$$

$$a_2 = (g_{mc}R_A + 1)R_2C_1R_1r_{oc}(C_2 + C_c) + R_2r_{oc}R_AC_c(C_2 + C_A) + R_1R_2C_cR_AC_A + R_2C_2R_A(R_1(C_1 + C_c + C_A) + r_{oc}C_A) + R_1C_1R_A(r_{oc}(C_c + C_A) + R_2C_2) \quad (2.61)$$

$$a_3 = R_1C_1R_2r_{oc}R_A(C_2C_A + C_2C_c + C_cC_A) \quad (2.62)$$

Upon applying the approximations $g_{mk}R_k \gg 1, C_2 \approx C_L; C_c, C_2 \gg C_1, C_A$, we obtain the denominator coefficients to be same as seen for the case of cascoded load indirect compensation. Using the numerator coefficients, the locations of the zeros are given as

$$z_{1,2} = -\frac{1}{2(R_1 \parallel r_{oc})C_1} \pm \sqrt{\frac{1}{4(R_1 \parallel r_{oc})^2C_1^2} + \frac{g_{m2}g_{mc}}{C_cC_1}} \quad (2.63)$$

The zeros are real and one of the zero is in LHP while the other in RHP [7].

$$z_{LHP} = -\frac{1}{2(R_1 \parallel r_{oc})C_1} - \sqrt{\frac{1}{4(R_1 \parallel r_{oc})^2C_1^2} + \frac{g_{m2}g_{mc}}{C_cC_1}} \quad (2.64)$$

$$z_{RHP} = -\frac{1}{2(R_1 \parallel r_{oc})C_1} + \sqrt{\frac{1}{4(R_1 \parallel r_{oc})^2C_1^2} + \frac{g_{m2}g_{mc}}{C_cC_1}} \quad (2.65)$$

Also $|z_{LHP}| > |z_{RHP}|$. Now, if the condition $\frac{g_{m2}g_{mc}}{C_cC_1} \gg \frac{1}{4(R_1 \parallel r_{oc})^2C_1^2}$ is satisfied, the locations of the zeros can be simplified as

$$z_{LHP} \approx -\sqrt{\frac{g_{m2}g_{mc}}{C_cC_1}} \quad (2.66)$$

$$z_{RHP} \approx \sqrt{\frac{g_{m2}g_{mc}}{C_cC_1}} \quad (2.67)$$

The approximate pole locations for this topology are exactly the same as derived for cascoded load indirect compensation. Since the location of RHP zero is far away from the

unity-gain frequency, it is unlikely to degrade op-amp's stability. The LHP and RHP zeros are collocated in the frequency domain, and tend to cancel each others' effect in the phase response. Also if the non-dominant poles, p_2 and p_3, are complex conjugate we can recall that their location is given as $\mathrm{Re}(p_{2,3}) \approx \sqrt{\frac{g_{m2}g_{mc}}{C_1C_2}}$ which is same as the location of the LHP zero. Thus, the complex poles will be collocated with the LHP zero and form a cluster, which can be modeled by a single real pole. Thus the opamp response can be approximately represented with a two real poles and an RHP zero [7].

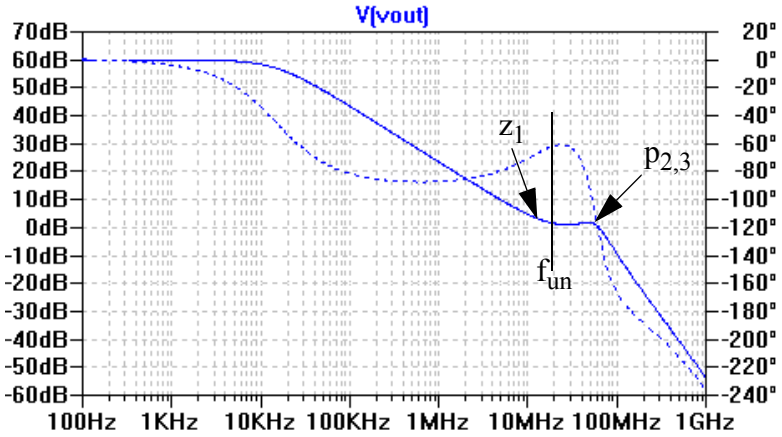

Figure 2-26. Small signal frequency response for the op-amp with indirect compensation using cascoded diff-pair. Here, f_{un}=20MHz and PM=60° .

Indirect Compensation using Split-Length Devices

It has been demonstrated in previous sections and that indirect compensation of two-stage op-amps can be achieved using the internal low impedance nodes in a cascoded topology. However, the voltage supply level has been scaling down and hence cascoding will no longer be feasible in the nano-CMOS processes. Techniques for indirect compen-

sation using split-length devices have been proposed in [1] and further illustrated in [9] which enable compensation in these low voltage nano-CMOS technologies.

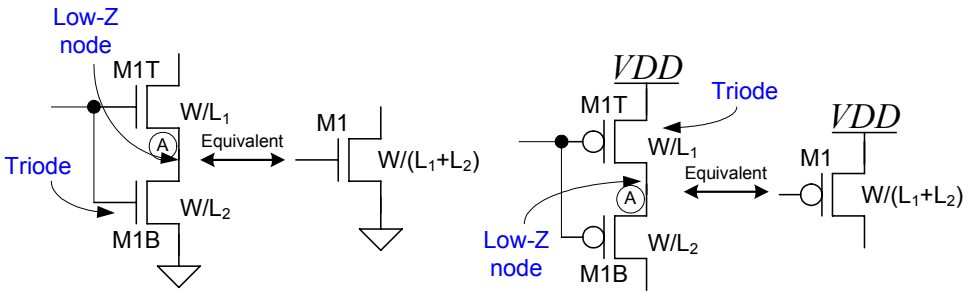

Figure 2-27. Figure illustrating split length NMOS and PMNOS devices and creation of the low impedance nodes.

Figure 2-27 illustrates how a NMOS or PMOS can be split up by its length to create a low impedance node-A. In the case of an NMOS, it can be shown that the lower device, M1B, will either be in triode or cut-off region. Since a triode device offers a low channel resistance and also that node-A is connected to the source of the upper device, node-A is a low impedance node. Similarly for the PMOS case, the top device, M1T, remains in triode or cut-off region. Hence node-A is again a low impedance node in the PMOS stack. The low impedance node-A can be used to feed back the compensation current to the output of the first gain stage i.e. node-1 [1].

Now since a simple (non-cascoded) diff-amp stage has visibly two sets of devices, current mirror load device and the diff-pair device. Indirect compensation can be achieved by splitting the lengths of either the load device or the diff-pair device.

Split Length Current Mirror Load

Figure 2-28 shows a two-stage op-amp with a split length current mirror load (SLCL). Here, the compensation capacitor is connected to the low impedance node-A in order to achieve indirect compensation. Since we are using minimum length devices in this example, the widths of the split PMOS devices have been doubled to 44 in order to keep the overall PMOS sizing to be 44/4, which is equivalent to 22/2. When using a process with minimum L of 1, we would have used 22/1 sized devices instead of 44/2.

Small signal analysis of the op-amp presented in Figure 2-28 is fairly complicated. In order to analyze the topology and to obtain the small signal transfer function, few simplifying assumptions have been made.

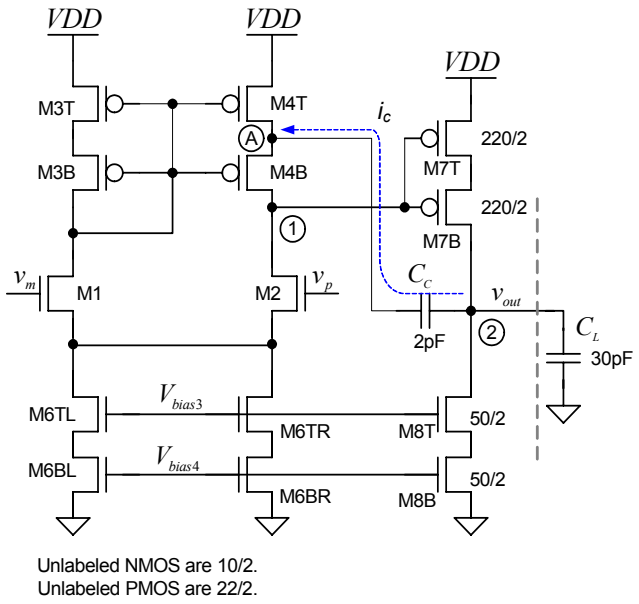

Figure 2-28. A two stage op-amp with indirect feedback compensation using split-length load devices (SLCL) [1].

Schematic in Figure 2-29 illustrates the deduction of a small signal model for the op-amp. Figure 2-29 shows the small signal analytical model for the op-amp topology under consideration. The transconductance of each of the split PMOS devices is labeled as g_{mp}. The resistances and capacitances at nodes 1 and A, have been lumped together and connected between the respective nodes and the ground. The resistance, R_A, can be approximated to be equal to the channel resistance of the trioded PMOS, which is approximated as $1/g_{mp}$ for small V_{SD} values. Also, here if the current mirror load is designed with the same g_m as the diff-pair, $g_{mp} = \sqrt{2}g_{m1}$, where g_{m1} is the equivalent transconductance of the first stage[1].

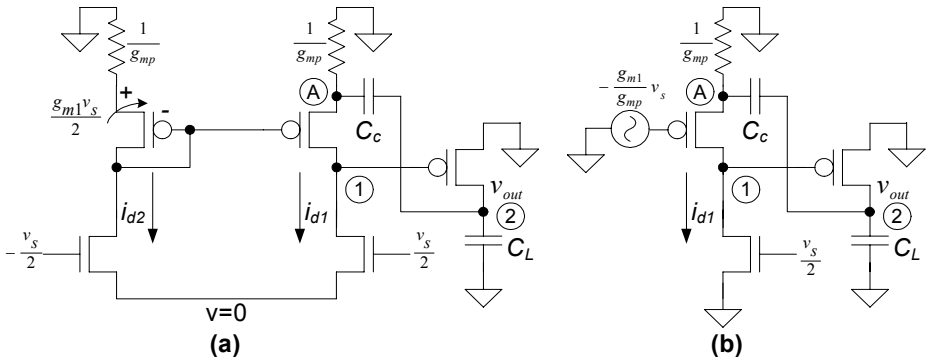

Figure 2-29. Small signal equivalent of the op-amp with split length load devices.

1. For a fixed bias current, I_D, $g_m = \sqrt{2I_D W/L}$. For L_p=L/2, we have the new transconductance, g_{mp}, given as $g_{mp} = \sqrt{2}g_{m1}$.

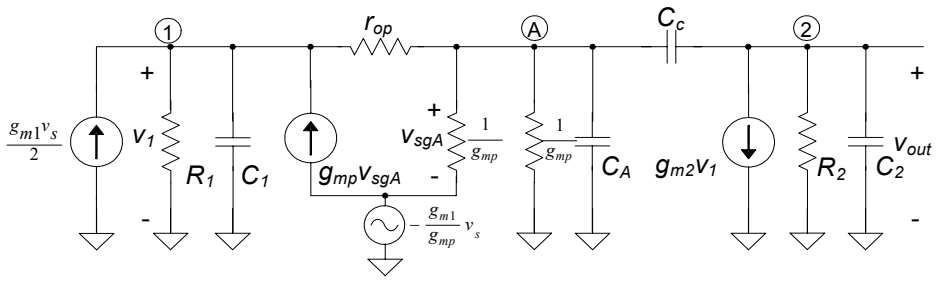

Figure 2-30. Small signal model for analysis of the op-amp employing split length load devices.

Applying nodal analysis on the derived small signal model in Figure 2-30, we get the following set of equations.

$$-g_{m1}\frac{v_s}{2}+\frac{v_1}{R_1}+v_1sC_1-g_{mp}\left(v_A+\frac{g_{m1}}{g_{mp}}v_s\right)+\frac{(v_1-v_A)}{r_{oc}}=0 \tag{2.68}$$

$$\frac{(v_A-v_1)}{r_{oc}}+g_{mp}\left(v_A+\frac{g_{m1}}{g_{mp}}v_s\right)+v_AsC_A+g_{mp}v_A+sC_c(v_A-v_{out})=0 \tag{2.69}$$

$$g_{m2}v_1+\frac{v_{out}}{R_2}+v_{out}sC_2+sC_c(v_{out}-v_A)=0 \tag{2.70}$$

On simultaneously solving Equations 2.68, 2.69 and 2.70, we obtain the following small signal transfer function.

$$\frac{v_{out}}{v_s}=-A_v\left(\frac{b_0+b_1s+b_2s^2}{a_0+a_1s+a_2s^2+a_3s^3}\right) \tag{2.71}$$

Again, on applying the conditions $g_{mk}R_k \gg 1$, $C_2 \approx C_L; C_c$, $C_2 \gg C_1, C_A$, we obtain the following approximate transfer function coefficients,

$$A_v = g_{m1}R_1 g_{m2}R_2 \tag{2.72}$$

$$b_0 \approx 4g_{mp}r_{op} \tag{2.73}$$

$$b_1 \approx 3r_{op}(C_c + C_A) \tag{2.74}$$

$$b_2 \approx (2r_{op}C_1C_c)/g_{m2} \tag{2.75}$$

$$a_0 \approx 4g_{mp}r_{op} \tag{2.76}$$

$$a_1 \approx 2g_{m2}R_2R_1g_{mp}r_{op}C_c \tag{2.77}$$

$$a_2 \approx 4R_2C_1R_1g_{mp}r_{op}(C_2 + C_c) + 2R_2C_2[r_{op}(C_c + C_A) + R_1(C_c + C_A + C_1)] \tag{2.78}$$

$$a_3 \approx 2R_1C_1R_2r_{op}(C_2C_A + C_2C_c + C_cC_A) \tag{2.79}$$

The unity-gain frequency is estimated as

$$f_{un} = \frac{g_{m1}}{2\pi(2C_c)} \tag{2.80}$$

Using the numerator expression in Equation 2.71, we obtain the location of the first LHP zero to be at

$$z_1 \approx -\frac{b_0}{b_1} = -\frac{4g_{mp}}{3(C_c + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c + C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un} \tag{2.81}$$

which implies that the LHP zero is located slightly farther away from the unity-gain frequency (i.e. at a frequency $3.77 \cdot f_{un}$).

The second LHP zero is located at

$$z_2 \approx -\frac{b_1}{b_2} = -\frac{3g_{m2}}{2C_1} \tag{2.82}$$

The high frequency second zero (z_2) appears due to the f_T limitation of the device(s) and can be ignored for the signal frequencies of interest.

The locations of the dominant pole is again given as

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{2g_{m2}R_2R_1C_c} \tag{2.83}$$

For $g_{mp} \gg \frac{g_{m2}C_c(C_2 \parallel C_c + C_A)}{C_1(C_2 + C_c)}$, the non-dominant poles are estimated as

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2}C_c}{2C_1(C_c + C_2)} \approx -\frac{g_{m2}C_c}{2C_1C_L}, \text{ and} \tag{2.84}$$

$$\begin{aligned} p_3 \approx -\frac{a_2}{a_3} &= -\frac{2g_{mp}}{(C_A + C_2 \parallel C_c)} - \frac{C_2/C_1}{R_1 \parallel r_{op}(C_2 + C_c \parallel C_c)} \\ &\approx -\left[\frac{2g_{mp}}{C_2 \parallel C_c} + \frac{1}{(R_1 \parallel r_{op})C_1}\right] \end{aligned} \tag{2.85}$$

And for $g_{mp} < \frac{g_{m2}C_c(C_2 \parallel C_c + C_A)}{C_1(C_2 + C_c)}$, the conjugate poles lie at

$$\left|\mathrm{Re}(p_{2,3})\right| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}} \tag{2.86}$$

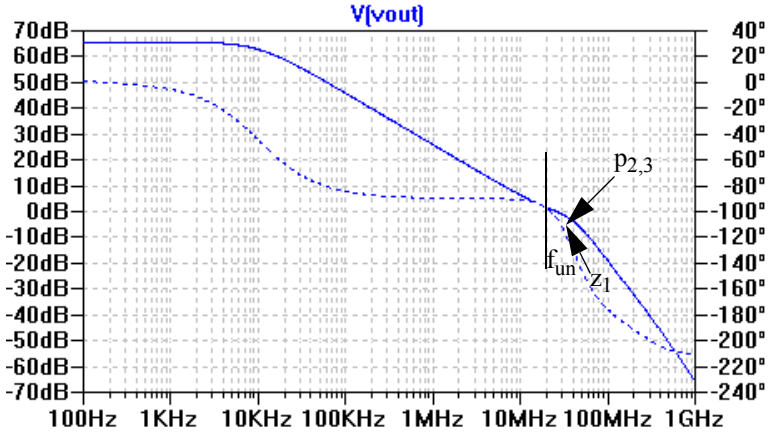

Figure 2-31. Frequency response of the SLCL op-amp topology. Here, f_{un}=20MHz and PM=75° .

The frequency response of this op-amp (see Figure 2-28) is displayed in Figure 2-31 while its time-domain settling is shown in Figure 2-32. As we can observe here, this op-amp achieves a high unity-gain frequency and a fast settling with lower power consumption than the common-gate indirect compensation topology seen in Figure 2-17.

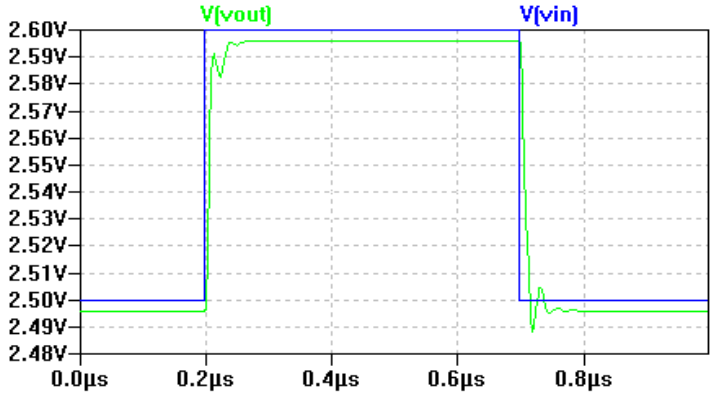

Figure 2-32. Small step input transient response of the SLCL op-amp topology. Here, the settling time, ts = 60ns.

The model in Figure 2-30 can be further simplified to a two-node model by assuming that the resistance r_{op} is large compared to other resistances. Figure 2-33 shows the simple two-node model for the present topology, derived using similar reasoning as seen for the case of indirect compensation using cascoded devices. Here, the parameter $R_c = \frac{1}{g_{mp}}$ corresponds to the general indirect compensation model seen in Figure 2-21.

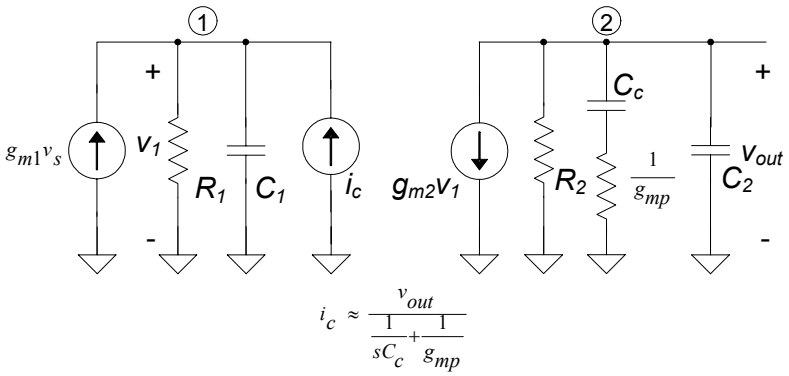

Figure 2-33. A simple two node small signal model for the SLCL op-amp.

Split Length Diff Pair

Figure 2-34 shows a two-stage op-amp with a split length differential pair (SLDP). Again the low impedance node-A is used to feedback the compensation current to node-1. The widths of the split-length NMOS devices have been doubled in the present design to achieve a combined W/L of 10/2 (=20/4).

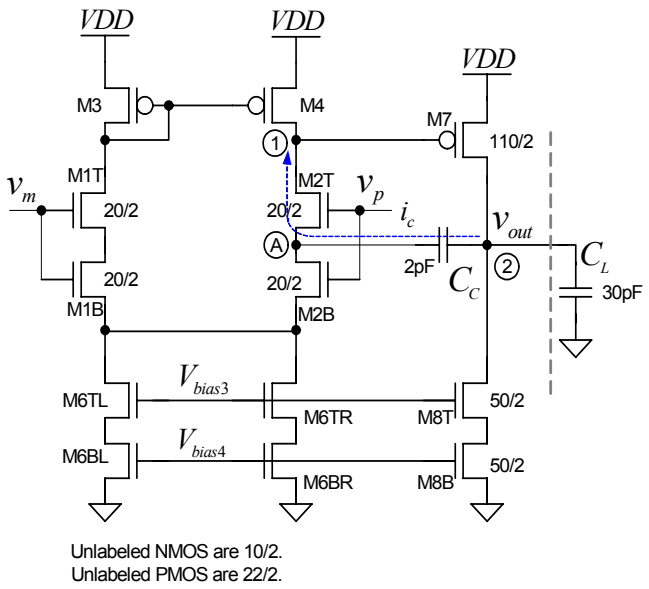

Figure 2-34. A two stage op-amp with indirect feedback compensation using split-length diff-pair (SLDP).

Again, simplifying assumptions have been made to analyze the split diff pair opamp topology. Figure 2-35 illustrates the derivation of a small signal model for the op-amp. Figure 2-36 shows the small signal analytical model for this op-amp topology. The transconductance of each of the split NMOS device is labeled as g_{mn}. The resistances and capacitances at nodes 1 and A, have been lumped together and connected between the respective nodes and the ground. The resistance, R_A, can be approximated to be equal to the channel resistance of the trioded NMOS, which is $1/g_{mn}$. Also, here $g_{mn} = \sqrt{2}g_{m1}$, where g_{m1} is the equivalent transconductance of the first stage.

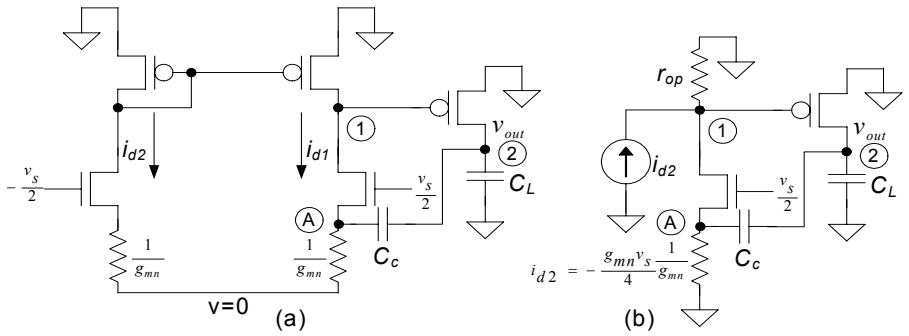

Figure 2-35. Small signal equivalent of the op-amp with split length diff-pair.

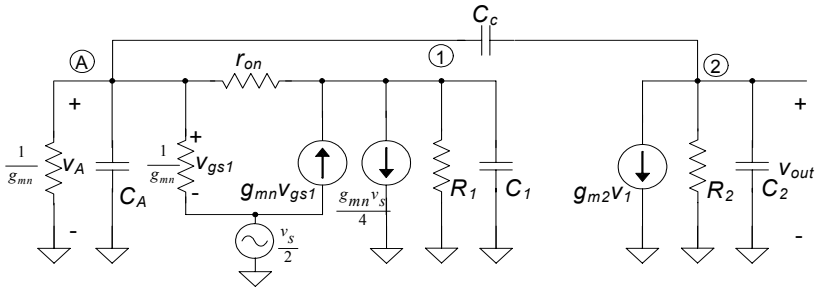

Figure 2-36. Small signal model for analysis of the op-amp employing split length diff-pair devices.

Again, applying nodal analysis on the derived small signal model in Figure 2-36, we get the following set of equations.

$$g_{mn}v_A + v_A sC_A + \frac{(v_A - v_1)}{r_{on}} + g_{mn}\left(v_A - \frac{v_s}{2}\right) + sC_c(v_A - v_{out}) = 0 \qquad (2.87)$$

$$\frac{v_1}{R_1} + v_1 sC_1 - g_{mn}\left(v_A - \frac{v_s}{2}\right) + \frac{(v_1 - v_A)}{r_{on}} + g_{mn}\frac{v_s}{4} = 0 \qquad (2.88)$$

$$g_{m2}v_1 + \frac{v_{out}}{R_2} + v_{out}sC_2 + sC_c(v_{out} - v_A) = 0 \tag{2.89}$$

Simultaneous solution of the Equations 2.87, 2.88 and 2.89, leads to the following small signal transfer function.

$$\frac{v_{out}}{v_s} = -A_v\left(\frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2 + a_3 s^3}\right) \tag{2.90}$$

Applying the conditions $g_{mk}R_k \gg 1$, $C_2 \approx C_L; C_c$, $C_2 \gg C_1, C_A$, we obtain the following approximate transfer function coefficients,

$$A_v = (g_{mn}/2)R_1 g_{m2} R_2 \tag{2.91}$$

$$b_0 \approx 8 g_{mn} r_{on} \tag{2.92}$$

$$b_1 \approx 6 r_{on}(C_c + C_A) \tag{2.93}$$

$$b_2 \approx 4 r_{on} C_1 C_c / g_{m2} \tag{2.94}$$

$$a_0 \approx 8 g_{mn} r_{on} \tag{2.95}$$

$$a_1 \approx 4 g_{m2} R_2 R_1 g_{mn} r_{on} C_c \tag{2.96}$$

$$a_2 \approx 8 R_2 C_1 R_1 g_{mn} r_{on}(C_2 + C_c) + 4 R_2 C_2 [r_{op}(C_c + C_A) + R_1(C_c + C_A + C_1)] \tag{2.97}$$

$$a_3 \approx 4 R_1 C_1 R_2 r_{on}(C_2 C_A + C_2 C_c + C_c C_A) \tag{2.98}$$

The unity-gain frequency is estimated to be

$$f_{un} = \frac{2 g_{m1}}{2\pi C_c} \tag{2.99}$$

Using the numerator expression of the transfer function, we obtain the location of the first LHP zero to be at

$$z_1 \approx -\frac{b_0}{b_1} = -\frac{4g_{mn}}{3(C_c + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_c + C_A)} \approx \frac{2\sqrt{2}}{3}\omega_{un} \tag{2.100}$$

which implies that the LHP zero arrives slightly earlier than the unity-gain frequency (i.e. at a frequency $0.94 \cdot f_{un}$). This has the effect of flattening the gain magnitude response around f_{un}.

The second LHP zero is located at

$$z_2 \approx -\frac{b_1}{b_2} = -\frac{3g_{m2}}{2C_1} \tag{2.101}$$

Again, the high frequency second zero (z_2) can be ignored. The location of the dominant pole is given as

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{2}{g_{m2}R_2R_1C_c} \tag{2.102}$$

For $g_{mn} \gg \frac{4g_{m2}C_c(C_2 \parallel C_c + C_A)}{C_1(C_2 + C_c)}$, the non-dominant poles are given as

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2}C_c}{2C_1(C_c + C_2)} \approx -\frac{g_{m2}C_c}{2C_1C_L}, \text{ and} \tag{2.103}$$

$$\begin{aligned} p_3 \approx -\frac{a_2}{a_3} &= -\frac{2g_{mn}}{(C_A + C_2 \parallel C_c)} - \frac{C_2/C_1}{R_1 \parallel r_{on}(C_2 + C_c \parallel C_c)} \\ &\approx -\left[\frac{2g_{mn}}{C_2 \parallel C_c} + \frac{1}{(R_1 \parallel r_{on})C_1}\right] \end{aligned} \tag{2.104}$$

And for $g_{mn} < \frac{4g_{m2}C_c(C_2 \parallel C_c + C_A)}{C_1(C_2 + C_c)}$, the conjugate poles appear at

$$\left|\mathrm{Re}(p_{2,3})\right| = \frac{g_{m2}}{C_L}\sqrt{\frac{g_{mp}C_L}{g_{m2}C_1}} \tag{2.105}$$

The frequency response of this op-amp, with the schematic seen in Figure 2-34, is displayed in Figure 2-37 while its time-domain settling is shown in Figure 2-38. We can again observe that this op-amp achieves a high unity-gain frequency with lower power consumption that the common-gate indirect compensation topology seen in Figure 2-17. However, the time-domain settling is not as good as the phase margin is reduced due to the gain flattening.

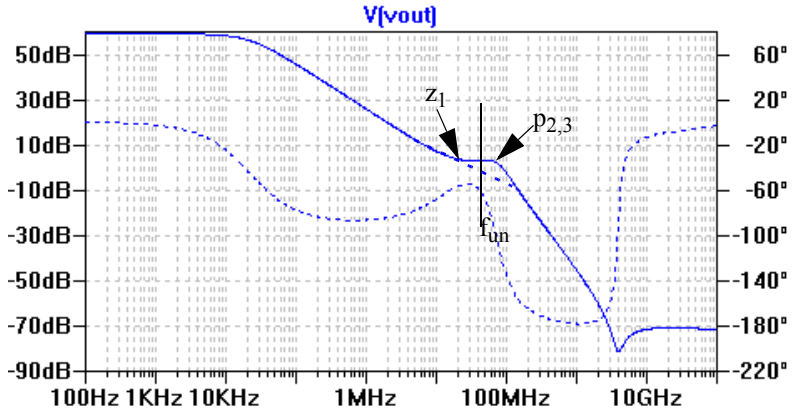

Figure 2-37. Frequency response of the SLDP op-amp. Here, f_{un}=35MHz and PM=60° . The zero appearing before f_{un} flattens the magnitude response and reduces the phase margin.

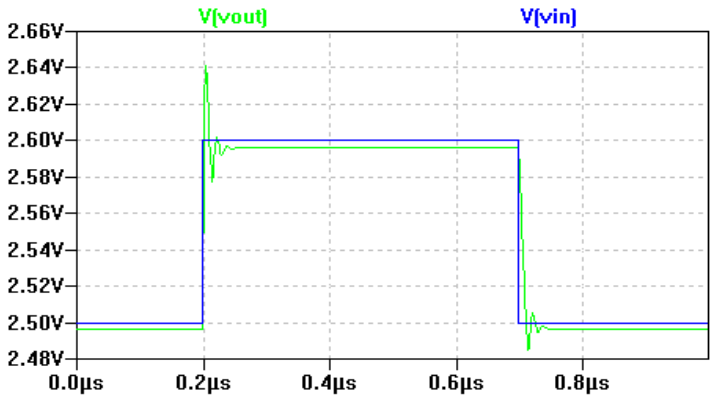

Figure 2-38. Small step input transient response of the SLDP op-amp. Here t_s=75ns.

The model in Figure 2-36 is reduced to a two-node model by assuming that the resistance r_{on} is large compared to other resistances. Figure 2-38 shows the simpler two-node model for the split diff-pair opamp topology. Similarly, the parameter $R_c = \frac{1}{2g_{mn}}$ corresponds to the general indirect compensation model in Figure 2-21.

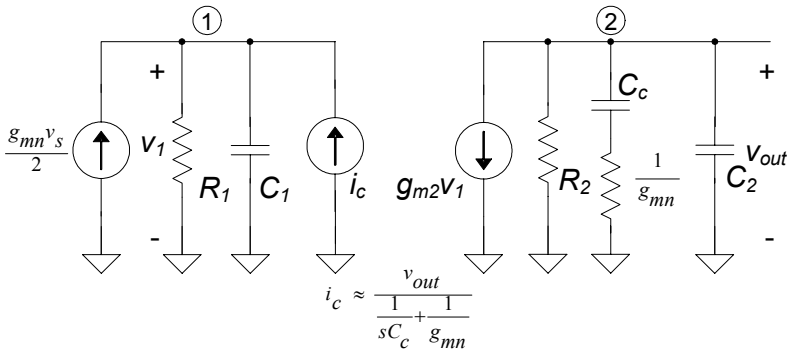

Figure 2-39. A simple two node small signal model for the SLDP op-amp.

The split diff-pair op-amp topology results in better power supply rejection ratio (PSRR) than the split load topology, as the compensation capacitor is isolated from the power supply and the ground rails.

It can be observed that when using split-length devices for indirect compensation, we do not have a strong control over the location of the LHP zero. Especially in the SLDP case, the LHP zero arrives before the unity-gain frequency (f_{un}), which flattens out the op-amp magnitude response. This can result in a situation where the phase margin degrades sharply due to the presence of the complex conjugate non-dominant poles. In another scenario, the complex conjugate non-dominant poles can peak beyond unity-gain and affect the stability. Both of these scenarios are illustrated in Figure 2-40.

These scenarios can potentially be avoided by pushing the LHP zero farther right from f_{un}. In the case of SLCL indirect compensation, we have the flexibility of varying g_{mp} independent of g_{m1} in order to control the location of the LHP zero and hence the phase margin of the op-amp. However, in the case of SLDP we do not have such convenience and it might be hard to obtain desirable phase margins with the SLDP topology. But the SLDP indirect compensation topology is of great utility when designing indirect compensated multi-stage op-amps as described in the Chapter 3.

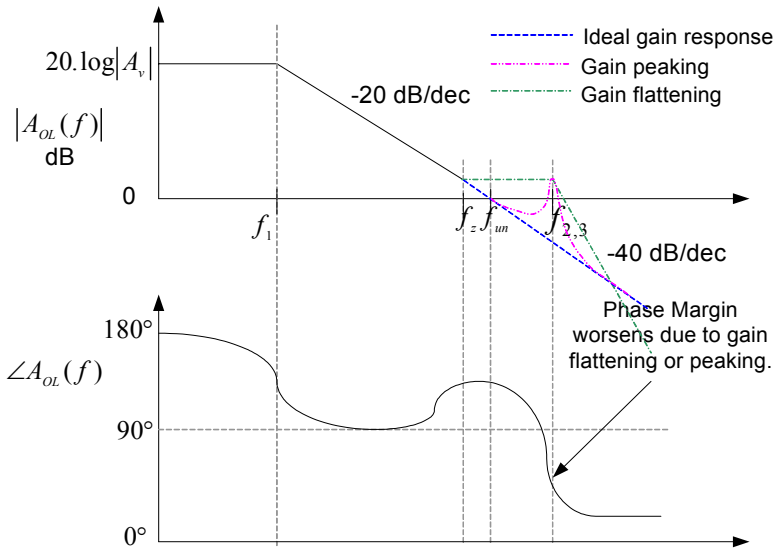

Figure 2-40. Illustration of degradation in phase margin due to gain flattening and gain peaking.

Nevertheless, in scenarios where a resistive switch (R_{sw}) is connected between the op-amp output and the capacitive load (C_L), the R_{sw}-C_L low-pass filtering can help in constricting the op-amp's bandwidth and help improve the phase-margin and transient settling. Also in sub-100nm processes where devices have larger f_T values and smaller parasitics, the effects of gain peaking and flattening are not pronounced.

Slew-Rate Limitations in Op-Amps

Slew rate (SR) defines how fast a given load can be charged or discharged by an op-amp. If a constant current source (I_S) charges a load capacitance (C_L), then the slew rate is given as

$$SR = \frac{dV_{out}}{dt} = \frac{I_S}{C_L} \tag{2.106}$$

The op-amp topologies presented earlier in the chapter in Figures 2-22, 2-24, 2-28 and 2-34 are all Class A op-amps. Class A op-amps have a current source either charging or discharging the output load capacitance, which limits the slew-rate of these op-amps. Figure 2-41 shows the slew rates in a class A op-amp. Here, there is no slew-rate limitation when the op-amp is charged up as M7 is turned fully on and it sources current roughly given by the square law equation[2]. On the other hand when the output is discharged through the output current source, slew-rate limitation comes into picture. the discharge slew-rate is then given as $\frac{I_{SS2}}{C_L}$, where I_{ss2} is the bias current in the output stage. This implies that for a class A op-amp more power needs to be burned in the output stage to achieve a better slew-rate.

To mitigate the slew-rate limitations associated with the class A op-amp, we consider the op-amps topology with a class AB output buffer. Figure 2-42 shows an indirect compensated two-stage op-amp with class AB output buffer. The class AB output buffer is realized using a floating current source to bias the push-pull output stage. The bias circuit

---

2. The current sourced into the load varies by square of the gate overdrive of the transistor, and is given as $i_D = \frac{\beta}{2}(v_{ov})^2$. where $V_{ov} = V_{SG}-V_{THP}$ for the PMOS case.

required to generate references V_{ncas} =($2V_{GS}$) and V_{pcas}=(VDD-$2V_{SG}$) is shown in Figure 2-43. The floating current mirror acts like a biasing battery and turns PMOS M9 on while shutting off NMOS M10 while charging the load, similarly M9 shuts off and M10 turns on when the load is discharged [1].

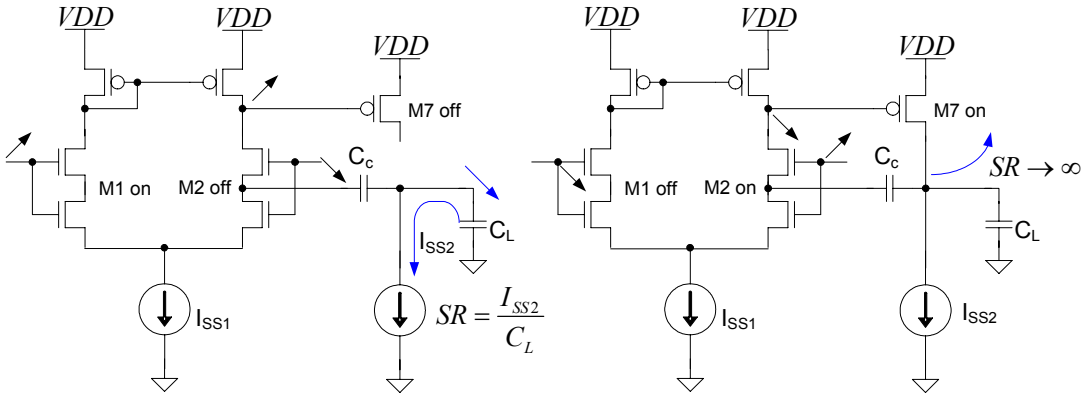

Figure 2-41. Slew rate limitations in a Class A op-amp topology. Here, the slew rate limitation occurs when the load capacitance is discharged by the constant current source I_{SS2}. However there is no SR limitation when the load is charged up.

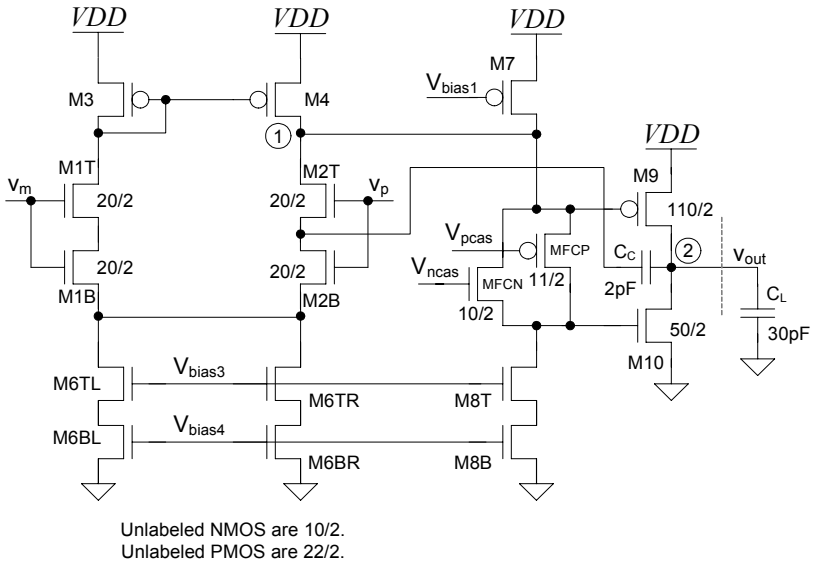

Figure 2-42. An indirect-compensated op-amp with Class AB output buffer.

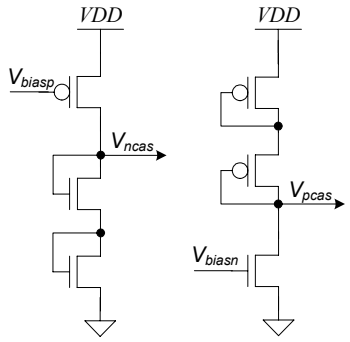

Figure 2-43. Schematic for generation of bias voltages Vncas and Vpcas used in Figure 2-42.

It may appear that class AB output buffer doesn't have any slew rate limitation as the devices in the output buffer source or sink currents given by the MOSFET's square law equation. However, as illustrated in Figure 2-44, the feedback compensation current, i_c, flowing through the compensation capacitor, C_c, is limited by the maximum current which can be sunk by the diff-amp tail current source (I_{SS1} here). This will pose a slew rate limitation on charging of the load and is given as

$$SR = \frac{dV_{out}}{dt} = \frac{I_{SS1}}{C_c} \tag{2.107}$$

Here the slew-rate limitation comes from the total bias current in the input diff-amp stage. As we can observe from Equation 2.107, indirect compensation results in much faster slew-rates as the compensation capacitor size is much lesser than that in the case of the Miller compensated op-amp.

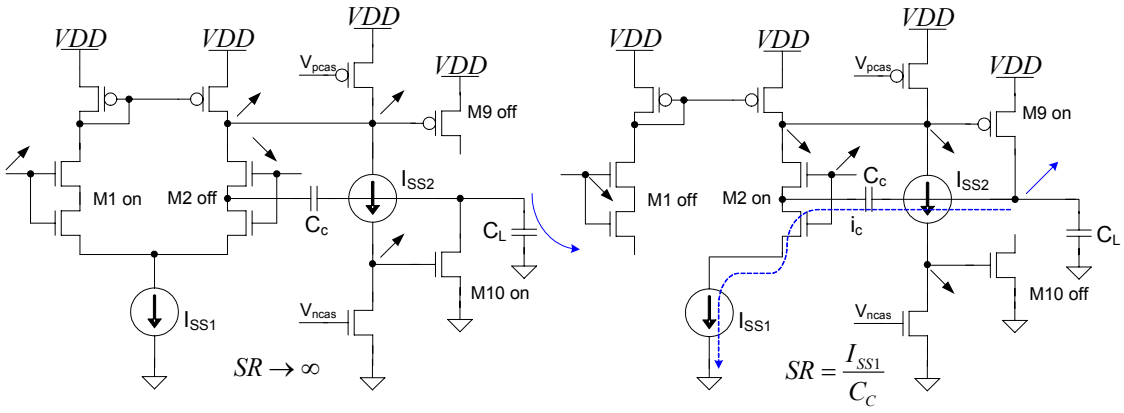

Figure 2-44. Slew rate limitations in a Class AB op-amp topology. Here, there is no SR limitation when the load capacitance is discharged. However, when the output goes high by charging the load up, the feedback compensation current is limited by the diff-amp current I_{ss1}. This leads to a output charging slew rate limitation given as I_{ss1}/C_C.

Several standard indirect compensated Class AB topologies employing wide-swing cascoding like telescopic and folded-cascode op-amps have been discussed in [1] with ample illustrations.

Low Supply Voltage Designs

Also we can observe that the class A and class AB topologies shown in Figures 2-22, 2-24, 2-28, 2-34 and 2-42 require a minimum supply voltage of $VDD_{min} = V_{THP} + V_{SD,\,sat} + 3V_{DS,\,sat}$, which is equal to 1.425V for AMI C5N process with the design parameters used in Table 2-1.

A further reduction in supply voltage can be accommodated if a cascade of simple diff-amps, without employing any cascoding, are used to construct the op-amps.

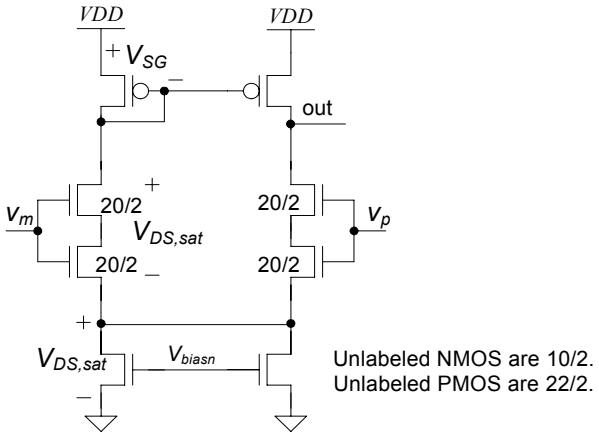

Figure 2-45. A basic diff-amp block for construction of low voltage op-amps. The split diff-pairs can be used for indirect compensation in the designed op-amp topology.

Figure 2-45 shows a basic diff-amp block which can be used to construct low voltage op-amps. The minimum supply voltage for this diff-amp is $V_{DDmin} = V_{THP} + V_{SD,sat} + 2V_{DS,sat} = 1.275V$. However, this topology results the open-loop DC gain to be an order less than that in the case of cascoded (telescopic and folded-cascode) diffamps. Thus in order to achieve high open-loop DC gain, multiple low-voltage gain stages can be cascaded. The resulting multi-stage op-amp topologies are discussed in the next chapter.

Ultra low power op-amp design techniques are proposed in [12], where the body input is employed for biasing and amplification. However such techniques are not the mainstay in low-voltage circuit design due to significant compromise in performance. Thus using the building block diff-amp, shown in Figure 2-45, is the only logical approach towards manufacturable low-power op-amp designs.

The two-stage topologies, discussed in this chapter, have been fabricated on chip using AMI 0.5µm CMOS process and their test results are presented later in Chapter 5. Since AMI 0.5µm is relatively a long-channel process with miniscule random offsets and process variations, the actual chip test results are bound to be close to the SPICE simulation results. From the simulation results we can concur that the two-stage op-amps employing split-length indirect feedback compensation exhibit a ten times enhancement in unity-gain frequency and four times faster step-input response settling time when compared to the Miller compensated op-amps. Also these op-amps consume 40% less power and occupy only half the layout area. Further, these techniques can be used to compensate op-amps when using small supply voltage (VDD).

Summary

Indirect feedback compensation technique leads to the design of high-speed, compact and low power two-stage op-amps when compared to the traditional Miller (or Direct) compensation scheme. Utilization of indirect compensation results in lower biasing current in the output stage and hence smaller device sizes. Also op-amp compensation can be achieved by employing a significantly smaller compensation capacitor, when employing indirect compensation. Further, since the internal high impedance node is not loaded by the compensation capacitance, the indirect compensated op-amp exhibits higher unity-gain frequency and thus potentially faster transient settling.

When using wide-swing cascode op-amp topologies, the low impedance node in the cascoded device-stack can be used for indirect compensation. For low-voltage op-amp

topologies, split-length devices can be used to achieve indirect compensation. We have provided detailed analysis for each of the indirect compensation methods. Slew rate limitations of class A op-amp topologies have been discussed. A class AB topology employing push-pull output buffer alleviates the slew rate limitations. Since the class AB topology is slew rate limited only by the compensation capacitance, smaller compensation capacitance results in significantly better slew rates, when using indirect compensation.

MULTI-STAGE OPERATIONAL AMPLIFIER FREQUENCY COMPENSATION

IT'S evident that three-stage op-amps are bound to be indispensable for integrated system design in near future with further scaling in CMOS processes. Continued interest in the three-stage op-amp design has seen numerous three-stage op-amp design techniques being reported in literature [13]-[30]. Even though the three-stage op-amps provide high-gain and enable low voltage circuit implementations, they have not been widely used in system design. This is due to the fact that most of the reported three-stage op-amp topologies have either complex stability criterion, or they consume much more power when compared to the prevalent two-stage op-amps. This chapter discusses biasing schemes commonly observed in literature which are not practical and do not have well controlled current flowing in the gain stages. A diff-amp based multi-stage biasing scheme is re-enforced in the first section of this chapter. Later the widely reported op-amp design and compensation schemes are discussed along with their limitations.

Later in this chapter, the indirect feedback compensation technique introduced in the previous chapter is applied to three-stage op-amp compensation. This technique results in stable op-amps with minimal design restrictions posed by earlier reported op-amp design techniques. Towards the end of this chapter, a generalized indirect compensation model is presented with exact analysis for multi-stage op-amp design.

Biasing for Multi-stage Op-Amps

Biasing is an important concern when designing multi-stage op-amps. If all the gain stages of the multi-stage op-amp are not biased properly with the intended overdrive voltages, the bias currents and hence the transconductances and gains of the amplifying stages remain unknown. This may significantly worsen the performance of the op-amp, consume larger current and can even push the multi-stage op-amp to instability. Thus considerable attention must be paid to biasing while designing practical multi-stage op-amps.

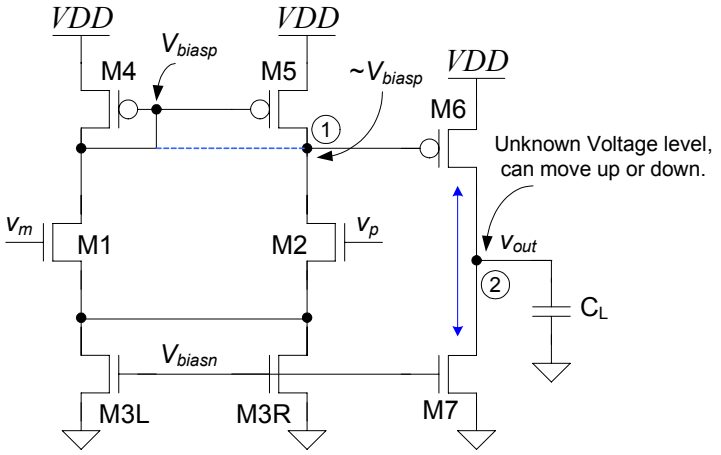

Figure 3-1. Biasing of a two-stage op-amp. Note that the compensation network is not included here.

For a two stage op-amp, the first stage is always a diff-amp which is followed by a common-source gain stage serving as the second stage (see Figure 3-1). Here, the voltage level of node-1 biases the second gain stage. Also node-1 transfers the amplified AC input signal by the first stage to the second stage. Now, due to symmetry in the diff-amp, the node-1 is approximately at the voltage level V_{biasp}. This serves as a reference to bias the

second stage, with the same overdrive voltage as in the first stage. Even with process offsets, node-1 will remain close to the reference V_{biasp}.

Looking at the output of the op-amp in Figure 3-1 (i.e. node-2), the current source realized by the PMOS M6, fights with the current sink realized by the NMOS M7. Now, if these two currents do not match precisely, the voltage at node-2 will float up or slide down depending the whether M7 is stronger or weaker than M6. Thus in open loop configuration, the voltage level of the output node will remain unknown. However, when the two-stage op-amp is placed in a closed loop configuration node-2 attains a well defined voltage which is set by the negative feedback.

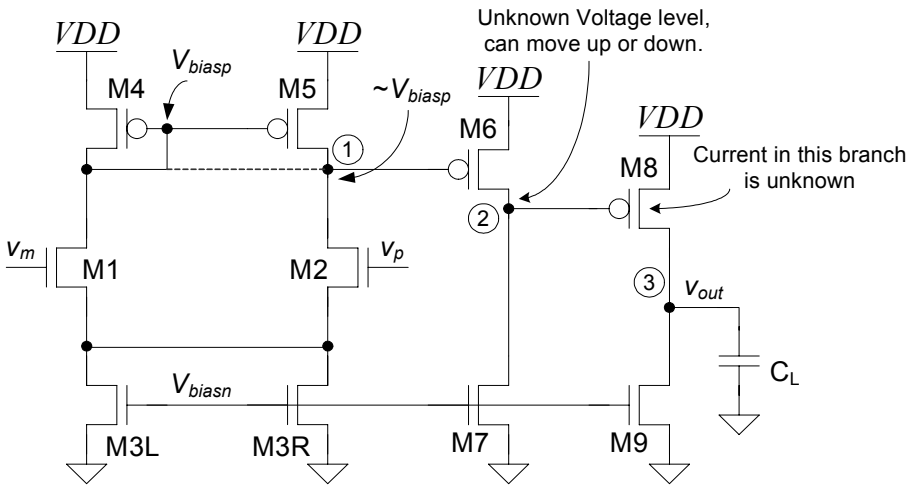

Figure 3-2. Example of bad biasing of a three stage op-amp often found in literature. Again, frequency compensation is not considered in this figure.

Now, if we try to use the two-stage topology seen in Figure 3-1 and attempt to realize a three-stage op-amp by just cascading another common-source gain stage in series, we

obtain the topology shown in Figure 3-2. Since the voltage level of node-2 here is unknown, it doesn't set the right value of current in the third stage. Thus the third stage (device M8) is not at all biased properly and the current flowing through that branch is unknown. This implies that the overdrive voltage and the transconductance, g_{m3}, are unknown for the third stage. This may potentially lead to a situation where a large current flows through the third stage resulting in large power consumption and poor gain. Such designs, as seen in Figure 3-2, will function properly in a closed-loop configuration but with an offset which sets the bias currents. However, it must be noted that here we are trying to set the voltage level at node-2 (which serves as the bias for the third stage) by matching the output resistances of the PMOS current source and the NMOS current sink, which are fighting each other. This may work in large channel processes where output resistances are large. But when using the modern sub-100nm CMOS processes, which have low gains and large mismatches, the bias voltage at node-2 will vary significantly from the ideal value and thus will adversely affect the biasing of the third stage [1]. Examples of such topologies with inadequate biasing will be illustrated in following sections in this chapter.

Consider the three-stage op-amp topology illustrated in Figure 3-3. Here diff-amps are used for the first and second gain stages, both of which are biased with the same reference, V_{biasn}. Here, the voltage levels of the nodes 1 and 2 are set to be approximately equal to V_{biasp}, due to symmetry in each of the diff-amps. Thus the bias currents in all the three gain stage branches are well defined, and their transconductances and gains are precisely fixed and set by the bias reference V_{biasn}. A diff-amp is not used in the last stage due to its

limited output swing. Also incorporation of diff-amps as inner gain stages leads to higher common-mode rejection ratio (CMRR) in the resulting op-amp [1].

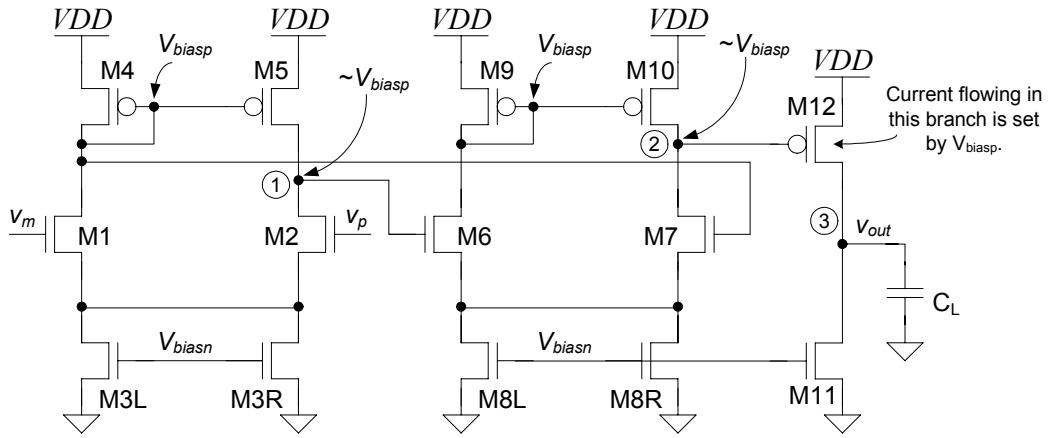

Figure 3-3. A three-stage class A op-amp design where currents flowing in every stage is known and all the gain stages are biased properly with the desired overdrive voltage value. Compensation network is not shown in this figure.

The topology, with a diff-amp as inner stage(s), will always bias up properly even in the presence of large offsets. This topology for three stage can be generalized for design of the N-stage class A op-amp as shown in Figure 3-4. For an N-stage op-amp the first (N-1) stages should be realized using diff-amps and the last stage can be a common-source stage or a class AB output buffer.

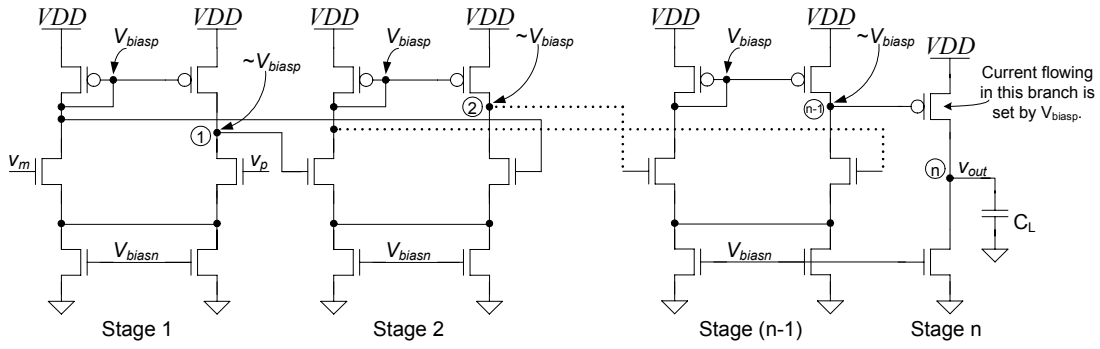

Figure 3-4. N-stage class A op-amp topology where all the gain stages are biased properly and bias currents are known. Frequency compensation has not been considered in this figure.

Nested Miller Compensation Techniques

The Miller (or Direct) compensation technique can be extended to three or more stage op-amp design by using nested compensation loops in the op-amp. A comprehensive analysis and comparison of various multi-stage Miller compensation techniques is provided in [13]. The following sub-sections present a brief review on multi-stage nested Miller compensation techniques. Note that in the discussion in this section doesn't present a design recipe for multi-stage op-amps based on a given phase margin, as often seen in literature. Instead we have focused on design approaches to achieve best possible phase-margin for the given power consumption.

Nested Miller Compensation

Nested Miller Compensation (NMC) topology is a straight-forward extension of the Miller (or Direct) compensation technique used in the two-stage op-amps. A simplified block diagram for the nested Miller compensation three-stage op-amp is shown in Figure 3-

5. Before compensation, the three poles associated with the high impedance nodes 1,2 and 3 are located close to each other. These poles must be separated from each other or must be arranged in such a way that the resulting op-amp is stable. In this technique, pole splitting is achieved by connecting compensation capacitors, C_{c1} and C_{c2}, between the output and the internal nodes 1 and 2 respectively [6]. Here, the second stage should be non-inverting and the third stage needs to be inverting in order to observe the nested Miller effect and hence the dual pole-splitting.

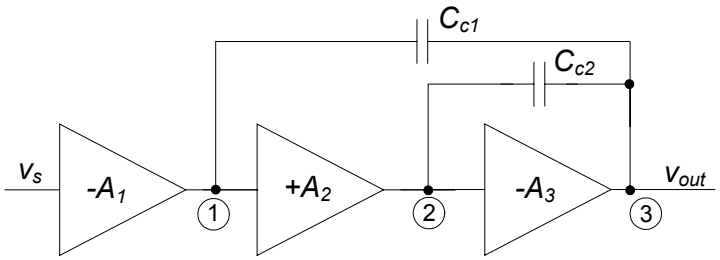

Figure 3-5. Block diagram of a Miller compensated three-stage op-amp.

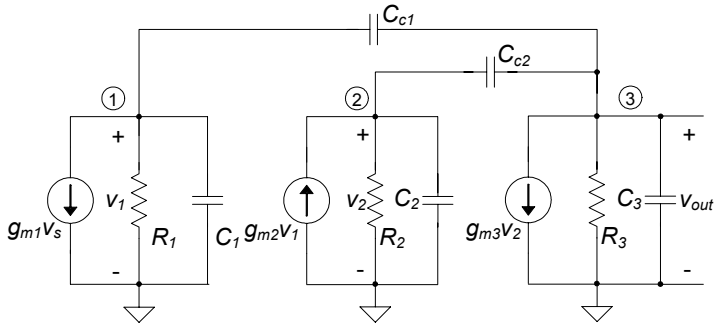

Figure 3-6. Small signal model for nested Miller compensated three-stage op-amp.

The small signal transfer function for the nested Milled compensation three-stage op-amp, obtained by applying nodal analysis on the small signal model shown in Figure 3-6, is given as [6]

$$\frac{v_{out}}{v_{in}} \approx \frac{g_{m1}R_1 g_{m2}R_2 g_{m3}R_3\left(1-\frac{sC_{c2}}{g_{m3}}-\frac{s^2C_{c1}C_{c2}}{g_{m2}g_{m3}}\right)}{(1+sg_{m3}R_3g_{m2}R_2R_1C_{c1})\left(1+\frac{sC_{c2}(g_{m3}-g_{m2})}{g_{m2}g_{m3}}+\frac{s^2C_{c2}C_3}{g_{m2}g_{m3}}\right)} \tag{3.1}$$

From Equation 3.1, we can infer that the small signal transfer function has two zeros and three poles. For $g_{m3} \gg g_{m2}$, Equation 3.1 can be further simplified as

$$\frac{v_{out}}{v_{in}} \approx \frac{g_{m1}R_1 g_{m2}R_2 g_{m3}R_3\left(1-\frac{sC_{c2}}{g_{m3}}-\frac{s^2C_{c1}C_{c2}}{g_{m2}g_{m3}}\right)}{(1+sg_{m3}R_3g_{m2}R_2R_1C_{c1})\left(1+\frac{sC_{c2}}{g_{m2}}+\frac{s^2C_{c2}C_3}{g_{m2}g_{m3}}\right)} \tag{3.2}$$

Reference [13] uses the approximation $g_{m3} \gg g_{m1}, g_{m2}$ to simplify the analysis and neglect the effect of zeros on stability of the op-amp. However, this assumption implies that a large value of bias current is used in the third stage, which leads to poor power utilization. On the other hand the effect of zeros is considered in [6] and a complex non-dominant pole approach is used as opposed to the separate pole approach suggested in [14]. Also [13] uses topologies where common source stages are cascaded to realize gain stages which are example of bad biasing as discussed earlier.

Here, the dominant pole is given as

$$p_1 \approx -\frac{1}{g_{m3}R_3g_{m2}R_2R_1C_{c1}} \tag{3.3}$$

and the unity gain frequency (or the gain bandwidth) of the op-amp is

$$f_{un} \approx \frac{g_{m1}}{2\pi C_{c1}} \tag{3.4}$$

The zeros are estimated by factorizing the numerator which yields the following roots

$$z_{1,2} \approx -\frac{g_{m2}}{2C_{c1}}\left(1 \pm \sqrt{1 + \frac{4g_{m3}C_{c1}}{g_{m2}C_{c2}}}\right) \tag{3.5}$$

Thus, there exists an LHP zero along with an RHP zero which are given as

$$z_{LHP} \approx -\frac{g_{m2}}{2C_{c1}}\left(\sqrt{1 + \frac{4g_{m3}C_{c1}}{g_{m2}C_{c2}}} + 1\right) \tag{3.6}$$

$$z_{RHP} \approx \frac{g_{m2}}{2C_{c1}}\left(\sqrt{1 + \frac{4g_{m3}C_{c1}}{g_{m2}C_{c2}}} - 1\right) \tag{3.7}$$

Since $|z_{RHP}| < |z_{LHP}|$, the RHP zero appears at a lower frequency than the LHP zero and degrades the phase margin [6].

The non-dominant poles are estimated by factorizing the quadratic polynomial in the denominator in Equation 3.1. The poles p_2 and p_3 are real and widely spaced when the condition $C_{c2} \gg \frac{4g_{m2}g_{m3}C_3}{(g_{m3} - g_{m2})^2}$ is satisfied, and are given as

$$p_2 \approx -\frac{g_{m2}g_{m3}}{(g_{m3} - g_{m2})C_{c2}}, \text{ and} \tag{3.8}$$

$$p_3 \approx -\frac{(g_{m3} - g_{m2})C_{c2}}{C_2C_3 + C_{c2}(C_2 + C_3)} \approx -\frac{(g_{m3} - g_{m2})}{C_2 + C_3} \tag{3.9}$$

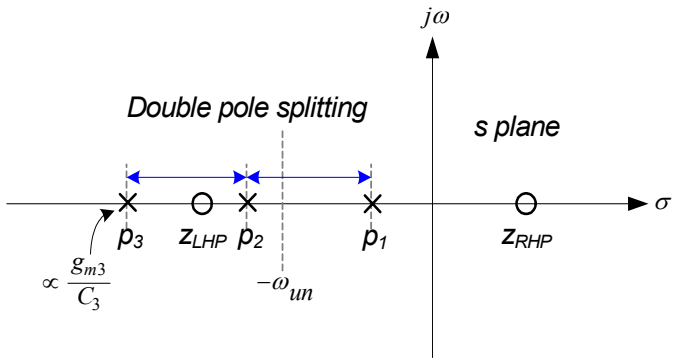

Figure 3-7. S-plane plot for a NMC three-stage op-amp with widely spaced poles. Here large amount of power is consumed in the third stage to keep pole p_3 farther away from pole p_2 and f_{un}.

Now, in order to have pole p_2 and p_3 in LHP for op-amp stability, the condition $g_{m3} \gg g_{m2}$ must always be satisfied. The poles can be splitted apart by employing the design criterion $|p_1| \ll |p_2| \ll |p_3|$, which approximates a two-stage op-amp if $|p_3|$ is positioned far beyond f_{un} (shown in Figure 3-7). However, this translates into a large value of g_{m3} coming at the cost of either large bias current in the last stage or a much reduced unity gain frequency. A higher unity gain frequency (or lower power) can be achieved if poles p_2 and p_3 are complex conjugate, as shown in Figure 3-8. However, care must be taken to avoid peaking and instability while using complex non-dominant poles by avoiding a low damping factor. Since f_{un} depends only upon C_{c1} from Equation 3.4, and the poles, p_2 and p_3,depend upon C_{c2} only (see Equations 3.8 and 3.9). Hence stable op-amp can theoretically be designed by using larger values of C_{c1} and restricting the f_{un} below p_2 and p_3 [6].

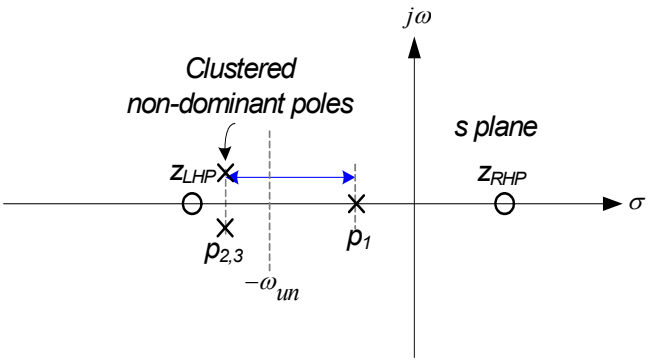

Figure 3-8. S-plane plot for a NMC three-stage op-amp with clustered or conjugate non-dominant poles. Here lesser amount of power is consumed in the third stage, compared to the case when the poles are widely spaced.

The frequency locations of the zeros, for this op-amp topology, are comparable to that of the second pole p_2. The RHP zero appearing will reduce the phase margin before $|p_2|$, and hence the overall phase margin of the op-amp. The effect of the RHP zero can be eliminated by using zero nulling resistor, or a trioded device whose gate voltage may exceed the supply voltage. Using a voltage buffer to block the feed-forward compensation current will lower the output swing. Indirect feedback compensation is discussed later in this chapter, which can be employed to move the RHP zero to LHP and achieves higher phase margins and better stability [6].

Figure 3-8 shows the circuit implementation of the NMC technique with a zero nulling resistor [13]. Here, the second stage is made non-inverting by using a current mirror at the cost of an additional delay in the forward path. The second stage current mirror also biases the third stage.

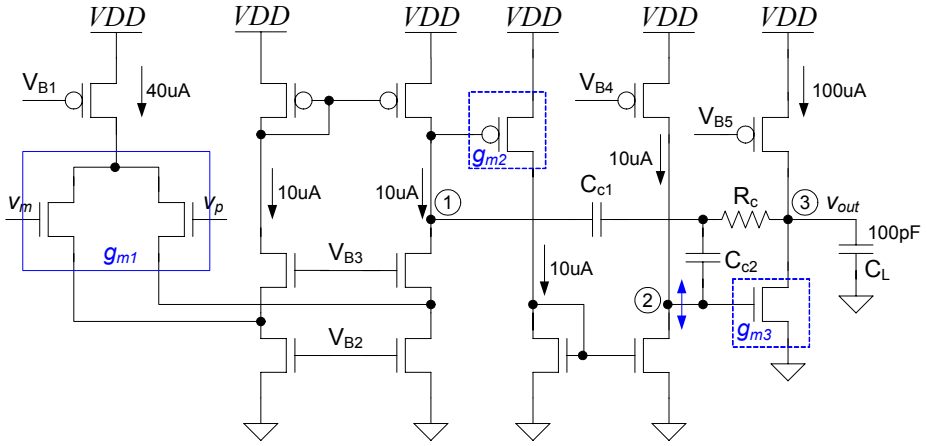

Figure 3-9. Schematic of a three-stage op-amp implemented using NMC and using a zero nulling resistor [13]. Here, $V_{B1\text{-}5}$ are the voltage references used to bias the op-amp.

A major limitation of the NMC topology is that a large amount of power is required to achieve stability as g_{m3} needs to be large. Further to that, the RHP zero reduces the phase margin and affects the stability of the op-amp. Also, more power may be consumed in realizing the numerous bias references used in the NMC topology.

Nested Gm-C Compensation

A modified version of the Nested Miller Compensation technique called Nested Gm-C Compensation (NGCC) has been proposed in [14]. Here feed-forward transconductances g_{mk}'s are employed to move the RHP zero to infinity as explained using the small

signal analysis later [6]. The block diagram for a three stage NGCC op-amp is shown in Figure 3-10.

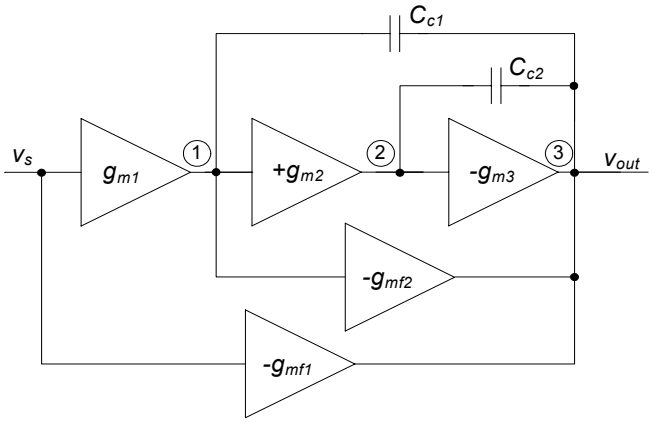

Figure 3-10. Block diagram of a three-stage op-amp with NGCC [14].

The small signal transfer function for the NGCC three-stage op-amp is given as [14]

$$\frac{v_{out}}{v_s} \approx -\frac{g_{m1}g_{m2}g_{m3} + sg_{m1}(g_{mf2} - g_{m2})C_{c2} + s^2(g_{mf1} - g_{m1})C_{c1}C_{c2}}{(R_1R_2R_3)^{-1} + sg_{m2}g_{m3}C_{c1} + s^2(g_{m3} + g_{mf2} - g_{m2})C_{c1}C_{c2} + s^3C_3C_{c1}C_{c2}} \quad (3.10)$$

It can be observed from Equation 3.10 that the zeros are eliminated if we force the conditions $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$. Also the expressions involving the poles of the transfer function are simplified by these conditions. This leads to the simplified small signal transfer function given as

$$\frac{v_{out}}{v_s} \approx -\frac{g_{m1}R_1g_{m2}R_2g_{m3}R_3}{(1 + sg_{m3}R_3g_{m2}R_2R_1C_{c1})\left(1 + \frac{sC_{c2}}{g_{m2}} + \frac{s^2C_{c2}C_3}{g_{m2}g_{m3}}\right)} \quad (3.11)$$

It can be observed that the denominator of Equation 3.11 is same as the denominator of Equation 3.2, only that we do not need the criterion $g_{m3} \gg g_{m2}$ anymore. This can potentially lead to lower power op-amp design when compared to the NMC op-amp topology [14].

Since the zeros have been eliminated, only the locations of the poles are given as

$$p_1 \approx -\frac{1}{g_{m3}R_3 g_{m2}R_2 R_1 C_{c1}} \tag{3.12}$$

With the assumption that $g_{m3} \gg g_{m2}$, we have the non-dominant poles given by [6]

$$p_2 \approx -g_{m2}/C_{c2}, \text{ and} \tag{3.13}$$

$$p_3 \approx -g_{m3}/C_3 \tag{3.14}$$

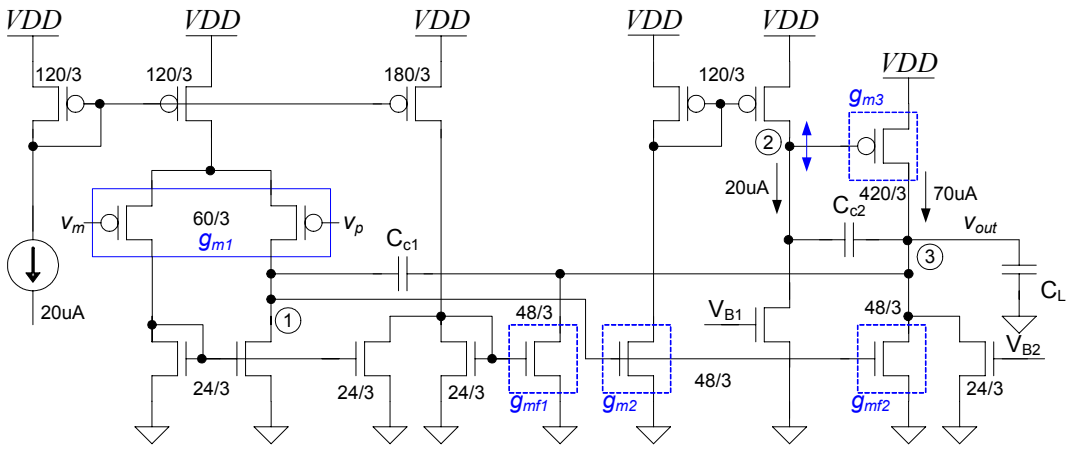

Figure 3-11. Schematic of a three-stage op-amp implemented using NGCC [14]. Here, $V_{B1,2}$ are the voltage references used to bias the op-amp.

Figure 3-11 shows a circuit implementation for a three-stage op-amp employing the NGCC scheme, which corresponds to the block diagram seen in Figure 3-10. Here, the

second gain stage is non-inverting and is realized using a current mirror, which in turn biases the third stage. Additional devices are used to create the forward transconductances, g_{mf1} and g_{mf2}, which intend to mirror the transconductances g_{m1} and g_{m2} respectively.

Although NGCC topology can lead to lower power op-amp designs compared to NMC, but it has serious limitations. Firstly it is difficult to realize the feed-forward transconductance (FTS) for the input stage, i.e. g_{mf1}, as it consumes more power and it is hard to have constant g_m value for rail to rail inputs. Secondly, since for class AB operation of the op-amp, g_{mf2} device is a power device which cancels the transconductance g_{m2} of the output stage. Now since the value of g_{mf2} changes by an order of magnitude while driving a large load, while g_{m2} will remain fixed. Thus the cancellation $g_{mf2} = g_{m2}$ will not hold all times and the compensation may break down during large signal amplification. Also extra bias current is required to realize FTS stages, which may not go well for low power op-amp design [15].

Reverse Nested Miller Compensation

Another compensation technique called Reverse Nested Miller Compensation (RNMC) is discussed in [18]. Here, when the third gain stage is non-inverting, the compensation capacitors can be reverse nested as shown in the block diagram in Figure 3-12. Here, the second and third stages need to be inverting and non-inverting respectively so as to achieve overall negative feedback compensation loops and hence pole-splitting. RNMC results in higher gain bandwidth for the op-amp as the output is not loaded by the inner compensation capacitor [19]. The small signal model for the RNMC three-stage op-amp is shown in Figure 3-13.

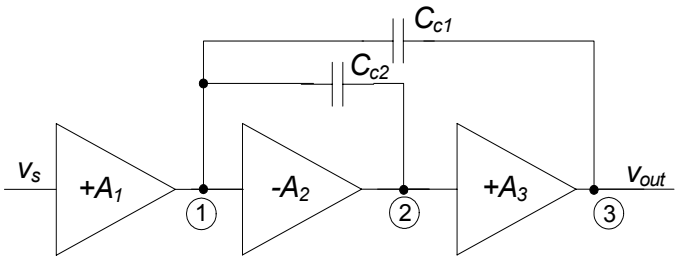

Figure 3-12. Block diagram of a reverse nested Miller compensated (RNMC) three-stage op-amp.

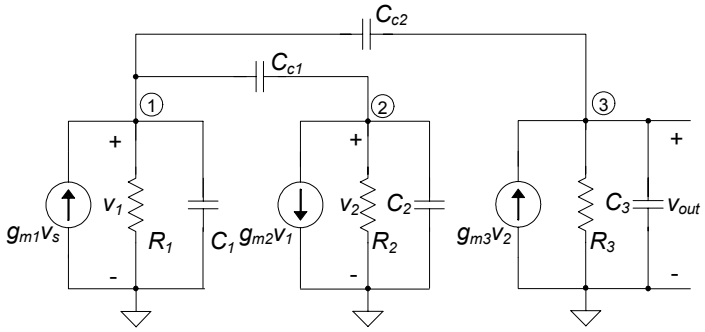

Figure 3-13. Small signal diagram for the RNMC three-stage op-amp [18].

On performing nodal analysis on the model seen in Figure 3-13, and applying the simplifying assumptions, we obtain the following small signal transfer function [18]

$$\frac{v_{out}}{v_s} \approx -A_v \frac{1-\left(\frac{C_{c1}}{g_{m2}}+\frac{C_{c2}}{g_{m2}g_{m3}R_2}\right)s-\frac{C_{c1}C_{c2}}{g_{m2}g_{m3}}s^2}{\left(1+\frac{s}{p_1}\right)\left[1+\left(\frac{C_{c1}C_3}{g_{m3}C_{c2}}-\frac{C_{c1}}{g_{m2}}+\frac{C_{c2}}{g_{m3}}\right)s+\frac{C_{c1}C_3}{g_{m2}g_{m3}}s^2\right]} \tag{3.15}$$

where the dc gain is given as $A_v = g_{m1}R_1g_{m2}R_2g_{m3}R_3$ and the dominant pole is given as

$$p_1 \approx -\frac{1}{g_{m3}R_3g_{m2}R_2R_1C_{c2}} \tag{3.16}$$

and the unity-gain frequency is

$$f_{un} \approx \frac{g_{m1}}{2\pi C_{c2}} \tag{3.17}$$

Note that the expressions for p_1 and f_{un} derived here are same as the expressions for NMC, only the labeling of C_{c1} and C_{c2} has been swapped to allow systematic drawing of the RNMC schematics.

The transfer function in Equation 3.15 also signifies presence of two zeros and two non-dominant poles.

The location of zeros are given as

$$z_{LHP} \approx -\left(\frac{g_{m3}}{C_{c2}} + \frac{1}{R_2C_{c1}}\right)\left[\sqrt{1 + \frac{4g_{m2}g_{m3}C_{c1}C_{c2}}{(g_{m3}R_2C_1 + C_{c2})^2}} + 1\right] \tag{3.18}$$

$$z_{RHP} \approx \left(\frac{g_{m3}}{C_{c2}} + \frac{1}{R_2C_{c1}}\right)\left[\sqrt{1 + \frac{4g_{m2}g_{m3}C_{c1}C_{c2}}{(g_{m3}R_2C_1 + C_{c2})^2}} - 1\right] \tag{3.19}$$

Also since $|z_{RHP}| < |z_{LHP}|$, the RHP zero appears at a lower frequency than the LHP zero and reduces the phase margin. Various methods have been reported to eliminate or cancel the RHP zero and improve the performance of the op-amp.

We could use two separate resistors to eliminate both the zeros, but retaining the LHP zero helps in improving the phase margin of the op-amp. A single resistor can be used

to eliminate only the RHP zero using the block diagram shown in Figure 3-14. Also, here a pole is cancelled with the LHP zero at $-\frac{g_{m2}}{C_{c2}}$, for $R_c = \frac{1}{g_{m2}}$ and $g_{m2} = g_{m3}$. The resulting op-amp small signal transfer function is given as

$$\frac{v_{out}}{v_{in}} = A_v \frac{1}{\left(1 - \frac{s}{p_1}\right)\left(1 + s\frac{C_{c1}C_3}{g_{m3}C_{c2}}\right)} \tag{3.20}$$

However, this requires the transconductances g_{m2} and g_{m3} to be greater than g_{m1} by an order of magnitude and hence this technique is impractical for lower power designs [18].

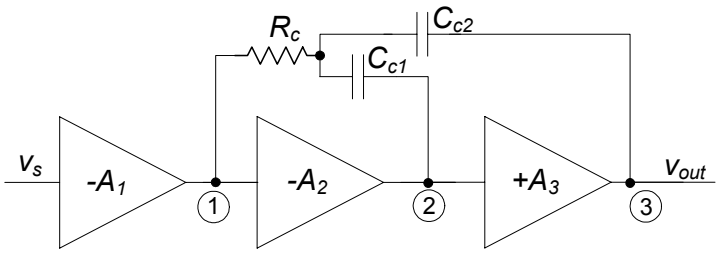

Figure 3-14. Elimination of RHP zero using a single zero nulling resistor [18].

Also, two voltage followers can be used to eliminate both the zeros, but it is advisable to use voltage follower only in the inner compensation loop to avoid reduction in output swing. In Figure 3-15 the RHP zero is eliminated using a voltage buffer (VF). the output resistance of the voltage follower is denoted as R_c. Another topology is shown in Figure 3-16, where a current follower (CF) is used to eliminate the RHP zero and improve the phase margin. The resistance looking into the current follower is denoted as R_c. In these techniques R_c is chosen as $R_c \geq \frac{\gamma}{g_{m3}}$, where $\gamma \geq 1$. This will require the buffer transcon-

ductance to be a scaled mirror of g_{m3}, which will necessitate large current in the buffer branch and thus increase power consumption [18].

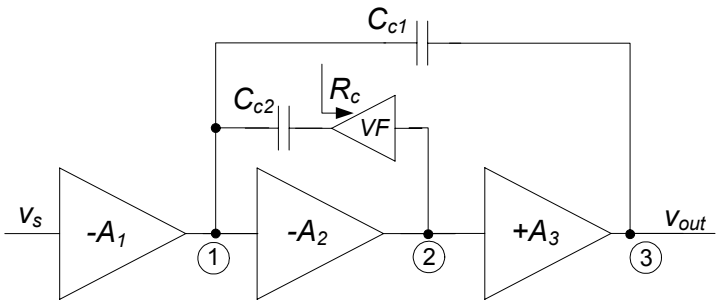

Figure 3-15. Elimination of RHP zero using a voltage follower [18].

Op-amps with phase margins of around $60°$ can obtained by using the techniques shown in Figures 3-15 and 3-16. A detailed derivation of pole-zero locations for the op-amps and their design guidelines are presented in [18].

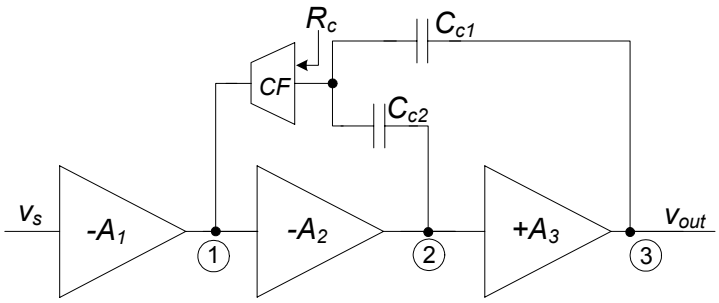

Figure 3-16. Elimination of RHP zero using a current follower [18].

Figure 3-17 depicts a circuit implementation for a three-stage op-amp designed using RNMC technique employing a voltage buffer for RHP zero cancellation [18]. Note that the small signal models employed to analyze such RNMC topologies, do not account for the extra forward-path delay arising due to the use of the current-mirror in the third (non-inverting) stage. Thus, the small signal analysis of the RNMC topologies may not accurately predict their stability.

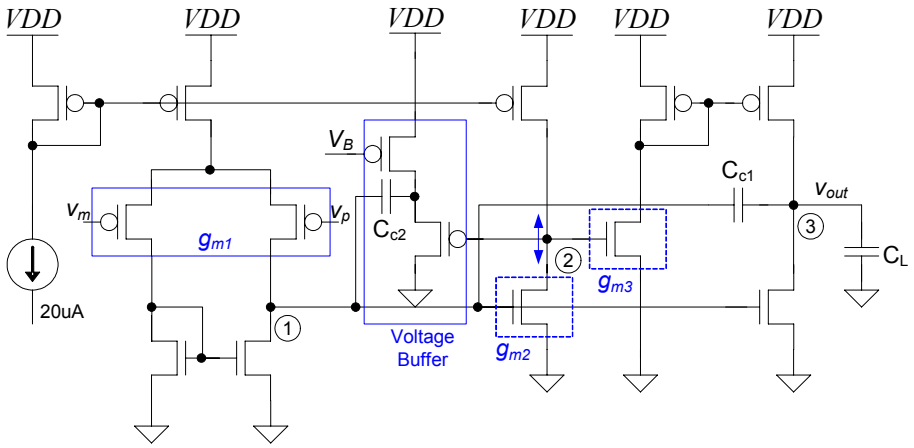

Figure 3-17. Schematic of a three-stage op-amp implemented using RNMC with a voltage follower [18].

Here, the third stage is non-inverting type and realized using a current mirror while the second gain stage is an inverting common source stage. Here, the common source second stage is used to bias the third gain stage. This method of biasing is not advisable for practical op-amp design as explained earlier.

RNMC with Pole-Zero Cancellation using Voltage Buffer and Resistor

An improved compensation method has been reported in [4], which employs a voltage buffer and resistor to achieve dual pole-zero cancellation. Again, as in RNMC, the third stage should be a non-inverting one while the second stage should be inverting. The block diagram of this topology is shown in Figure 3-18 and the schematic is illustrated in Figure 3-19. The use of a voltage buffer around the first stage is analogous to indirect compensation as discussed in chapter 2. A common gate stage can also be used to achieve similar results.

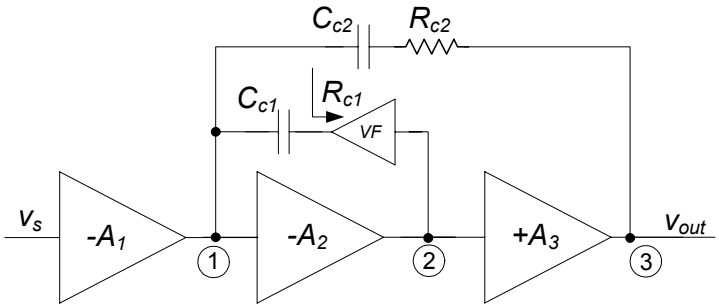

Figure 3-18. Block diagram of an op-amp employing RNMC using a voltage buffer and a resistor [4].

Here, the output resistance of the voltage buffer is represented as R_{c1} and an additional resistor R_{c2} is used in series with the compensation capacitor C_{c2}. The small signal transfer function for this topology is given as [4]

$$\frac{v_{out}}{v_s} \approx -A_v \frac{[1+(R_{c1}C_{c1}+R_{c2}C_{c2})s+R_{c1}C_{c1}R_{c2}C_{c2}s^2]}{\left(1-\frac{s}{p_1}\right)\left[1+\frac{C_{c1}}{g_{m3}C_{c2}}[C_3+C_{c2}(1+g_{m3}R_{c1})]s+\frac{R_{c2}C_{c1}C_3}{g_{m3}}s^2\right]\left[1+\frac{C_{c1}(R_{c1}+R_{c2})}{g_{m2}R_{c2}}s\right]} \tag{3.21}$$

By equating the coefficients of the second order polynomial in the numerator and the denominator, double pole-zero cancellation can be achieved. This leads to the design conditions

$$R_{c1} = \frac{C_3}{g_{m3}C_{c2}}, \text{ and} \tag{3.22}$$

$$R_{c2} = \frac{C_{c1}}{g_{m3}C_{c2}}\left(1 + \frac{C_3}{C_{c2}}\right) \tag{3.23}$$

Thus, by using the design Equations 3.22 and 3.23, and neglecting the effect of the parasitic poles, we obtain an almost $90°$ phase margin for a given load value C_3. Also we notice that the resistances R_{c1} and R_{c2} values are purely a function of real circuit parameters and independent of the parasitics. However, with process and temperature variations, exact pole-zero cancellation may not be achieved and the collocated pole-zero pair may form a doublet. Nevertheless if these pole-zero doublets are placed farther beyond the unity gain frequency, close to $90°$ phase margin can be achieved [4]. This constraint leads to the following condition on the compensation capacitor values

$$C_{c2} > \sqrt{\frac{2g_{m1}C_{c1}C_3}{g_{m3}}} \tag{3.24}$$

This condition also dictates the upper bound on the unity gain frequency of the op-amp, which is given as [4]

$$f_{un} < \frac{1}{2\pi}\sqrt{\frac{2g_{m3}}{g_{m1}C_3C_{c1}}} \tag{3.25}$$

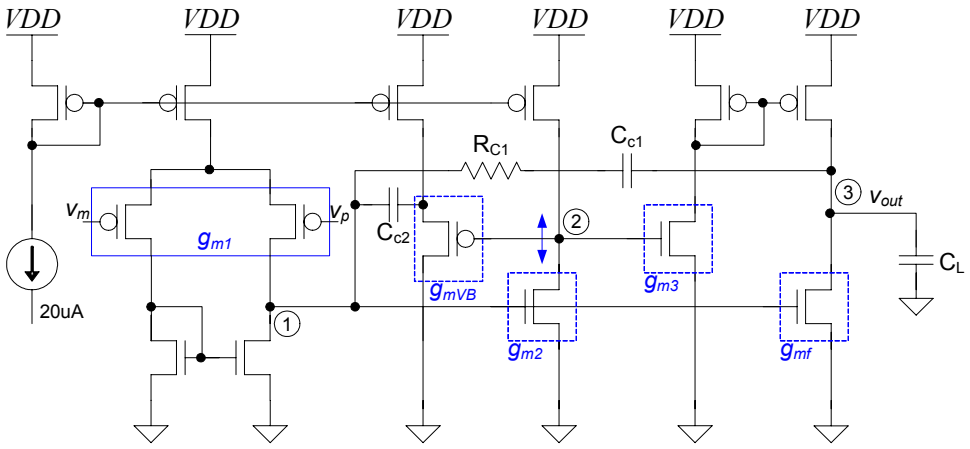

Figure 3-19. Schematic of a three-stage op-amp implemented using RNMC with a voltage buffer and a resistor [4].

This compensation technique promises an excellent phase margin of 90° for a RNMC topology. The limitations of this topology are that the third stage should always be non-inverting and additional bias current is required in the voltage buffer branch. Also the biasing scheme involving a common source second stage is not practical as discussed earlier.

Feedforward RNMC

A feed-forward variant of NMC has been proposed for RNMC topology in [19] and its termed as nested feedforward RNMC (shown in Figure 3-20). Here the conditions $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m3} - g_{m2}$ should be satisfied to cancel the RHP zeros. Again this topology ends up consuming more power in the feedforward transconductance stages and the compensation breaks down when g_{m3} varies by order of magnitude. Another topol-

ogy called crossed feedforward RNMC is proposed in [19], which also suffers from the same limitations.

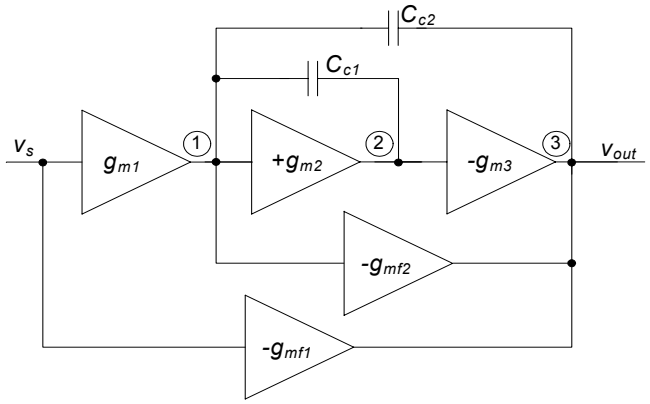

Figure 3-20. Block Diagram or an op-amp employing crossed feedforward RNMC [19].

Active-Feedback Compensation

Another multi-stage op-amp compensation scheme, called active feedback compensation, has been proposed in [22] and expounded upon in [23]. The block diagram for this compensation scheme is shown in Figure 3-21 and its circuit implementation is depicted in Figure 3-22. This technique essentially is a variant of NMC and uses Miller compensation between node-2 and node-3. A form of indirect compensation is used here to feedback the compensation current from node-3 to node-1. Also there is a feedforward transconductance, g_{mf}, connected from node-1 to node-3. In the block diagram, the high-gain block (HGB) is the cascade of additional gain-stages while the high-speed block (HSB) implements the compensation at high frequencies. Detailed expressions and design constraints for design of low-power op-amps using this technique can be found in [23]. However, the design constraints for this technique are complex and the resulting topology

consumes more power for realizing g_{mf} and g_{ma}. Moreover, the bias circuit used to realize the references used in the schematic shown in Figure 3-22 (bias circuit not shown here) consumes large amount of static power and occupies large layout area.

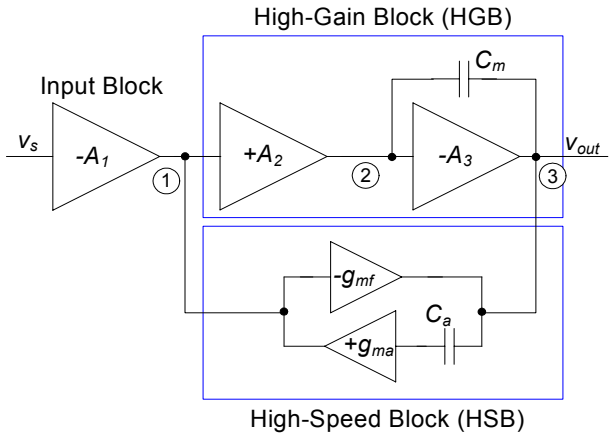

Figure 3-21. Block diagram of a three-stage opamp with active-compensation [23].

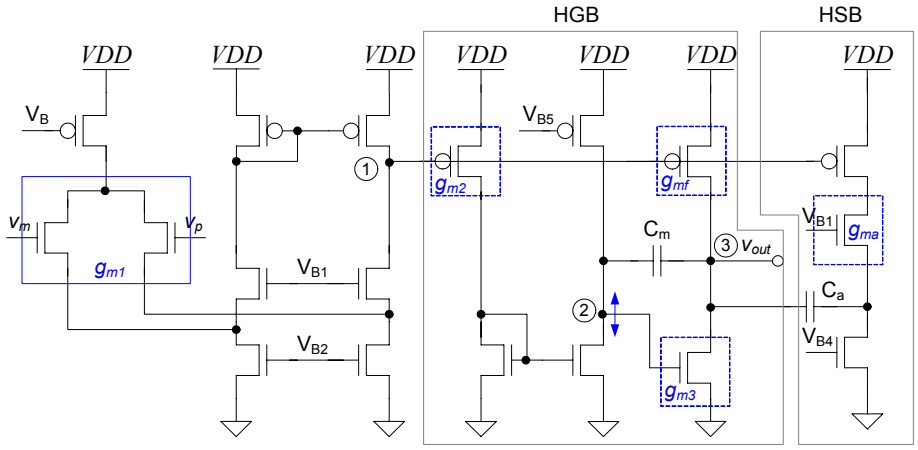

Figure 3-22. Schematic of an active-compensated three-stage op-amp [23]. The biasing circuit is not shown here.

A generalized indirect feedback compensation scheme is proposed and analyzed in the next section which can result in very low-power low-voltage multi-stage op-amps with improved stability.

Indirect Feedback Compensation

Three Stage Class A Op-Amp Design

The theory of indirect feedback compensation, developed in chapter 2, can be applied to three-stage op-amp design. As we know that, in the case of reversed nested compensation topologies, the output is not loaded by both of the compensation capacitors which leads to a larger unity gain frequency. Thus we start with an indirect compensated reverse-nested op-amp topology in order to develop low-power and low-voltage three-stage op-amp design techniques. Figure 3-23 shows the reverse nested indirect compensated class A three-stage op-amp. In this topology an NMOS diff-amp is cascaded with a PMOS diff-amp which are followed by a PMOS common-gate stage. The PMOS diff-pair in second stage employes wider devices[1] to increase the input common-mode range (CMR) of the second stage, so that it can incorporate the output range of the first stage. Split length diff-pairs are used for indirect compensation in order to achieve higher power supply rejection ratio (PSRR). Split length load topologies can also be used interchangeably if PSRR is not a concern. Further ideas on indirect compensation of three-stage op-amps are developed in this section by systematically analyzing this topology.

---

1. A wider diff-pair for the same bias current will have smaller overdrive voltage and hence wider input common range for the diff-amp stage [1].

A diff-amp is used in the second stage to ensure that the third (common source) stage is properly biased. The compensation capacitor Cc1 is used to indirectly feedback the compensation current (i_{c1}) from the output of the second stage (node-2) to the output of the first stage (node-1). Similarly, capacitor C_{c2} is used to indirectly feedback current i_{c2} from node-3 to node-1.

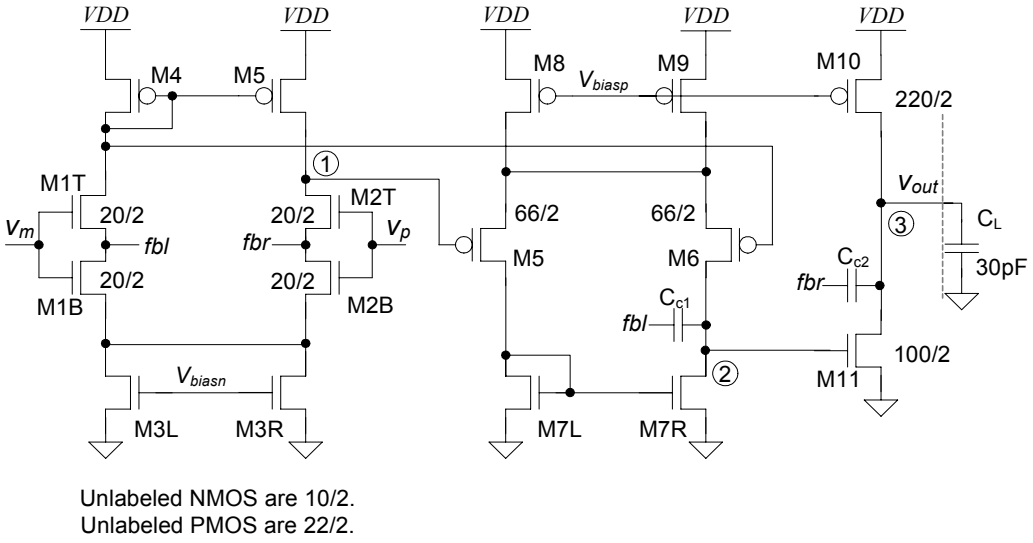

Figure 3-23. A low-power and low-VDD three-stage class A op-amp employing reversed nested indirect compensation.

Figure 3-24 illustrates the feedback compensation currents and the movement of the nodes when a positive input is applied. The feedback currents, i_{c1} and i_{c2}, are fed back in such a way that the respective loops have an overall 'negative feedback'. In other terms, analogous to the miller compensation case, an inversion is maintained between the node pair involved in the compensation. For example in Figure 3-24 the voltages at node-1 and

node-2 decrease together. Now if the feedback current i_{c1} is fed from node-2 to node '*fbr*', it will lead to positive feedback and the involved nodes may hit the power supply rails, causing the op-amp topology to fail. Instead the compensation current i_{c1} is fed back to node '*fbl*'. This inverts the sign of the current indirectly fed back to node-1 and creates an overall negative feedback loop. Following the same logic, as there is a small signal voltage inversion from node-1 to node-3, the compensation current i_{c2} from node-3 is indirectly fed back to node-1 through the low impedance node '*fbr*'.

As a rule of thumb, the compensation capacitance must be connected across two nodes which are moving in opposite direction i.e. have arrows of opposite direction (up or down) in Figure 3-24. This scheme leads to an overall negative feedback in the loops in the circuit, which is a prerequisite for stability. Figure 3-23 displays a block diagram for the presented op-amp, which further clarifies on how feedback compensation currents are fed back to node-1.

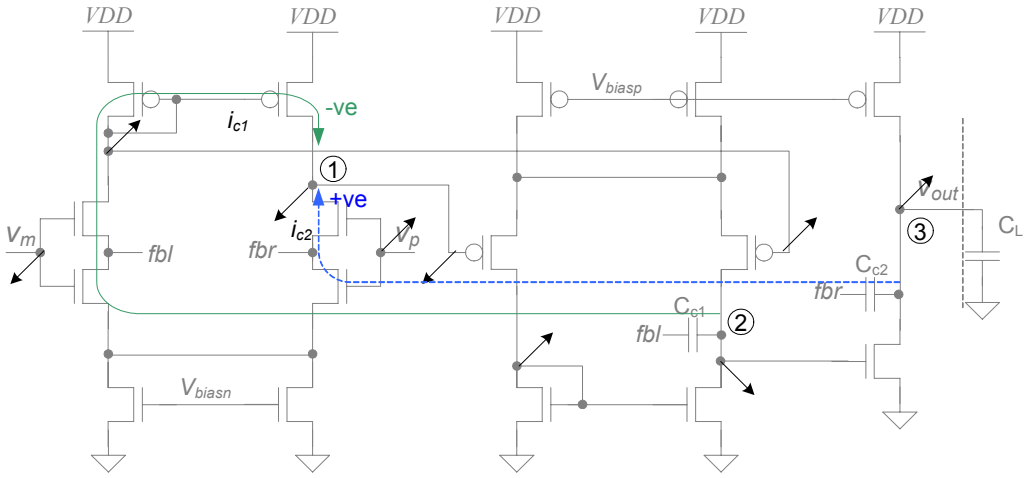

Figure 3-24. Three stage op-amp from Figure 3-23 with labelling showing feedback compensation currents and node movements. The circuit diagram is displayed in lighter shade so that the labels and arrows are clearly visible.

An obvious advantage of employing indirect feedback compensation is that, unlike in the reverse nested Miller compensation, the third stage need not always be non-inverting and also the second stage need not be always inverting. Indirect compensation can be easily achieved with a non-inverting second stage and an inverting third (output) stage by choosing appropriate signs of the feedback compensation currents as shown for i_{c1} and i_{c2} in the present topology. In fact, indirect compensation allows any permutation of the signs of the gains of the op-amp stages. Also the forward-path delay is minimized in the topology seen in Figure 3-23.

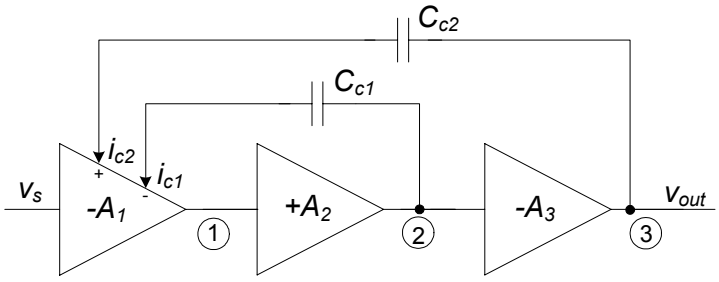

Figure 3-25. Block diagram for the indirect compensated three-stage op-amp shown in Figure 3-23.

The small signal model for the three-stage op-amp introduced in Figure 3-23 can be derived using the simple model, obtained for the two-stage split-length diff-pair topology in sub-section (see Figure 2-39). The small signal model for a generalized three-stage topology is shown in Figure 3-25. For the present topology, g_{mc1} and g_{mc2} are the transconductances of transistor M2T and M1T respectively and are both equal to $\sqrt{2}g_{m1}$. R_{c1} and R_{c2} are the resistances attached to the nodes *fbr* and *fbl* respectively which are both approx-

imately equal to $1/\sqrt{2}g_{m1}$ [2]. Also, the feedback compensation currents i_{c1} and i_{c2} are given as $i_{c1} = \frac{v_2}{1/sC_{c1} + R_{c1}}$ and $i_{c2} = \frac{v_{out}}{1/sC_{c2} + R_{c2}}$ respectively.

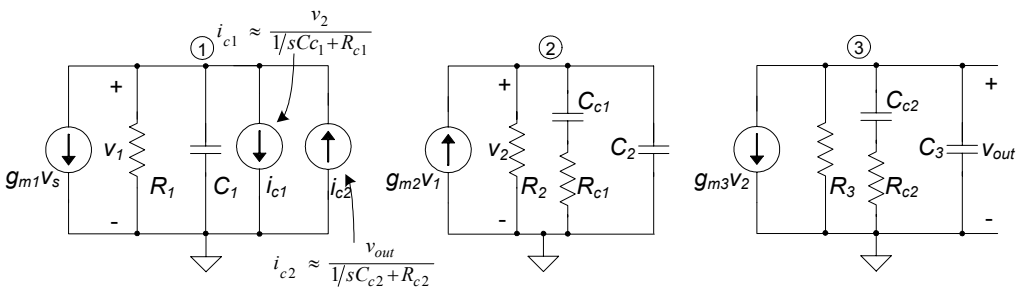

Figure 3-26. A generalized small signal model for the three-stage op-amp employing reverse nested indirect compensation.

Now, applying nodal analysis on the small signal model presented in Figure 3-26, we get the following three equations for each of the nodes.

$$g_{m1}v_s + \frac{v_1}{R_1} + v_1 sC_1 + \frac{v_2}{1/sC_{c1} + R_{c1}} - \frac{v_{out}}{1/sC_{c2} + R_{c2}} = 0 \tag{3.26}$$

$$-g_{m2}v_1 + \frac{v_2}{R_2} + \frac{v_2}{1/sC_{c1} + R_{c1}} + v_2 sC_2 = 0 \tag{3.27}$$

$$g_{m3}v_2 + \frac{v_3}{R_3} + \frac{v_{out}}{1/sC_{c2} + R_{c2}} + v_{out} sC_3 = 0 \tag{3.28}$$

2. $\frac{1}{g_{mp}} \| \left(2 \cdot \frac{1}{\sqrt{2}g_{mp}}\right) = \frac{1}{\sqrt{2}g_{mp}}$

Simultaneously solving Equations 3.26-3.28, we get the following small signal transfer function.

$$\frac{v_{out}}{v_s} = A_v\left(\frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5}\right) \tag{3.29}$$

where the transfer function coefficients are given as

$$A_v = g_{m1}R_1 g_{m2}R_2 g_{m3}R_3 \tag{3.30}$$

$$b_0 = 1 \tag{3.31}$$

$$b_1 = R_{c1}C_{c1} + R_{c2}C_{c2} \tag{3.32}$$

$$b_2 = R_{c1}C_{c1}R_{c2}C_{c2} \tag{3.33}$$

$$a_0 = 1 \tag{3.34}$$

$$\begin{aligned} a_1 = {} & g_{m2}R_2 g_{m3}R_3 R_1 C_{c2} + g_{m2}R_2 R_1 C_{c1} + R_2 C_{c1} + R_3 C_{c2} \\ & + R_{c1}C_{c1} + R_{c2}C_{c2} + R_1 C_1 + R_2 C_2 + R_3 C_3 \end{aligned} \tag{3.35}$$

$$\begin{aligned} a_2 = {} & g_{m2}R_2 g_{m3}R_3 R_1 C_{c2} R_{c1} C_{c1} + g_{m2}R_2 R_1 C_{c1}(R_3 C_3 + R_{c2}C_{c2} + R_3 C_{c2}) \\ & + R_3 C_3(R_{c1}C_{c1} + R_{c2}C_{c2} + R_1 C_1 + R_2 C_2 + R_2 C_{c1}) \\ & + R_2 C_2(R_{c1}C_{c1} + R_{c2}C_{c2} + R_1 C_1 + R_3 C_{c2}) \\ & + R_1 C_1(R_{c1}C_{c1} + R_{c2}C_{c2} + R_2 C_{c1} + R_3 C_{c2}) \\ & + R_{c1}C_{c1}(R_{c2}C_{c2} + R_3 C_{c2}) + R_2 C_{c1} C_{c2}(R_2 + R_3) \end{aligned} \tag{3.36}$$

$$\begin{aligned} a_3 = {} & g_{m2}R_2 R_1 C_{c1} R_2 C_{c2} + R_3 C_3 R_{c1} C_{c1}(R_1 C_1 + R_2 C_2 + R_{c2}C_{c2} + R_2 C_{c1}) \\ & + R_3 C_3 R_{c2} C_{c2}(R_1 C_1 + R_2 C_2 R_2 C_{c1}) + R_3 C_3 R_2 C_2 R_1 C_1 \\ & + R_2 C_2 R_{c1} C_{c1}(R_1 C_1 + R_{c2}C_{c2} + R_3 C_{c2}) + R_2 C_2 R_1 C_1 R_3 C_{c2} \\ & + R_1 C_1(R_{c1}C_{c1}(R_{c2}C_{c2} + R_3 C_{c2}) + R_2 C_{c1} R_3 C_{c2} + R_2 C_{c1} R_{c2} C_{c2}) \end{aligned} \tag{3.37}$$

$$\begin{aligned} a_4 = {} & R_3 C_3(R_{c1}C_{c1}(R_{c2}C_{c2}(R_1 C_1 + R_2 C_2) + R_1 C_1 R_2 C_2)) \\ & + R_3 C_3(R_{c2}C_{c2} R_1 C_1(R_2 C_2 + R_2 C_{c1})) \\ & + R_2 C_2 R_1 C_1 R_{c1} C_{c1}(R_{c2}C_{c2} + R_3 C_{c2}) \end{aligned} \tag{3.38}$$

$$a_5 = R_1C_1R_2C_2R_3C_3R_{c1}C_{c1}R_{c2}C_{c2} \tag{3.39}$$

In order to simplify the above complex expressions we can conveniently apply the approximations $g_{mk}R_k \gg 1, k = 1, 2, 3; C_3 \approx C_L; C_{c1}, C_{c2}, C_3 \gg C_1, C_2$, and obtain the following modified coefficients given as

$$b_0 = 1 \tag{3.40}$$

$$b_1 = R_{c1}C_{c1} + R_{c2}C_{c2} \tag{3.41}$$

$$b_2 = R_{c1}C_{c1}R_{c2}C_{c2} \tag{3.42}$$

$$a_0 = 1 \tag{3.43}$$

$$a_1 \approx g_{m2}R_2g_{m3}R_3R_1C_{c2} \tag{3.44}$$

$$a_2 \approx g_{m2}R_2g_{m3}R_3R_1C_{c2}R_{c1}C_{c1} + g_{m2}R_2R_1C_{c1}(R_3C_3 + R_{c2}C_{c2} + R_3C_{c2}) \tag{3.45}$$

$$a_3 \approx g_{m2}R_2R_1C_{c1}R_2C_{c2}R_3C_3 \tag{3.46}$$

$$a_4 \approx R_3C_3(R_{c1}C_{c1}R_{c2}C_{c2}(R_1C_1 + R_2C_2) + R_{c2}C_{c2}R_1C_1R_2C_{c1}) \tag{3.47}$$

$$a_5 = R_1C_1R_2C_2R_3C_3R_{c1}C_{c1}R_{c2}C_{c2} \tag{3.48}$$

The numerator of the small signal transfer function in Equation 3.29 is a polynomial of second order with positive coefficients which implies the presence of two LHP zeros.

The locations of the LHP zeros are simply evaluated as

$$z_1 = -\frac{1}{R_{c1}C_{c1}} \tag{3.49}$$

$$z_2 = -\frac{1}{R_{c2}C_{c2}} \tag{3.50}$$

Also, the denominator of the small signal transfer function is a polynomial of fifth order with positive coefficients which implies the presence of five LHP poles.

With the assumption that $|p_1| \gg |p_k|$, k=2 to 5, the dominant real pole is given as

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m3}R_3g_{m2}R_2R_1C_{c2}} \tag{3.51}$$

The unity gain frequency of the op-amp can be estimated as

$$f_{un} = \frac{|p_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_{c2}} \tag{3.52}$$

Here, the unity gain frequency is only dependent upon the compensation capacitance C_{c2} as output node is only loaded by C_{c2} besides the load C_3.

Now, we can use the condition

$$\frac{a_1}{a_2}, \frac{a_2}{a_3} \ll \frac{a_3}{a_4}, \frac{a_4}{a_5} \tag{3.53}$$

which implies the parasitic poles p_4 and p_5 arising due to the contribution from the inner low impedance nodes, used for indirect compensation, are far away from the non-dominant poles p_2 and p_3, i.e. $|p_2|, |p_3| \ll |p_4|, |p_5|$. It can easily be shown that the inequality 3.53 holds when $C_3 \gg C_k$, where C_k stands for all the internal parasitic capacitances. This is true for all the modern deep-submicron CMOS processes, which we intend to use for the multi-stage op-amp design.

The parasitic poles p_4 and p_5 lie close to the mirror poles arising due to the f_T limitation of the devices used in the op-amp. Thus, the denominator, D(s), of the small signal transfer function can be approximated as

$$D(s) \approx \left(1 + \frac{a_0}{a_1}s\right)\left(1 + \frac{a_2}{a_1}s + \frac{a_3}{a_1}s^2\right)\left(1 + \frac{a_4}{a_3}s + \frac{a_5}{a_3}s^2\right) \tag{3.54}$$

Now we have two conditions for determining the non-dominant pole locations which are explained in the following sub-sections.

Design with Pole-Zero Cancellation

The two LHP zeros can be used to cancel the non dominant poles p_2 and p_3. This can be achieved by equating the respective quadratic terms as shown below

$$1 + b_1 s + b_2 s^2 = 1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2 \tag{3.55}$$

Thus the conditions $b_1 = a_2/a_1$ and $b_2 = a_3/a_1$ must be satisfied in order to achieve pole-zero cancellation. The first condition $b_1 = a_2/a_1$ leads to

$$R_{c2}C_{c2} = \frac{C_{c1}}{C_{c2}}\left(\frac{R_3C_3 + (R_3 + R_{c2})C_{c2}}{g_{m3}R_3}\right) \tag{3.56}$$

or

$$R_{c2} \approx \frac{C_{c1}}{C_{c2}^2 g_{m3}}(C_3 + C_{c2}) \tag{3.57}$$

And the second condition $b_2 = a_3/a_1$, results in the following equation

$$R_{c1} \approx \frac{C_3}{g_{m3}C_{c2}} \tag{3.58}$$

The values of resistances R_{c1} and R_{c2} are estimated using Equations 3.58 and 3.56 respectively. These resistance values can realized by using additional resistance in series with the compensation capacitors C_{ck}. Thus we also have the limitation that $R_{ck} > \frac{1}{\sqrt{2}g_{m1}}$, as the value of R_{ck} can't be less than the series resistance offered by the internal nodes *fbl* or *fbr*.

The poles p_2 and p_3 are real and spaced apart with the locations at

$$p_2 \approx z_1 \approx -\frac{1}{R_{c1}C_{c1}} = -\frac{g_{m3}C_{c2}}{C_3C_{c1}} \tag{3.59}$$

$$p_3 \approx z_2 \approx -\frac{1}{R_{c2}C_{c2}} = -\frac{g_{m3}C_{c2}}{C_{c1}(C_3 + C_{c2})} \tag{3.60}$$

Also, we can observe that for a large load capacitance when $C_3 \gg C_{c2}$ we have $p_2 \approx z_1 \approx p_3 \approx z_2$, which implies that the non-dominant pole-zero doublets appear close together in the frequency domain. This arrangement of the non-dominant poles and zeros shown in Figure 3-27 is the optimal pole-zero constellation for a multi-stage op-amp for low power consumption.

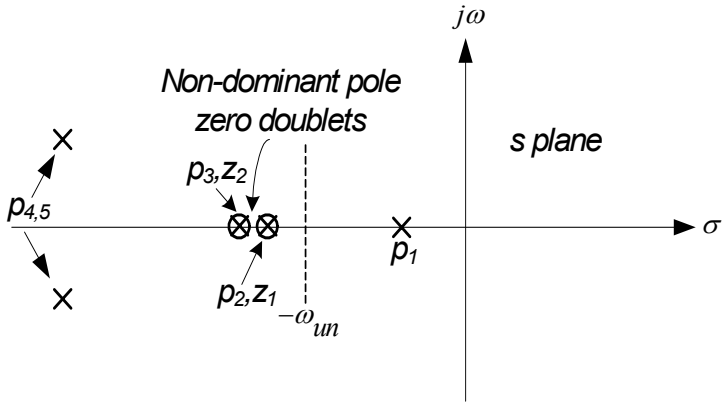

Figure 3-27. S-plane plot for the indirect-compensated three-stage op-amp designed with pole-zero cancellation method.

The parasitic poles p_4 and p_5 are real when the condition $a_4^2 > 4a_3a_5$ is satisfied. This translates into the criterion that $R_{c1}R_{c2} > g_{m2}R_2^3\frac{C_2}{C_1}$. Then the parasitic poles p_4 and p_5 can be approximated as

$$p_4 \approx -\frac{a_3}{a_4} \approx -\frac{g_{m2}R_2}{R_{c2}C_1} \tag{3.61}$$

$$p_5 \approx -\frac{a_4}{a_5} = -\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + \frac{1}{R_{c1}C_2}\right] \tag{3.62}$$

If $R_{c1}R_{c2} < g_{m2}R_2^3\frac{C_2}{C_1}$, then the conjugate poles p_4 and p_5 are located at

$$\mathrm{Re}(p_{4,5}) \approx -\sqrt{\frac{a_3}{a_5}} = -\sqrt{\frac{g_{m2}R_2}{R_{c1}C_1R_{c2}C_2}} \approx -\frac{g_{m3}C_{c2}}{C_3}\sqrt{\frac{g_{m2}R_2C_{c2}}{C_1C_2C_{c1}}} \tag{3.63}$$

The conjugate poles $p_{4,5}$ can peak the frequency magnitude response, when using processes with large parasitics, and can cause instability in the designed op-amps. As a rule of thumb, the op-amp will be stable if the peak power due to conjugate poles is less than -10 dB.

It is important to realize that perfect pole-zero cancellation is impossible to achieve as numerous approximations have been made to arrive at Equations 3.55 and 3.56. Besides, with process and temperature variations the locations of poles and zeros are likely to vary. But even with these variations the pole-zero pairs remain ‘collocated’ and form pole-zero doublets. The frequency response of a pole-zero doublet is very close to that of the cancelled pole by a zero. Even so, the pole-zero doublets have been reported to degrade time domain settling of the op-amp, if the doublet is located at a frequency less than the unity gain frequency [4]. Thus, the pole-zero doublets should be placed at a frequency higher

than the unity gain frequency (f_{un}) of the op-amp. This leads to another constraint for unconditional time-domain stability given as

$$p_2, z_1, p_3, z_2 > \frac{g_{m1}}{C_{c2}} \tag{3.64}$$

which translates into the following lower bound on the capacitor C_{c2}, given as

$$C_{c2} > \sqrt{\frac{g_{m1}}{g_{m3}} C_3 C_{c1}} \tag{3.65}$$

This lower bound on C_{c2} can be satisfied even with low values of C_{c1}. This also sets an upper limit on the unity gain frequency of the op-amp, which is given as

$$f_{un} < \frac{1}{2\pi} \sqrt{\frac{g_{m3}}{g_{m1} C_3 C_{c1}}} \tag{3.66}$$

The small signal transfer function after pole-zero cancellation is given as

$$\frac{v_{out}}{v_s} \approx \frac{-A_v}{\left(1 - \frac{s}{p_1}\right)\left(1 + \frac{a_4}{a_3} s + \frac{a_5}{a_3} s^2\right)} \approx \frac{-A_v}{\left(1 - \frac{s}{p_1}\right)} \text{ for } f \ll f_T \tag{3.67}$$

The phase margin (Φ) for the pole-zero cancelled three-stage op-amp is given as

$$\Phi = 90° - \arctan\left(\frac{\frac{2\pi f_{un}}{f_{p_{4,5}} Q_{4,5}}}{1 - \left(\frac{2\pi f_{un}}{f_{p_{4,5}}}\right)^2}\right) \tag{3.68}$$

where the quality factor $Q_{4,5}$ is defined as

$$Q_{4,5} = \frac{\sqrt{a_3 a_5}}{a_4} = \sqrt{\frac{g_{m2} R_2}{R_{c1} R_{c2}}} \left(\frac{1}{\frac{1}{R_1}\sqrt{\frac{C_1}{C_2}} + \frac{1}{R_2}\sqrt{\frac{C_2}{C_1}}}\right) \tag{3.69}$$

Thus, the resulting small signal transfer function looks like a single dominant pole response with almost 90° phase margin, and an R-C circuit like settling in the time domain.

A three-stage op-amp was designed using the topology shown in Figure 3-23, by using the pole-zero cancellation method. Using the compensation capacitor values C_{c1}=1pF and C_{c2}=2pF, yields the values $R_{c1} = 7.65\text{K}\Omega$ and $R_{c2} = 4.08\text{K}\Omega$. The values of R_{c1} and R_{c2} are obtained by connecting series resistors with the capacitors C_{c1} and C_{c2}. Figure 3-28 shows the modified pole-zero cancelled topology employing resistors. Here the additional resistors are estimated as $R_{kc} = R_{ck} - \frac{1}{\sqrt{2}g_{m1}}$, k=1,2.

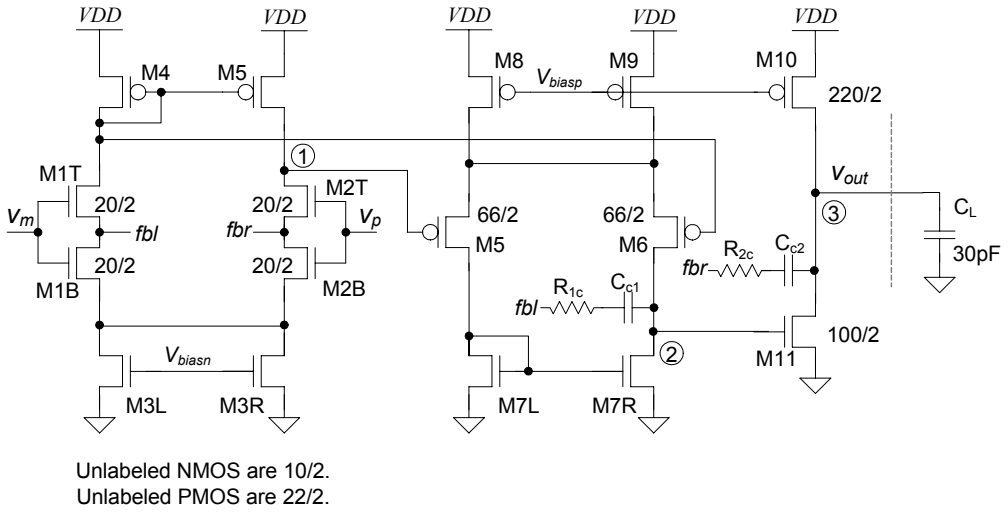

Figure 3-28. Modified three-stage op-amp achieving pole-zero cancellation by using series resistors with compensation capacitors.

Although this pole-zero cancellation approach results in excellent phase margin, its major limitation is that the pole-zero cancellation can only be achieved for a particular value of load capacitance $C_3 \approx C_L$. Large variations in value of load may render the three-

stage op-amp unstable. However, this limitation applies to all the multi-stage op-amp design techniques discussed so far. This approach is suitable for scenarios where the load capacitance is known and the variations in load are bounded, which is the case in many on-chip op-amps.

Figure 3-29 shows the numerically simulated response of the three-stage op-amp using MATLAB and employing the model shown in Figure 3-26. The MATLAB code for numerical simulation of the designed three-stage op-amps is provided in appendix A.

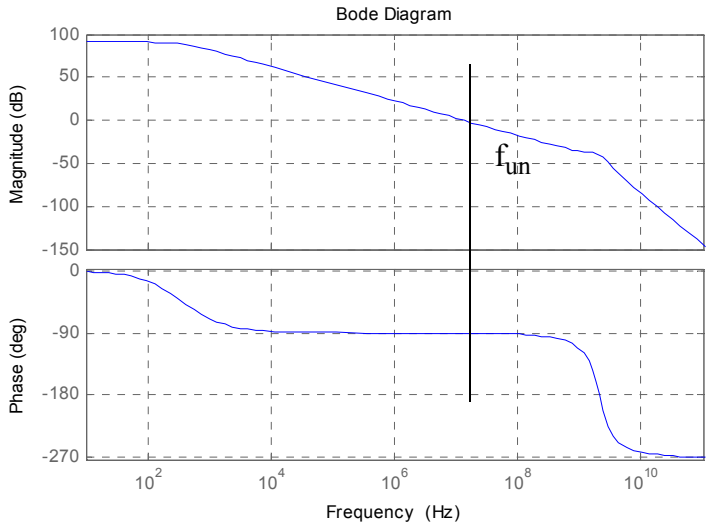

Figure 3-29. Numerically simulated frequency response of the pole-zero cancelled three-stage op-amp using the model shown in Figure 3-26. Here the op-amp unity gain frequency, f_{un}=30MHz and the phase margin, PM=90° .

Figures 3-30 and 3-31 demonstrate the pol-zero cancellation (or rather collocation) on a pole-zero plot for the op-amp small signal transfer function.

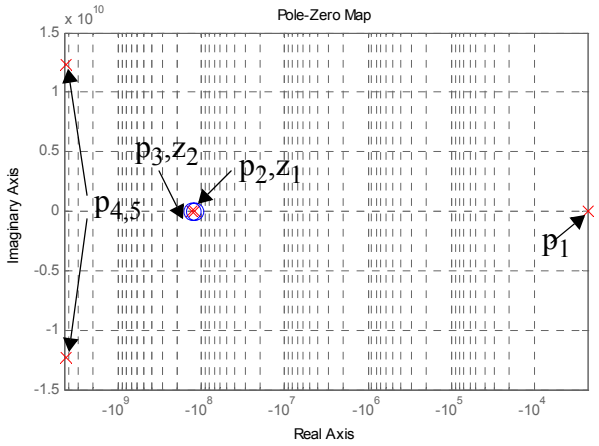

Figure 3-30. pole-zero plot of the three-stage opamp in Figure 3-28. Here the conjugate poles $p_{4,5}$ are the parasitic poles which lie close to the mirror poles.

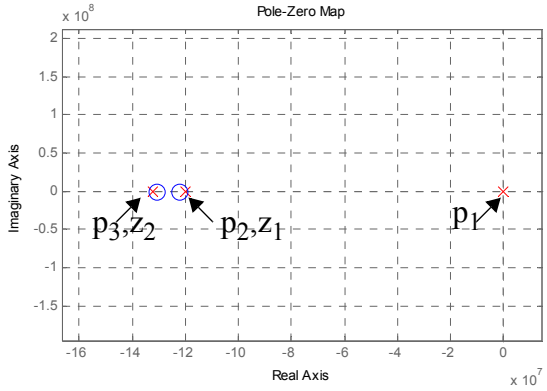

Figure 3-31. Magnified view of the pole-zero plot showing the non-dominant pole-zero cancellation.

Figure 3-29 displays the SPICE simulated frequency response of the three-stage op-amp shown in Figure 3-28. The numerical and SPICE simulated open loop DC gains

(=90dB) and unity gain frequencies (=22MHz) are in close conformity with each other. The op-amp phase margin here is close to $90°$.

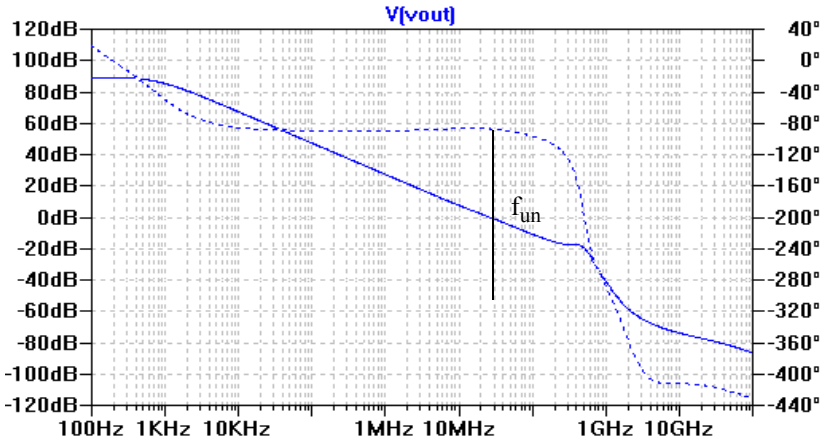

Figure 3-32. SPICE simulated frequency response for the op-amp seen in Figure 3-28. Here, f_{un}=30MHz and the phase margin, PM=$89°$, which are very close to the values obtained by the numerical simulations.

Figure 3-29 shows the transient small step input response for the three-stage op-amp. The simulated settling time is around 60ns. Even though the phase margin is close to $90°$, the small step input response shows an overshoot, which is attributed to the presence of conjugate poles $p_{4,5}$ a decade later in the frequency domain. These effects should be less prominent in the modern sub-100nm CMOS processes with smaller parasitics.

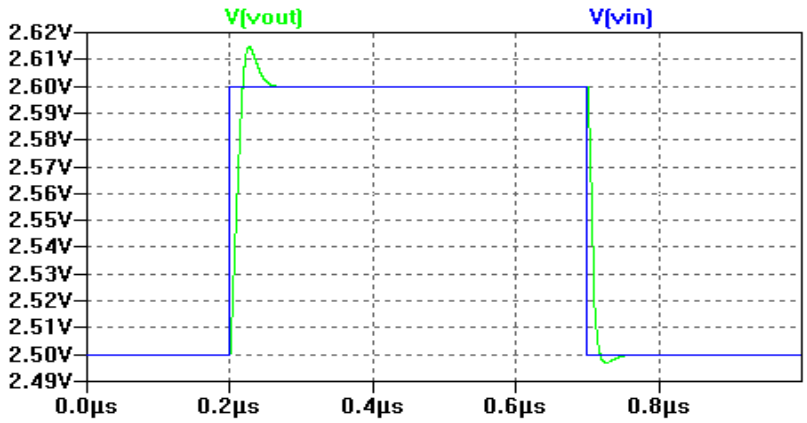

Figure 3-33. Small step transient response for the three-stage op-amp seen in Figure 3-28. Here the settling time, t_s=70ns.

The pole-zero cancellation technique has been observed through simulations to be highly robust to as much as 50% process variations in compensation resistances and capacitances, and the load capacitance and with wide variations in temperature. Monte-Carlo simulations can be performed for heuristic verification of the op-amp sensitivity to process, voltage and temperature variations.

Design without Pole-Zero Cancellation

If pole-zero cancellation is not employed, we can estimate the independent locations of the poles. Since, the locations of the poles and zeros are functions of circuits parameters and are intertwined, its hard to define the location of a pole or zero without affecting the other. The availability of more degrees of freedom makes the task of designing a three-stage op-amp without pole-zero cancellation difficult.

In order to find the locations of non-dominant poles p2 and p3, we need to estimate the roots of the expression $\left(1+\frac{a_2}{a_1}s+\frac{a_3}{a_1}s^2\right)$. The poles are real and spaced wide apart if $a_2^2 \gg 4a_1a_3$, which translates into the following condition

$$\frac{g_{m3}}{C_3} \gg \frac{4R_2}{R_{c1}^2 C_{c1}} \tag{3.70}$$

This implies that larger amount of power is burnt in the third stage to keep g_{m3} high. The widely spaced poles locations for this case are given as

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{1}{R_{c1}C_{c1}(1+\alpha_1)}, \quad \text{where } \alpha_1 = \frac{R_1(C_3+C_{c2})}{g_{m3}R_{c1}} \tag{3.71}$$

$$p_3 \approx -\frac{a_2}{a_3} = -\left[\frac{g_{m3}R_{c1}}{C_3R_2}+\frac{1}{R_2C_{c2}}+\frac{1}{R_2C_3}\left(1+\frac{R_{c2}}{R_3}\right)\right] \tag{3.72}$$

For $\frac{g_{m3}}{C_3} < \frac{4R_2}{R_{c1}^2 C_{c1}}$, the location of conjugate non-dominant poles $p_{2,3}$ is given as

$$Re(p_{2,3}) = -\sqrt{\frac{a_1}{a_3}} = -\sqrt{\frac{g_{m3}}{C_3R_2C_{c1}}} \tag{3.73}$$

The locations of the parasitic poles p_4 and p_5 is given using Equations 3.61-3.63. From Equation 3.71, we can deduce that $p_2 \approx \frac{z_1}{1+\alpha_1}$, which implies that the pole p_2 moves along with zero z_1 and appears earlier in frequency, and form a loosely coupled pole-zero doublet. If this p_2-z_1 doublet is allowed inside the unity gain frequency (f_{un}), at the risk of poor transient settling, it can degrade the phase margin of the op-amp. Also g_{m3} should be large enough to keep the pole p_3 away from f_{un}.

Figure 3-34 shows another three-stage indirect compensation op-amp topology using cascade of two NMOS type diff-amps followed by a PMOS common source stage. Design for variable load capacitance has been applied to this topology. The unity gain frequency is set lower at 10MHz to allow larger movement of p_3 and to keep p_2 out of f_{un}. The compensation capacitance values are set as C_{c1}=0.5pF and C_{c2}=3pF. Here, resistors are not used in series with the compensation capacitors although they can be used to move the zero to lower frequency if needed.

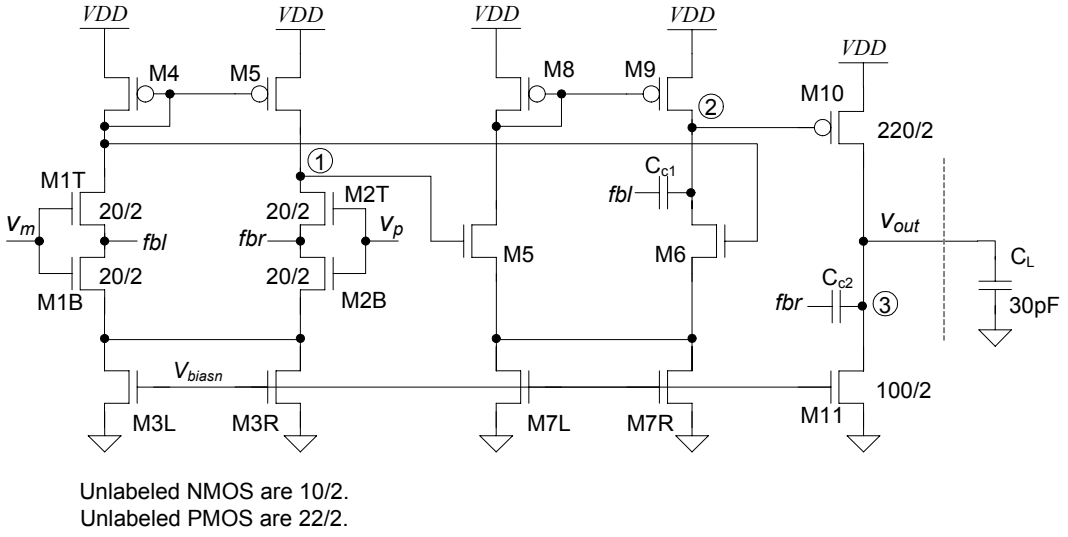

Figure 3-34. A three-stage indirect compensated op-amp topology designed without pole-zero cancellation.

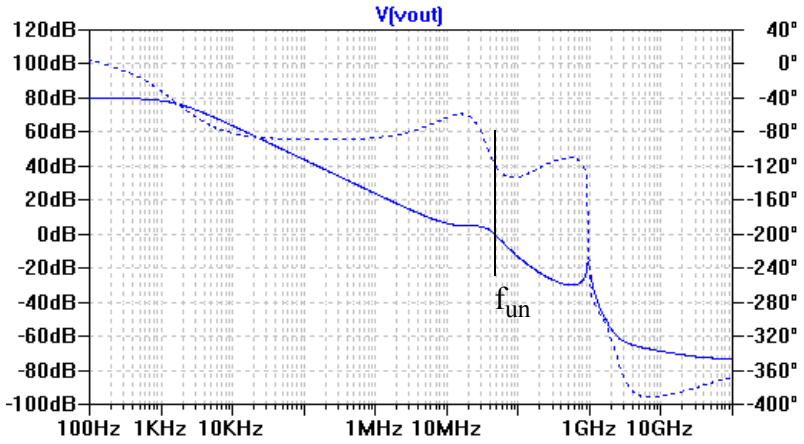

Figure 3-35. SPICE simulated frequency response for the op-amp seen in Figure 3-28. Here the op-amp unity gain frequency, f_{un}=30MHz and the phase margin, PM=60° .

Figure 3-32 displays the SPICE simulated frequency response of the three-stage op-amp shown in Figure 3-34. The op-amp phase margin is close to 60° . The small step transient response in Figure 3-36 shows characteristic settling for the phase margin of 60° , but the settling time is still fast at 80ns.

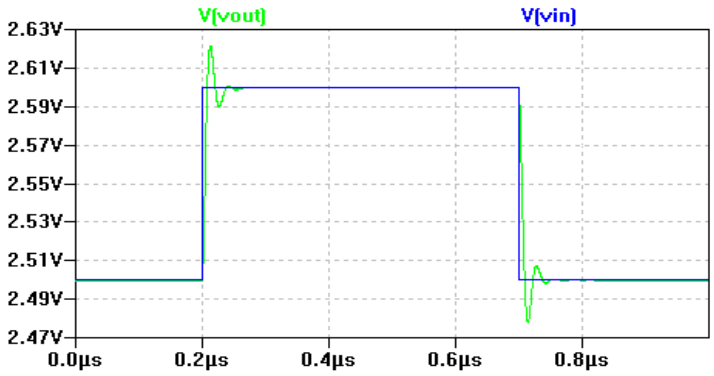

Figure 3-36. Small step transient response for the three-stage op-amp seen in Figure 3-28. Here the settling time, t_s=80ns

Three Stage Class AB Op-Amp Design

The theory developed in the last section can easily be extended to the design of Class AB three-stage indirect compensated op-amps. An extremely low-power pseudo class AB op-amp displayed Figure 3-37 in can be derived from the class A three-stage op-amp seen in Figure 3-24. The output of the first stage can be used to drive the gate of the PMOS M10. Now, the gate of M10 is biased around V_{biasp} and the gate of M11 is biased at V_{biasn}, and they move almost together emulating a bias battery for the output stage. We can observe that there are two gain paths for the signal, first $A_1A_2A_3$ and another A_1A_3, where A_k is the gain for the k-th stage. There is a crossover distortion for large signals when the gain paths are swapped by shutting either of the M10 or M11 devices. However, the large forward gain helps in reducing the distortion. The block diagram for this op-amp is shown in Figure 3-38. Here A_{3p} is the gain due to the PMOS M10 and A_{3n} is the gain contribution from NMOS M11.

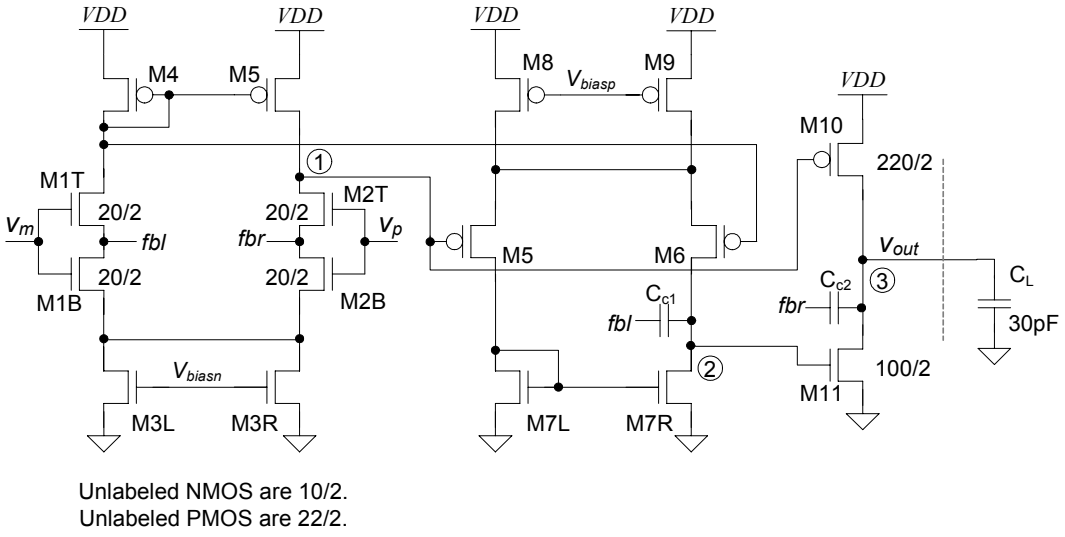

Figure 3-37. A three-stage indirect compensated Class AB op-amp.

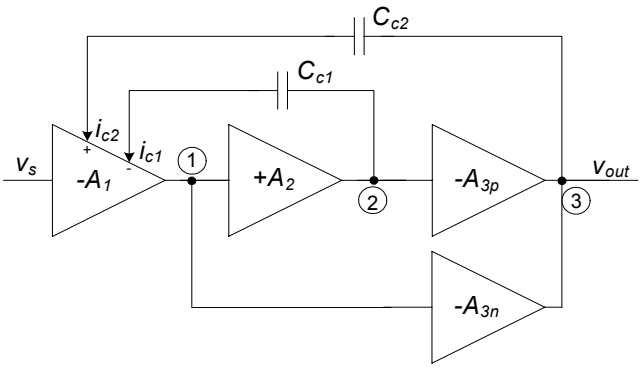

Figure 3-38. Block diagram for the three stage class AB op-amp seen in Figure 3-37.

We assume that the devices M10 and M11 are biased for the same transconductance defined as g_{m3}. The small signal model the present class AB op-amp is shown in Figure 3-39.

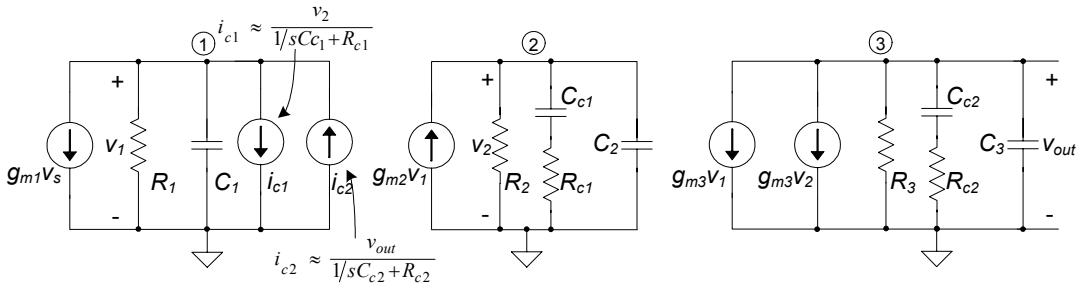

Figure 3-39. Small signal model for the three-stage class AB op-amp seen in Figure 3-37.

Now, applying nodal analysis on the small signal model presented in Figure 3-39, we get the following three equations for each of the nodes.

$$g_{m1}v_s + \frac{v_1}{R_1} + v_1 sC_1 + \frac{v_2}{1/sC_{c1}+R_{c1}} - \frac{v_{out}}{1/sC_{c2}+R_{c2}} = 0 \qquad (3.74)$$

$$-g_{m2}v_1 + \frac{v_2}{R_2} + \frac{v_2}{1/sC_{c1} + R_{c1}} + v_2 sC_2 = 0 \tag{3.75}$$

$$g_{m3}v_1 + g_{m3}v_2 + \frac{v_3}{R_3} + \frac{v_{out}}{1/sC_{c2} + R_{c2}} + v_{out}sC_3 = 0 \tag{3.76}$$

Simultaneously solving Equations 3.26-3.28, we get the following small signal transfer function.

$$\frac{v_{out}}{v_s} = A_v\left(\frac{b_0 + b_1 s + b_2 s^2 + b_3 s^3}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5}\right) \tag{3.77}$$

where the approximate transfer function coefficients, subjected to the simplifying conditions $g_{mk}R_k \gg 1$, $k = 1, 2, 3$; $C_3 \approx C_L$; $C_{c1}, C_{c2}, C_3 \gg C_1, C_2$, are given as

$$A_v = g_{m1}R_1(g_{m2}R_2 + 1)g_{m3}R_3 \tag{3.78}$$

$$b_0 = 1 \tag{3.79}$$

$$b_1 \approx R_{c1}C_{c1} + R_{c2}C_{c2} \tag{3.80}$$

$$b_2 \approx R_{c1}C_{c1}R_{c2}C_{c2} \tag{3.81}$$

$$b_3 = \frac{R_{c1}C_{c1}R_{c2}C_{c2}R_2C_2}{g_{m2}R_2 + 1} \tag{3.82}$$

$$a_0 = 1 \tag{3.83}$$

$$a_1 \approx g_{m2}R_2g_{m3}R_3R_1C_{c2} \tag{3.84}$$

$$a_2 \approx g_{m2}R_2g_{m3}R_3R_1C_{c2}R_{c1}C_{c1} + g_{m2}R_2R_1C_{c1}(R_{c2}C_{c2} + R_3(C_{c2} + C_3)) + g_{m3}R_3R_1C_{c2}(R_{c1}C_{c1} + R_2(C_{c1} + C_2)) \tag{3.85}$$

$$a_3 \approx (g_{m2}R_{c2}C_3 + g_{m3}R_{c1}C_2)R_1R_2R_3C_{c1}C_{c2} \tag{3.86}$$

$$a_4 \approx R_3C_3[R_{c1}C_{c1}\{R_{c2}C_{c2}(R_1C_1 + R_2C_2) + R_1C_1R_2C_2\}] + R_3C_3R_{c2}C_{c2}R_1C_1R_2(C_{c1} + C_2) \tag{3.87}$$

$$a_5 = R_1C_1R_2C_2R_3C_3R_{c1}C_{c1}R_{c2}C_{c2} \tag{3.88}$$

Again, the locations of the zeros are simply evaluated as

$$z_1 = -\frac{1}{R_{c1}C_{c1}}, \text{ and} \tag{3.89}$$

$$z_2 = -\frac{1}{R_{c2}C_{c2}} \tag{3.90}$$

Also, a third parasitic zero exists at the location

$$z_3 = -\frac{g_{m2}}{C_2} \tag{3.91}$$

The location of the dominant pole is given by

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m3}R_3g_{m2}R_2R_1C_{c2}} \tag{3.92}$$

and the unity gain frequency is

$$f_{un} = \frac{|p_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_{c2}} \tag{3.93}$$

Again, the denominator, D(s), of the small signal transfer function can be approximated as

$$D(s) \approx \left(1 + \frac{a_0}{a_1}s\right)\left(1 + \frac{a_2}{a_1}s + \frac{a_3}{a_1}s^2\right)\left(1 + \frac{a_4}{a_3}s + \frac{a_5}{a_3}s^2\right) \tag{3.94}$$

Now, we can either employ pole-zero cancellation or individually locate poles and zeros to design the op-amp.

Design with Pole-Zero Cancellation

The two LHP zeros, z_1 and z_2, can be used to cancel the non dominant poles p_2 and p_3. The pole-zero cancellation results in the following relations

$$R_{c2} \approx \frac{C_{c1}}{C_{c2}^2 g_{m3}}(C_3 + C_{c2}) + \frac{R_1 C_1}{g_{m2} R_2 C_{c2}} \tag{3.95}$$

$$R_{c1} \approx \frac{C_3}{g_{m3} C_{c2}} - \frac{C_2 + C_{c1}}{g_{m2} C_{c1}} \tag{3.96}$$

The Equations 3.95 and 3.96 can be further simplified to eliminate the parasitic terms. This results in R_{c1} and R_{c2} values independent of R_1, C_1 and C_2, as shown below. However, the accuracy of pole-zero cancellation is compromised by making these approximations.

$$R_{c2} \approx \frac{C_{c1}}{C_{c2}^2 g_{m3}}(C_3 + C_{c2}) \tag{3.97}$$

$$R_{c1} \approx \frac{C_3}{g_{m3} C_{c2}} - \frac{1}{g_{m2}} \tag{3.98}$$

The pole-zero cancellation results in the op-amp topology shown in Figure 3-40 and achieved a phase margin close to $90°$. Here C_{c1}=1pF, C_{c2}=2pF, $R_{1c} = 124\Omega$ and $R_{2c} = 1.14K\Omega$. This topology is henceforth referred as Reversed Nested Indirect Compensation (RNIC) in this treatise.

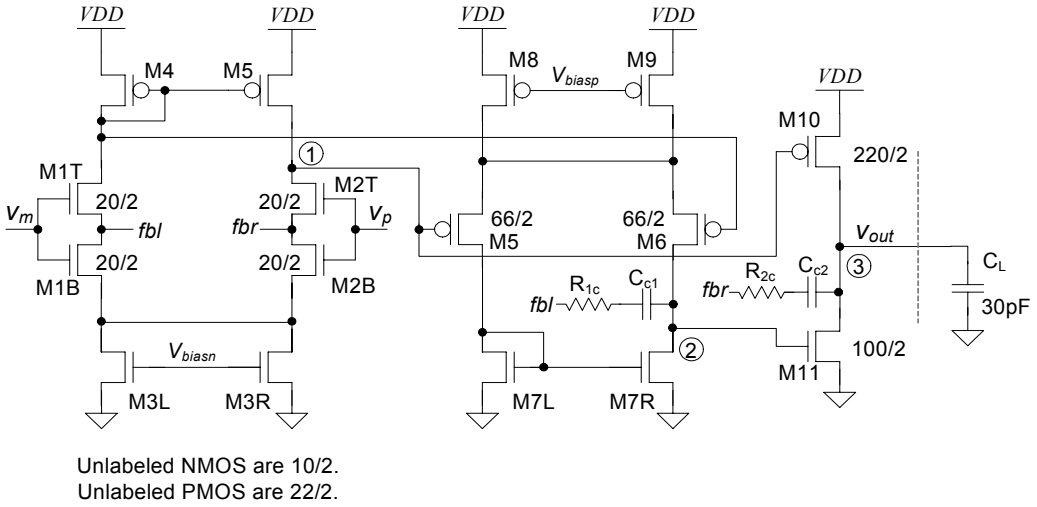

Figure 3-40. Three-stage Class AB op-amp topology employing pole-zero cancellation (RNIC-1).

Again, the pole-zero doublet locations are estimated as

$$p_2 \approx z_1 \approx -\frac{1}{R_{c1}C_{c1}} = -\frac{1}{\frac{C_{c1}C_3}{C_{c2}g_{m3}} - \frac{C_{c1}}{g_{m2}}} \tag{3.99}$$

$$p_3 \approx z_2 \approx -\frac{1}{R_{c2}C_{c2}} = -\frac{g_{m3}C_{c2}}{C_{c1}(C_3 + C_{c2})} \tag{3.100}$$

The parasitic poles p_4 and p_5 are real when the condition $a_4^2 \gg 4a_3a_5$ is satisfied. This loosely translates into the criterion $R_{c1}R_{c2} \gg g_{m2}R_2^3\frac{C_2}{C_1}$. Then

$$p_4 \approx -\frac{a_3}{a_4} \approx -\frac{(g_{m2}R_{c2}C_3 + g_{m3}R_{c1}C_2)}{R_{c1}R_{c2}\left(\frac{C_1}{R_2} + \frac{R_2}{C_1}\right) + \frac{C_1C_2}{C_{c2}C_{c2}} + R_{c2}C_1}, \text{ and} \tag{3.101}$$

$$p_5 \approx -\frac{a_4}{a_5} = -\left[\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + \frac{1}{R_{c2}C_{c2}} + \frac{1}{R_{c1}C_2}\right] \tag{3.102}$$

If the condition $R_{c1}R_{c2} < g_{m2}R_2^3\frac{C_2}{C_1}$ is satisfied, then the conjugate poles are located at

$$\mathrm{Re}(p_{4,5}) \approx -\sqrt{\frac{a_3}{a_5}} \approx -\sqrt{\frac{g_{m2}R_{c2}}{C_1C_2R_{c1}} + \frac{g_{m2}R_{c2}}{C_1C_2R_{c1}}} \tag{3.103}$$

Now, for unconditional stability the pole-zero doublets should be at higher frequency than the unity gain frequency. This leads to the condition that

$$p_2, z_1, p_3, z_2 > \frac{g_{m1}}{C_{c2}} \tag{3.104}$$

which translates into the following lower limit on the capacitor C_{c2}

$$C_{c2} > \frac{g_{m1}C_{c1}}{2g_{m2}}\left[\sqrt{\frac{4g_{m2}^2C_3}{g_{m1}g_{m3}C_{c1}} + 1} + 1\right] \tag{3.105}$$

which can be satisfied with much lower values of C_{c1}. The resulting transfer function after pole-zero cancellation is given as

$$\frac{v_{out}}{v_s} \approx \frac{A_v}{\left(1 - \frac{s}{p1}\right)\left(1 + \frac{a_4}{a_3}s + \frac{a_5}{a_3}s^2\right)} \approx \frac{A_v}{\left(1 - \frac{s}{p1}\right)} \text{ for } f \ll f_T \tag{3.106}$$

Thus, the resulting small signal transfer function looks like a single dominant pole response with almost 90° phase margin, and R-C circuit like settling in time domain.

Figures 3-41 and 3-42 present the numerically simulated frequency response and pole-zero plot for the op-amp seen in Figure 3-40.

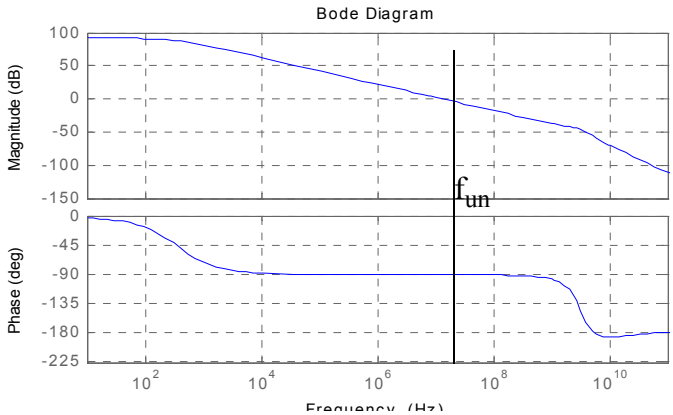

Figure 3-41. Numerically simulated frequency response for the class AB three-stage op-amp using the model shown in Figure 3-39. Here f_{un}=30MHz and PM=90° .

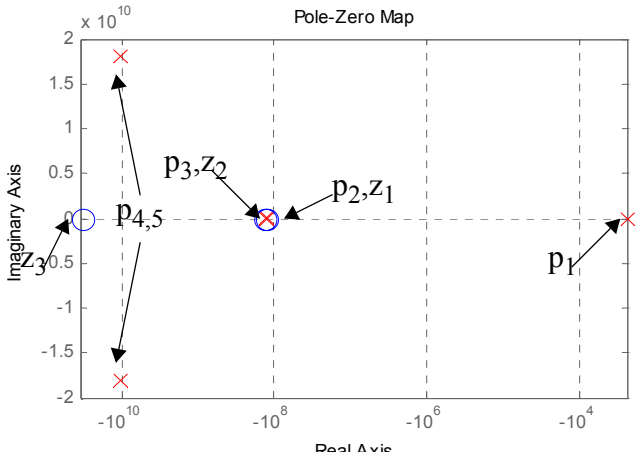

Figure 3-42. pole-zero plot for the class AB three-stage op-amp showing pole-zero cancellation of second and third poles.

Figures 3-43 shows the SPICE simulated frequency response for the op-amp shown in Figure 3-40. The SPICE simulated results are close to the numerically simulated values.

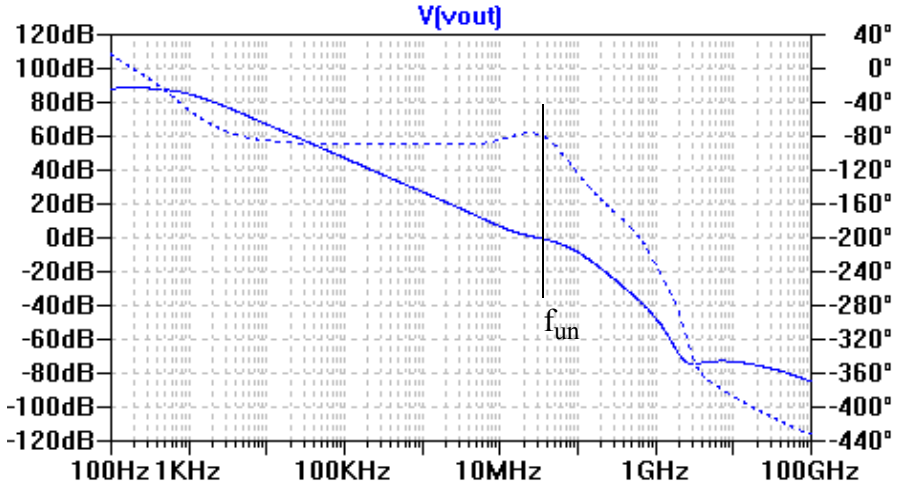

Figure 3-43. SPICE simulated frequency response of the class AB three-stage op-amp. Here f_{un}=30MHz and PM is close to 90° .

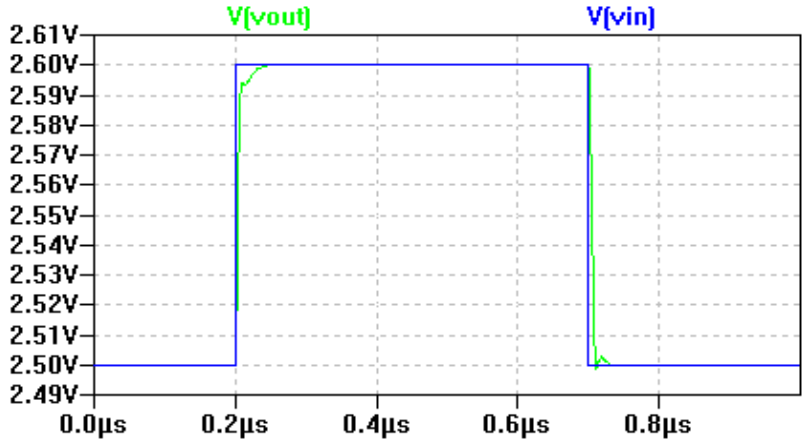

Figure 3-44. Small step transient response for the Class AB three-stage op-amp. The settling time here is close to 70ns.

Design without pole-zero cancellation

A three stage class AB op-amp can also be designed without employing pole-zero cancellation. The design equations can be derived as shown earlier. Figures 3-46 and 3-47

show the frequency and small step transient responses respectively for a class AB three stage op-amp designed using the topology seen in Figure 3-40 without the resistors R_{1c} and R_{2c}, and with the capacitors C_{c1}=C_{c2}=1.5pF (see Figure 3-45).

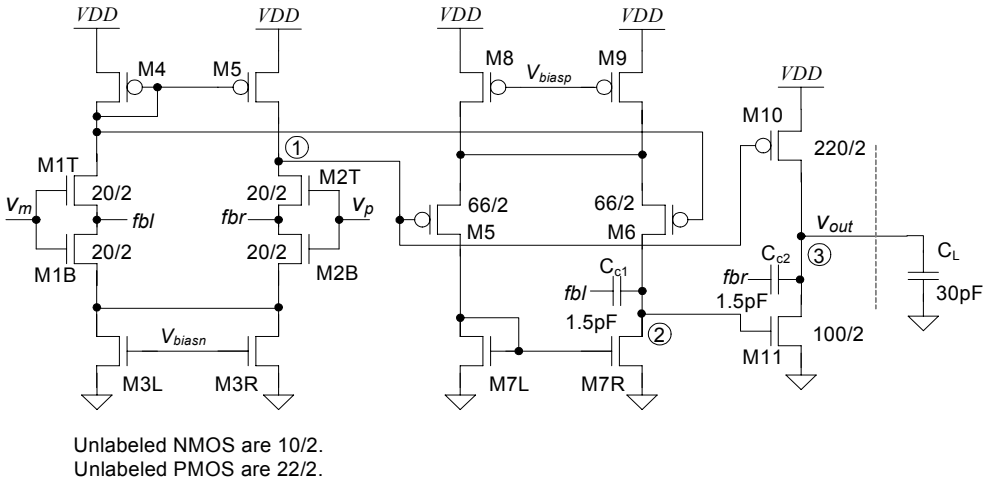

Figure 3-45. An indirect compensated, three-stage, class AB op-amp without the pole-zero cancellation.

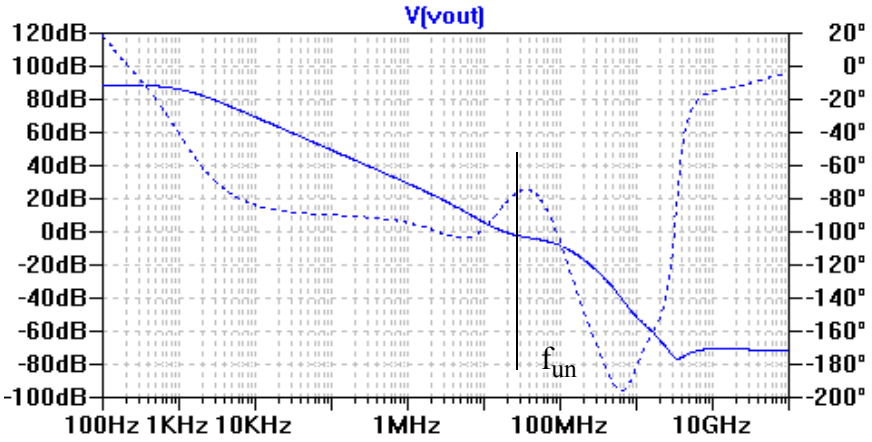

Figure 3-46. SPICE simulated frequency response of the three-stage Class AB designed without using pole -zero cancellation. ere f_{un}=25MHz and PM is close to 75°.

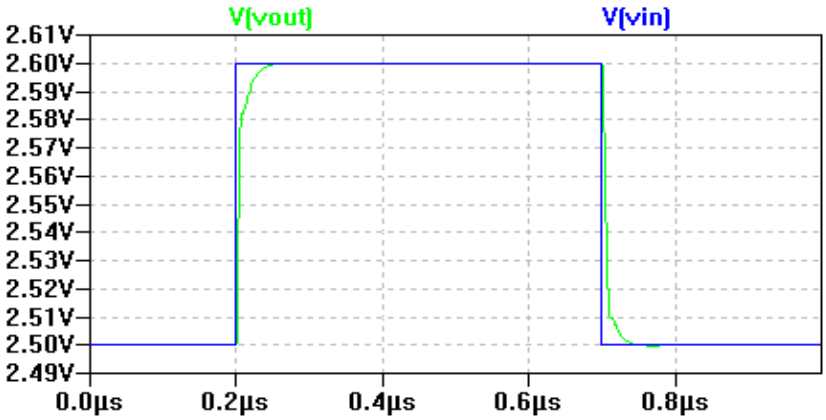

Figure 3-47. Small step transient response of the three-stage Class AB designed for pole - zero cancellation. Here, the settling time, t_s = 70ns.

The class AB three-stage op-amp topology seen in Figure 3-40, is a very low power topology but has two gain paths causing crossover distortion. For applications which require higher THD, a single gain path version of the op-amp can be realized using a floating current buffer as shown in Figure 3-48. The references V_{pcas} and V_{ncas}, shown in Figure 3-49, are used to bias the floating current source and implement the following equations

$$V_{ncas} = 2V_{GS} \tag{3.107}$$

$$V_{pcas} = V_{DD} - 2V_{SG} \tag{3.108}$$

Detailed description of operation and analysis of the floating current source is provided in [1].

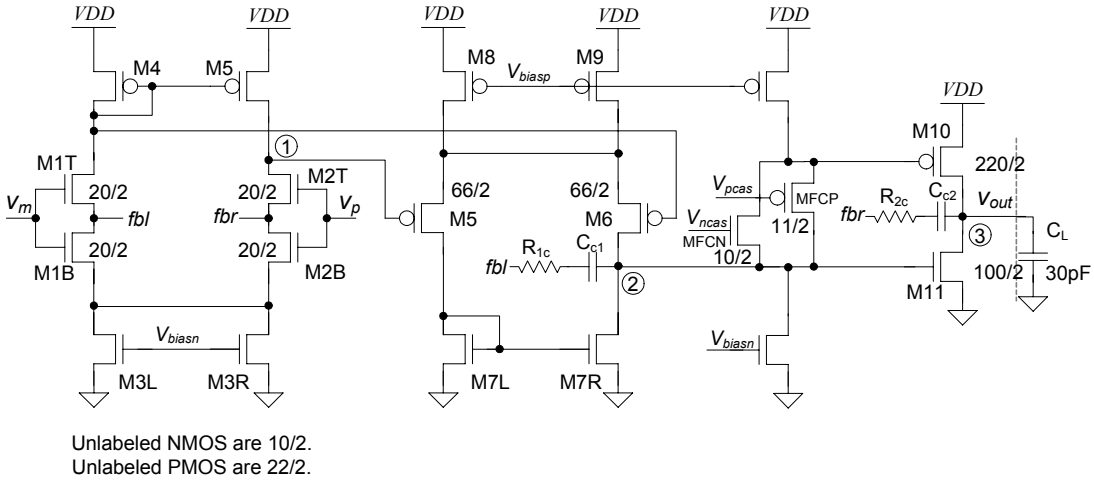

Figure 3-48. A Single gain path, three-stage class AB op-amp using floating current source buffer.

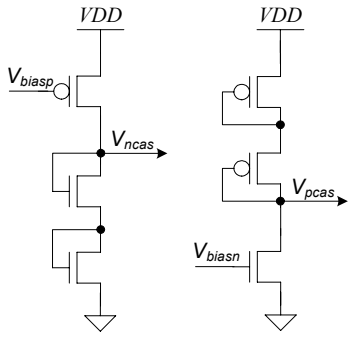

Figure 3-49. Circuits to generate Vpcas and Vncas references used in Figure 3-48.

Performance Comparison

The performance of the proposed three-stage op-amp topologies is compared with the ones reported in the literature. A set of figure of merits (FoMs) have been defined in [29] to compare various multistage topologies. We have adopted the same metrics as in [29] to compare the op-amp performances. The FoMs are defined as

$$FoM_S = \frac{f_{un} \cdot C_L}{V_{DD} \cdot I_{DD}} \tag{3.109}$$

$$FoM_L = \frac{SR \cdot C_L}{V_{DD} \cdot I_{DD}} \tag{3.110}$$

where fun is the gain-bandwidth, and SR is the average slew-rate of the op-amps[29]. The worst case slew rate (SR) limitation for the RNIC topologies is given as

$$SR = \min\left(\frac{I_{ss1}}{C_{C1}}, \frac{I_{ss1}}{C_{C2}}\right) \tag{3.111}$$

where I_{ss1} is the tail bias current in the first stage diff-amp, which is double the bias current in the first stage.

FoM_S is used to compare the small signal performances of the op-amps while FoM_L acts as a comparison metric for the large signal performance. Another set of FoMs are used in order to desensitize the performance comparison to the supply voltage value. These FoM's, which use the total quiescent DC current pulled from the supply (I_{DD}) as an independent variable instead of power, are given as [29]:

$$IFoM_S = \frac{f_{un} \cdot C_L}{I_{DD}} \tag{3.112}$$

$$IFoM_L = \frac{SR \cdot C_L}{I_{DD}} \tag{3.113}$$

These four FoM's, given by Equations 3.109-3.113, serve as a fair set of performance metrics for the comparison of the op-amps under consideration. Since in [29], a large

load capacitance is used to enhance the reported FoM values, a set of indirect-compensated op-amps have been designed to drive the same 500pF off-chip load, in order to facilitate a reasonable comparison. Figure 3-50 shows a low-power, indirect compensated, three-stage op-amp designed to drive 500pF load. This topology is henceforth referred to as Reversed nested Indirect Compensation (RNIC-2) op-amp in this thesis. Also Figure 3-51 shows the schematic of a high-performance variant of RNIC driving 500pF load and has faster set-tling. Again this high-performance topology is named as RNIC-3.

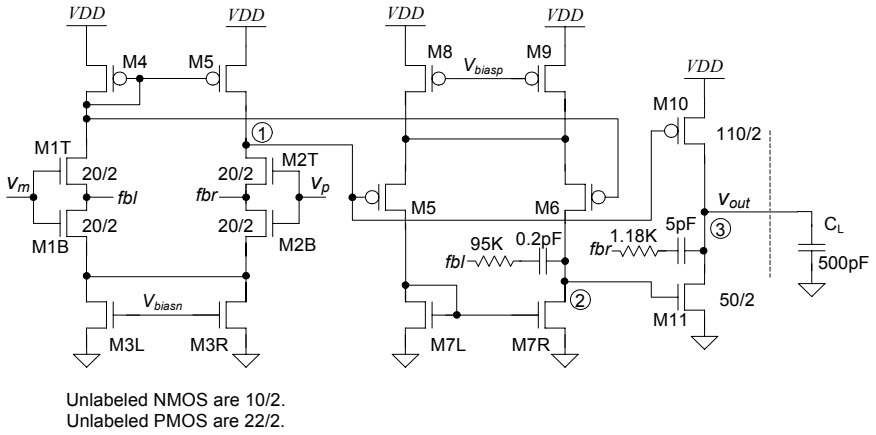

Figure 3-50. A low-power, indirect compensated, three-stage op-amp to drive 500pF off-chip load (RNIC-2).

Figure 3.48 shows a single gain path implementation of the low power, class AB, three stage op-amp seen in Figure 3.46. This topology achieves better THD performance compared to the dual gain path one.

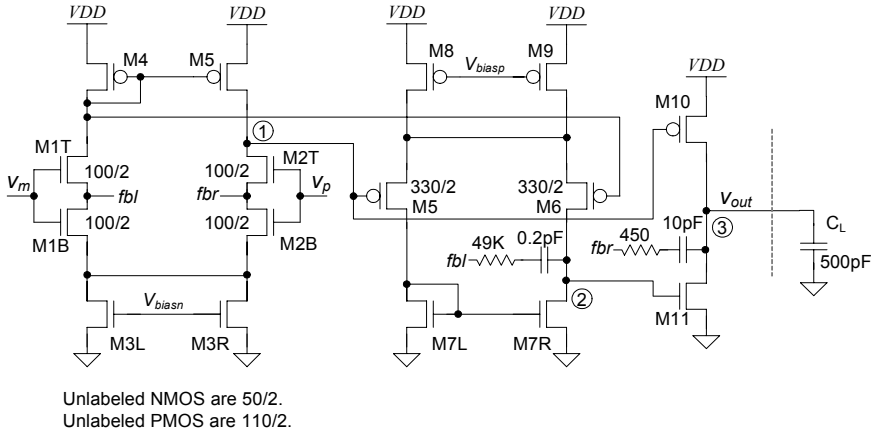

Figure 3-51. A high-performance, indirect compensated, three-stage op-amp to drive 500pF off-chip load (RNIC-3).

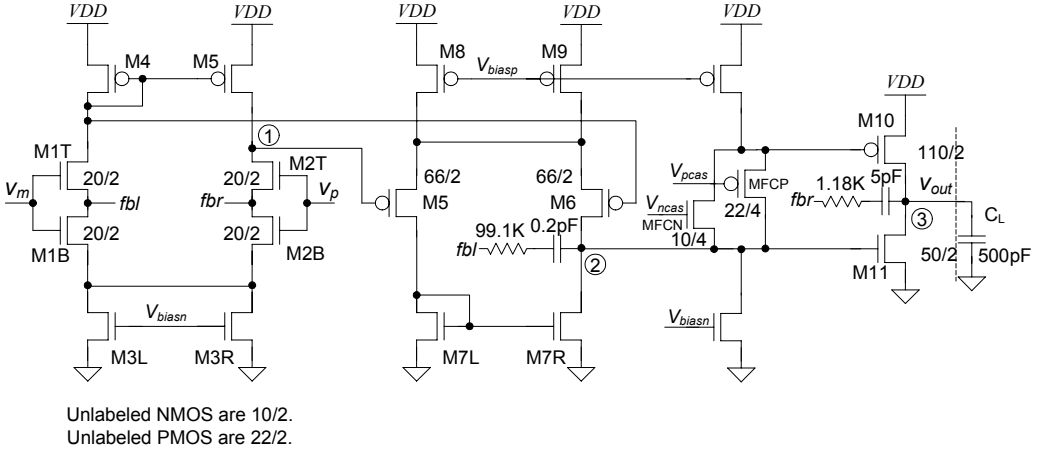

Figure 3-52. A low power, indirect compensated, three-stage op-amp with single gain path, to drive 500pF off-chip load (RNIC-4).

Table 3-1 presents a comprehensive comparison of the multistage op-amp topologies reported in literature using the FoM's described earlier. The indirect compensated, three-stage op-amps (RNIC) designed in this thesis perform well up to a supply voltage as

low as 1.25V. The performance metrics of these op-amps operating at 2V supply are also shown in the comparison Table 3-1. However, there is a proportional reduction in gain-bandwidth of the op-amps operating at 2V supply, due to the V_{DS} voltage dependence of the device transconductances given as $g_m = \beta(V_{GS} - V_{THN})(1 + \lambda V_{DS})$. A decrease in VDD results in reduction in V_{DS}, resulting in reduced g_m's, and hence relatively slower amplifiers. The op-amps operating at 2V supply are referred with a suffix 'A' in Table 3-1.

As it can be seen Table 3-1, the indirect-compensated three-stage op-amps outperform all other op-amps reported in literature by over 200%. These op-amps exhibit comparable performance even at a lower supply voltage of 2V. The performance comparison tabulated in Table 3-1 is pictorially illustrated in Figure 3-53.

Table 3-1. Comparison of Three-Stage Op-amp Topologies [29]

Topology	C_L (pF)	V_{DD} (V)	I_{DD} (mA)	Power (mW)	f_{un} (MHz)	Avg. SR (V/µs)	C_{c1}, C_{c2} (pF)	FoM_S (MHz.pF/mW)	FoM_L (V/µs.pF/mW)	$IFoM_S$ (MHz.pF/mA)	$IFoM_L$ (V/µs.pF/mA)
MNMC [17]	100	8	9.5	76	100	35	--	132	46	1053	368
NGCC [14]	20	2	0.34	0.68	0.61	2.5	--	18	74	36	147
NMCFNR [20]	100	2	0.2	0.4	1.8	0.79	30, 5.3	450	198	900	395
DFCFC [21]	1000	2	0.2	0.4	1	0.36	55, 3	2500	900	5000	1800
AFFC [23]	100	1.5	0.17	0.255	5.5	0.36	5.4, 4	2157	141	3235	212
ACBCF [24]	500	2	0.162	0.324	1.9	1	10, 3	2932	1543	5864	3086
TCFC [25]	150	1.5	0.03	0.045	2.85	1.035	1.1, 0.92	9500	3450	14250	5175
DPZCF [26]	500	1.5	0.15	0.225	1.4	2	30, 20	3111	4444	4667	6667
RNMC VB NR [27]	15	3	0.48	1.44	19.46	13.8	3, 0.7	203	144	608	431
SMFFC [28]	120	2	0.21	0.42	9	3.4	4	2571	971	5143	1943
RNMCFBNR [29]	500	3	0.085	0.255	2.4	1.8	11.5, 0.35	4706	3529	14118	10588
RAFFC [29]	500	3	0.105	0.315	2.4	1.95	11.5, 0.35	3810	3095	11429	9286
RAFFC Low-Power [29]	500	3	0.035	0.105	1.1	1.29	11.5, 0.35	5238	6143	15714	18429
RNIC-1 (This work)	**30**	**3**	**0.28**	**0.84**	**30**	**20**	**1, 2**	**1071**	**714**	**3214**	**2143**
RNIC-2 (This work)	**500**	**3**	**0.18**	**0.54**	**12**	**8**	**5, 0.2**	**11111**	**7407**	**33333**	**22222**
RNIC-3 (This work)	**500**	**3**	**0.5**	**1.5**	**35**	**20**	**10, 0.2**	**11667**	**6667**	**35000**	**20000**
RNIC-1A (This work)	**30**	**2**	**0.28**	**0.56**	**15**	**20**	**1, 2**	**804**	**1071**	**1607**	**2143**
RNIC-2A (This work)	**500**	**2**	**0.18**	**0.36**	**6**	**20**	**5, 0.2**	**8333**	**27778**	**16667**	**55556**
RNIC-3A (This work)	**500**	**2**	**0.5**	**1**	**17**	**20**	**10, 0.2**	**8500**	**10000**	**17000**	**20000**

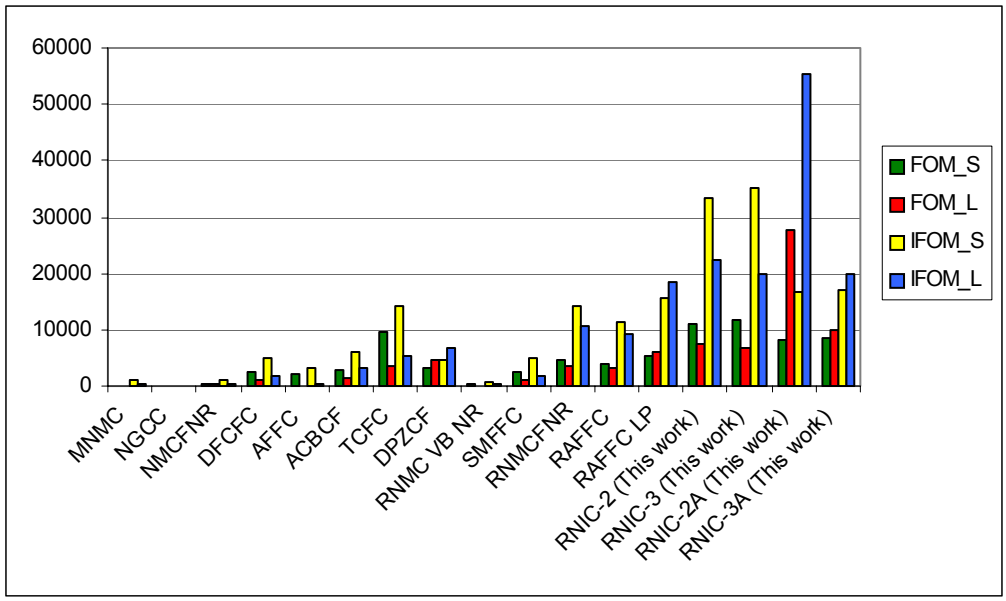

Figure 3-53. Bar chart showing the performance comparison of the various multistage op-amps tabulated in Table 3-1. It can be observed that the topologies proposed in this thesis exhibit significantly higher performance indexes.

However, one can observe that the proposed op-amps have been designed with higher power consumption when compared to the latest reported op-amp topologies in [29]. This has been intentionally done in order to obtain fast settling times which are comparable to the corresponding two-stage op-amps. A comparison of the settling times for a step input of 1% of VDD is listed in Table 3-2.

Table 3-3 shows the comparison between the RNIC-1 op-amp with the corresponding two-stage op-amps, seen in chapter 2, to drive a 30pF load. Here, we observe that by employing the RNIC three-stage topology, we can obtain an increase in the open-loop DC gain by 23 to 29 dB for the same unity-gain frequency (i.e. the same speed) at a lower

supply voltage, just by consuming 20% more power and by occupying almost the same layout area. The layout area remains almost equal as for the two-stage op-amp as the bias circuit is simplified and we no longer employ cascoding.

Table 3-2. Comparison of the proposed op-amps with the latest reported topologies.

Op-amp Topology	**VDD (V)**	**C_L (pF)**	**Power (mW)**	**f_{un} (MHz)**	**Avg. SR (V/μs)**	**PM**	**t_s (ns)**	**Area (mm^2)**
RNMCFBNR [29]	3	500	0.255	2.4	1.8	58◦	810	0.025
RAFFC [29]	3	500	0.315	2.4	1.95	58◦	560	0.025
RAFFC Low-Power [29]	3	500	0.105	1.1	1.29	56◦	1000	0.024
RNIC-1 (This work)	**3**	**30**	**0.84**	**30**	**20**	**89◦**	**70**	**0.018**
RNIC-2 (This work)	**3**	**500**	**0.54**	**12**	**8**	**88◦**	**250**	**0.022**
RNIC-3 (This work)	**3**	**500**	**1.5**	**35**	**20**	**72◦**	**100**	**0.031**
RNIC-1A (This work)	**2**	**30**	**0.56**	**15**	**20**	**89◦**	**90**	**0.018**
RNIC-2A (This work)	**2**	**500**	**0.36**	**6**	**20**	**88◦**	**350**	**0.022**
RNIC-3A (This work)	**2**	**500**	**1**	**17**	**20**	**72◦**	**150**	**0.031**

Table 3-3. Comparison between the proposed two-stage and three-stage topologies for C_L=30pF.

Op-amp Topology	**VDD (V)**	**C_L (pF)**	**Gain (dB)**	**Power (mW)**	**f_{un} (MHz)**	**PM**	**t_s (ns)**	**Area (mm^2)**
Indirect SLCL (two-stage)	5	30	66	0.7	20	58◦	60	0.015
Indirect SLDP (two-stage)	5	30	60	0.7	35	56◦	75	0.015
RNIC-1 (three-stage)	3	30	89	0.84	30	89◦	70	0.018
RNIC-1A (three-stage)	2	30	87	0.56	15	89◦	90	0.018

In this section we have demonstrated a methodology for achieving higher performance and simpler three-stage op-amp topologies by employing indirect compensation. However, yet higher performance can be achieved by optimizing the g_m's and hence the bias currents in each of the gain stages for a given load. A flowchart outlining the design procedure for the pole-zero cancelled RNIC op-amps is shown in Figure 3-54.

The design equations for the pole-zero cancelled three-stage op-amps developed in this chapter are summarized in Table 3-4.

Table 3-4. Design equations for the pole-zero cancelled three-stage op-amps.

<table>
<tr><td colspan="2">The indirect compensation resistance values are calculated as:</td></tr>
<tr><td>$R_{1c} = \frac{C_L}{g_{m3}C_{c2}} - R_{c0}$ for the Class A and single-gain-path Class AB Op-amps.</td><td>$R_{1c} = \frac{C_L}{g_{m3}C_{c2}} - \frac{1}{g_{m2}} - R_{c0}$ for the dual-gain-path Class AB Op-amp.</td></tr>
<tr><td colspan="2">$R_{2c} = \frac{C_{c1}}{C_{c2}^2 g_{m3}}(C_L + C_{c2}) - R_{c0}$, where $R_{c0} \approx \frac{1}{\sqrt{2}g_{m1}}$ is the impedance attached to the internal low impedance node A.</td></tr>
<tr><td colspan="2">The pole-zero locations are given as:</td></tr>
<tr><td>$f_{p_1} = -\frac{1}{g_{m3}R_3 g_{m2}R_2 R_1 C_{c2}}$
$f_{p_3} = f_{z_2} = \frac{g_{m3}C_{c2}}{2\pi(C_L + C_{c2})C_{c1}} \approx f_{p_2}$
$f_{un} = \frac{\lvert p_1 \rvert A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_{c2}}$</td><td>$f_{p_2} = f_{z_1} = \frac{g_{m3}C_{c2}}{2\pi C_L C_{c1}}$
$f_{p_{4,5}} = \frac{g_{m3}C_{c2}}{2\pi C_3}\sqrt{\frac{g_{m2}R_2 C_{c2}}{C_1 C_2 C_{c1}}}$</td></tr>
<tr><td colspan="2">The phase margin of the op-amp is given by:</td></tr>
<tr><td>$\Phi = 90° - \tan^{-1}\left(\frac{\frac{2\pi f_{un}}{f_{p_{4,5}}Q_{4,5}}}{1-\left(\frac{2\pi f_{un}}{f_{p_{4,5}}}\right)^2}\right)$</td><td>$Q_{4,5} = \sqrt{\frac{g_{m2}R_2}{R_{c1}R_{c2}}}\left(\frac{1}{\frac{1}{R_1}\sqrt{\frac{C_1}{C_2}} + \frac{1}{R_2}\sqrt{\frac{C_2}{C_1}}}\right)$</td></tr>
<tr><td>Design constraints:
$f_{p_2}, f_{p_3} > f_{un}$ and $R_{1c}, R_{2c} \geq 0$.</td><td>Design bound:
$f_{un} < \frac{1}{2\pi}\sqrt{\frac{g_{m3}}{g_{m1}C_L C_{c1}}}$</td></tr>
</table>

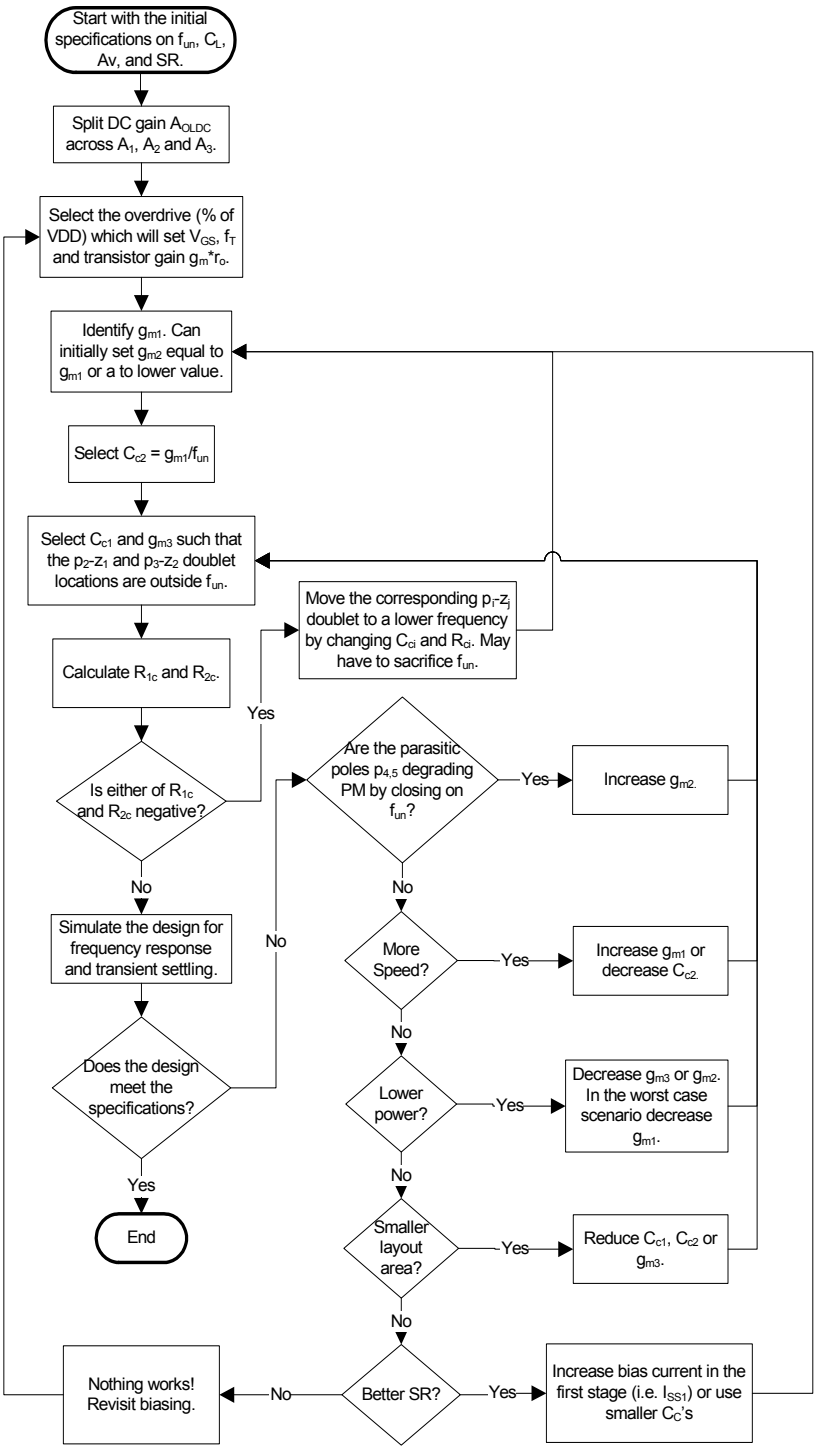

Figure 3-54. Flowchart showing the design procedure for a pole-zero cancelled, indirect compensated three-stage op-amp.

N-Stage Indirect Feedback Compensated Op-Amp Theory

The three-stage indirect compensation theory for op-amps, developed in earlier in this chapter, can be extended to encompass a generalized N-stage op-amp. 3-55 shows the block diagram for a N-stage indirect compensated op-amp. This op-amp is a cascade of N amplifying stages, where the first (N-1) stages have to be diff-amps for precise biasing of each gain stage. The N-stage op-amp is compensated using (N-1) compensation capacitors, denoted as C_{c_k}, for k=1 to (N-1). The compensation currents are indirectly fed-back to node-1 in such as way, that we have all negative feedback loops. The resistances associated with each indirect feedback compensation paths are denoted as R_{c_k}, for k=1 to (N-1).

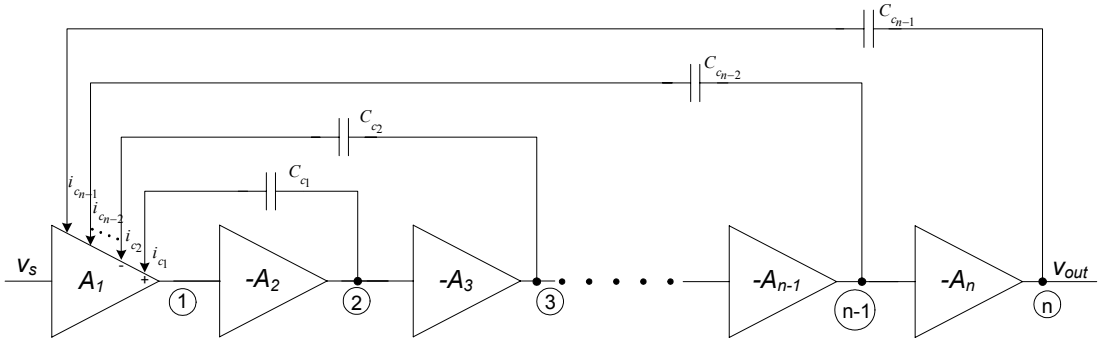

Figure 3-55. Block diagram for a generalized N-stage indirect compensated op-amp

A simplified model for N-stage (cascaded) op-amp employing indirect feedback compensation is shown in Figure 3-56.

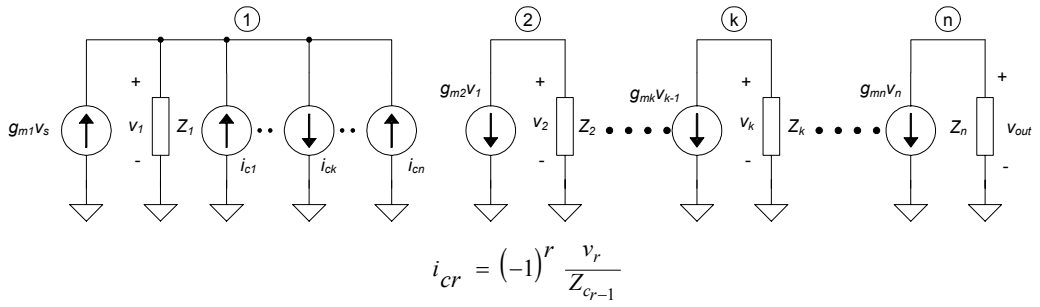

Figure 3-56. Small signal model for an N-stage indirect compensated op-amp.

The nodal analysis equations for the model shown in Figure 3-56 are given as

$$g_{m1}v_s + \frac{v_1}{Z_1} + \sum_{r=2}^{n} (-1)^r \frac{v_r}{Z_{c_{r-1}}} = 0 \tag{3.114}$$

$$g_{mk}v_{k-1} + \frac{v_k}{Z_k} = 0, \qquad k=2,3,.....,(n-1). \tag{3.115}$$

$$g_{mn}v_{n-1} + \frac{v_n}{Z_n} = 0 \tag{3.116}$$

where $Z_k = R_k \| \frac{1}{sC_k}$ and $Z_{ck} = R_{c_k} + \frac{1}{sC_{c_k}}$, for k=2,....,N.

The set of linear equations can be represented by the following matrix equation

$$\begin{bmatrix} \frac{1}{Z_1} & -\frac{1}{Z_{c_1}} & \frac{1}{Z_{c_2}} & \cdots & \cdots & \frac{(-1)^{k-1}}{Z_{c_{k-1}}} & \cdots & \frac{(-1)^{n-2}}{Z_{c_{n-2}}} & \frac{(-1)^{n-1}}{Z_{c_{n-1}}} \\ g_{m2} & \frac{1}{Z_2} & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & g_{m3} & \frac{1}{Z_3} & \cdots & 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & \cdots \\ 0 & 0 & 0 & \cdots & g_{m(k-1)} & \frac{1}{Z_k} & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & \cdots \\ 0 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & \frac{1}{Z_{n-1}} & 0 \\ 0 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & g_{mn} & \frac{1}{Z_n} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ \cdots \\ \cdots \\ v_k \\ \cdots \\ v_{n-1} \\ v_n \end{bmatrix} = \begin{bmatrix} g_{m1} v_s \\ 0 \\ 0 \\ \cdots \\ \cdots \\ \cdots \\ \cdots \\ 0 \\ 0 \end{bmatrix} \tag{3.117}$$

Now, the output voltage, v_{out} (=v_n), can be evaluated using Cramer's rule as shown below.

$$v_{out} = v_n = \frac{\Delta_n}{\Delta} \tag{3.118}$$

where the determinants Δ and Δ_n are given as

$$\Delta = \begin{vmatrix} \frac{1}{Z_1} & -\frac{1}{Z_{c_1}} & \frac{1}{Z_{c_2}} & \cdots & \cdots & \frac{(-1)^{k-1}}{Z_{c_{k-1}}} & \cdots & \frac{(-1)^{n-2}}{Z_{c_{n-2}}} & \frac{(-1)^{n-1}}{Z_{c_{n-1}}} \\ g_{m2} & \frac{1}{Z_2} & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & g_{m3} & \frac{1}{Z_3} & \cdots & 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & \cdots \\ 0 & 0 & 0 & \cdots & g_{m(k-1)} & \frac{1}{Z_k} & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & \cdots \\ 0 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & \frac{1}{Z_{n-1}} & 0 \\ 0 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & g_{mn} & \frac{1}{Z_n} \end{vmatrix} \tag{3.119}$$

and

$$\Delta_n = \begin{vmatrix} \frac{1}{Z_1} & -\frac{1}{Z_{c_1}} & \frac{1}{Z_{c_2}} & \cdots & \cdots & \frac{(-1)^{k-1}}{Z_{c_{k-1}}} & \cdots & \frac{(-1)^{n-2}}{Z_{c_{n-2}}} & g_{m1}v_s \\ g_{m2} & \frac{1}{Z_2} & 0 & \cdots & 0 & 0 & \cdots & 0 & 0 \\ 0 & g_{m3} & \frac{1}{Z_3} & \cdots & 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & \cdots \\ 0 & 0 & 0 & \cdots & g_{m(k-1)} & \frac{1}{Z_k} & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & 0 & \cdots \\ 0 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & \frac{1}{Z_{n-1}} & 0 \\ 0 & 0 & 0 & \cdots & \cdots & \cdots & \cdots & g_{mn} & 0 \end{vmatrix} \tag{3.120}$$

Now we have,

$$\Delta = \frac{1}{Z_1}\begin{vmatrix} \frac{1}{Z_2} & 0 & \cdots & 0 & 0 \\ g_{m3} & \frac{1}{Z_3} & \cdots & 0 & 0 \\ 0 & g_{m4} & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & g_{mn} & \frac{1}{Z_n} \end{vmatrix} + \frac{1}{Z_{c_1}}\begin{vmatrix} g_{m2} & 0 & \cdots & 0 & 0 \\ 0 & \frac{1}{Z_3} & \cdots & 0 & 0 \\ 0 & g_{m4} & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & g_{mn} & \frac{1}{Z_n} \end{vmatrix} + \frac{1}{Z_{c_2}}\begin{vmatrix} g_{m2} & \frac{1}{Z_2} & \cdots & 0 & 0 \\ 0 & g_{m3} & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & g_{mn} & \frac{1}{Z_n} \end{vmatrix} \tag{3.121}$$

$$+ \cdots + \frac{1}{Z_{c_{n-1}}}\begin{vmatrix} g_{m2} & 0 & \cdots & 0 & 0 \\ 0 & g_{m3} & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 0 & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & \cdots & 0 & g_{mn} \end{vmatrix}$$

or

$$\Delta = \prod_{i=1}^{n}\frac{1}{Z_i} + \frac{g_{m2}}{Z_{c_1}}\prod_{r=3}^{n}\frac{1}{Z_r} + \frac{g_{m2}g_{m3}}{Z_{c_2}}\prod_{r=4}^{n}\frac{1}{Z_r} + \cdots + \frac{1}{Z_{c_{n-1}}}\prod_{r=2}^{n} g_{mr} \tag{3.122}$$

$$\Delta = \prod_{i=1}^{n}\frac{1}{Z_i} + \sum_{r=2}^{n}\left(\frac{1}{Z_{c_{r-1}}}\prod_{p=2}^{r} g_{mp}\prod_{q=r+1}^{n}\frac{1}{Z_q}\right) \tag{3.123}$$

Also,

$$\Delta_n = g_{m1}v_s \begin{vmatrix} g_{m2} & \frac{1}{Z_2} & 0 & \cdots & 0 \\ 0 & g_{m3} & \frac{1}{Z_3} & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & \cdots & g_{mn} \end{vmatrix} = v_s \prod_{r=1}^{n} g_{mr} \tag{3.124}$$

Using Equations 3.121 and 3.124, we obtain the small signal transfer function for the N-stage op-amp, which is given as

$$\frac{v_{out}}{v_s} = \frac{\prod_{r=1}^{n} g_{mr}}{\prod_{i=1}^{n} \frac{1}{Z_i} + \sum_{r=2}^{n} \left(\frac{1}{Z_{c_{r-1}}} \prod_{p=2}^{r} g_{mp} \prod_{q=r+1}^{n} \frac{1}{Z_q} \right)} \tag{3.125}$$

For N=2, the Equation 3.125 is reduced to Equation 2.39 which is the two-stage indirect compensated op-amp case. Also for N=3, Equation 3.125 transforms into Equation 3.29 which corresponds to the three-stage indirect compensated op-amp.

In an attempt to further simplify Equation 3.125, we look at the denominator D(s)

$$D(s) = \prod_{i=1}^{n} \frac{(1+s\tau_i)}{R_i} + \left(\prod_{k=1}^{n} R_k \right) \sum_{r=2}^{n} \frac{sC_{c_{r-1}} \prod_{p=2}^{r} g_{mp} \prod_{q=r+1}^{n} (1+s\tau_q) \prod_{u=1}^{r} R_u}{(1+s\tau_{c_{r-1}})} \tag{3.126}$$

or

$$D(s) = \frac{\prod_{i=1}^{n}(1+s\tau_i)\prod_{j=1}^{n-1}(1+s\tau_{c_{j-1}}) + \left(\prod_{k=1}^{n}R_k\right)^2 \sum_{r=2}^{n}\left(sC_{c_{r-1}}\prod_{p=2}^{r}g_{mp}\prod_{q=r+1}^{n}(1+s\tau_q)\prod_{u=1}^{r}R_u\prod_{j=1,j\neq r-1}^{n-1}(1+s\tau_{c_{j-1}})\right)}{\prod_{k=1}^{n}R_k\prod_{j=1}^{n-1}(1+s\tau_{c_{j-1}})} \quad (3.127)$$

where the time constants in the Equation 3.127 are given as $\tau_k = R_kC_k$ and $\tau_{ck} = R_{c_k}C_{c_k}$.

Now, the small signal transfer function can be rewritten as

$$\frac{v_{out}}{v_s} = \frac{\left(\prod_{k=1}^{n}g_{mk}R_k\right)\prod_{j=1}^{n-1}(1+s\tau_{c_{j-1}})}{\prod_{i=1}^{n}(1+s\tau_i)\prod_{j=1}^{n-1}(1+s\tau_{c_{j-1}}) + \left(\prod_{k=1}^{n}R_k\right)^2 \sum_{r=2}^{n}\left(\frac{sC_{c_{r-1}}}{g_{m1}}\prod_{p=1}^{r}g_{mp}R_p\prod_{q=r+1}^{n}(1+s\tau_q)\prod_{\substack{j=1\\ j\neq r-1}}^{n-1}(1+s\tau_{c_{j-1}})\right)} \quad (3.128)$$

We can easily discern that the open loop dc gain is equal to $A_v = \prod_{k=1}^{n}g_{mk}R_k$, as expected.

The N-stage op-amp has (N-1) LHP zeros, whose location can easily be observed to be equal to

$$z_k = -\frac{1}{\tau_{c_k}} = -\frac{1}{R_{c_k}C_{c_k}}, \quad k=1,..,n-1 \quad (3.129)$$

The dominant pole location is estimated as

$$p_1 \approx -\frac{1}{\left(\prod_{k=2}^{n}g_{mk}R_k\right)R_1C_{c_{n-1}}} \quad (3.130)$$

Thus the unity gain frequency is given by

$$f_{un} \approx \left| \frac{A_v p_1}{2\pi} \right| = \frac{g_{m1}}{2\pi C_{c_{n-1}}} \tag{3.131}$$

As it can be observed, it is unwieldy to obtain closed form formulae for the locations of non-dominant poles for the generalized case of N stages. However, the denominator of Equation 3.128 can be simplified for a given value of N, and the non-dominant pole locations can be obtained and also pole-zero cancellation can be achieved using the methodology presented in this chapter.

Summary

We have proposed indirect feedback compensation techniques for design of three-stage, low-power, low-voltage and high-speed op-amps. A systematic method of analysis of indirect compensated, three-stage op-amps has been developed which can be applied to the various topologies employing indirect compensation. A pole-zero cancellation method is proposed for design of three-stage op-amps, which leads to substantial improvement in performance over contemporary design techniques. The pole-zero cancelled, indirect compensated op-amps are fairly robust to process and device variations and can be unhesitatingly be applied in design of integrated systems. Indirect feedback compensation alleviates the compulsion on using a non-inverting topology in reverse nested op-amp topologies. Also since the proposed topologies do not require many voltage references for biasing, lot considerable amount of static power is saved by avoiding complex biasing circuits.

Low power Class AB op-amps can be designed using dual-gain path topologies. However a single gain path implementation, employing a floating current source output-buffer results in an op-amp with better THD performance. The novel Reversed Nested Indirect compensated (RNIC) op-amp topology designed with AMI's 0.5μm CMOS process, proposed in this chapter, drives a 500pF load with a unity gain bandwidth of 35MHz, consumes only 1.5mW power at 3V supply, with 70ns transient settling and 89dB gain. This is an improvement by more than over 200% upon the state-of-the-art reported in [29]. Also the proposed three-stage topology leads to around 26dB higher gain with almost the same unity-gain frequency by consuming only 20% more power while operating at 40% of the supply voltage, and occupying the same layout area as the corresponding two-stage op-amp.

The three-stage indirect compensation analysis has been successfully extended for a generic N-stage op-amp. The proposed N-stage indirect compensation theory can be used for design of op-amps with four or more gain stages.

FULLY DIFFERENTIAL MULTI-STAGE OP-AMP DESIGN USING INDIRECT FEEDBACK COMPENSATION

FULLY-DIFFERENTIAL analog circuits have been exhaustively used in analog signal processing, as they reduce the non-linearities arising due to imperfections in the switches [1]. Fully-differential circuits also provide a larger (almost double) output voltage swing and cancel the common mode noise and even order non-linearities [6]. This chapters presents the design of indirect-compensated fully differential multi-stage op-amps, which are the engines of fully differential analog signal processing circuits.

A fully-differential op-amp requires two symmetrical differential gain paths for the positive and negative outputs and an additional common-mode feedback (CMFB) loop to control the output common-mode level [1]. The common-mode feedback can either be implemented as continuous time or using switched capacitors. However the switched capacitor design will become difficult in sub-100nm processes, due to small overlap of low PMOS and NMOS switch resistance regions [33]. On other hand, low power fully differential op-amp realizations can be achieved by using continuous time CMFB approach. Thus only continuous-time CMFB topologies have been considered in this chapter.

Figure 4-1 shows a high-level block diagram of a fully-differential amplifier. Here, the CMFB block implements the common-mode feedback by sensing the average of the op-amp outputs and comparing their average, $\frac{(v_{op} + v_{om})}{2}$, with the common-mode reference (V_{CM}). The output, V_{CMFB}, of the CMFB circuit controls the current(s) in the differential path to set the desired output common-mode level.

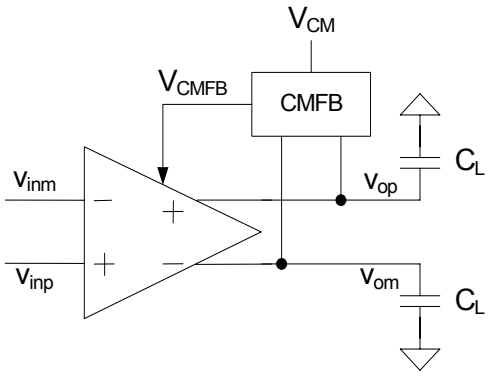

Figure 4-1. A high-level block diagram of a fully-differential op-amp with common-mode feedback [1].

Two-Stage Fully Differential Op-Amp Design

The common-mode feedback can be implemented in fully-differential amplifiers using numerous techniques which are detailed for two-stage op-amp designs in [1] and [6]. Figure 4-2 shows an example design of the CMFB amplifier using a three input diff-amp and Figure 4-3 illustrates the use of CMFB amplifier to set the common-mode level of the output. When the average of the differential outputs (i.e. the output common mode level) exceeds V_{CM}, the CMFB output voltage V_{CMFB} increases which in turn pulls the op-amp's differential outputs down. This negative feedback keeps the output common-mode level close to the require common-mode level V_{CM}. Here the diff-pair gain devices are made larger in size to increase the input common-mode range of the CMFB amplifier. But this topology fails for wide swing differential outputs as then the common-mode balancing breaks down.

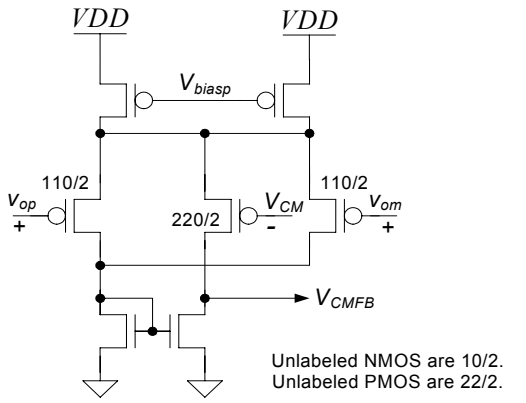

Figure 4-2. An example implementation of the three-input CMFB amplifier [1].

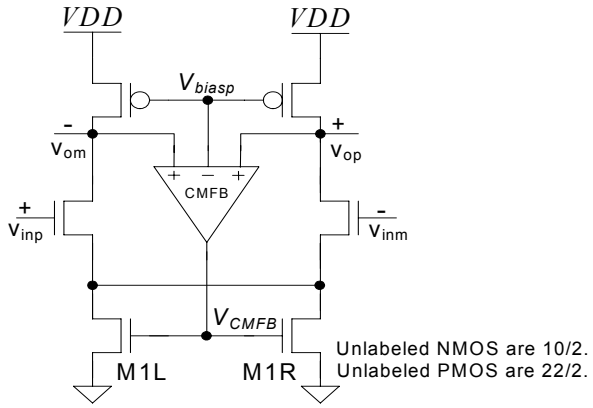

Figure 4-3. Use of a CMFB amplifier in setting the common-mode level of the output [1].

The CMFB loop also needs to be stabilized by employing appropriate frequency compensation. The compensation can be achieved by adding capacitors at the output of the CMFB amplifier, but it is convenient if the CMFB loop is compensated by the op-amp load itself as shown in Figure 4-1. It can be shown that the unity gain frequency of the CMFB loop can be given as [1]

$$f_{un,\,CM} = \frac{A_{CM} g_{md}}{2\pi C_L} \tag{4.1}$$

where g_{md} is the combined gm of the transistors M1L and M1R in Figure 4-3, and A_{CM} is the gain of the CMFB amplifier. For the CMFB loop to be stabilized with the output load C_L, we should have $A_{CM} \leq 1$, which implies that the gain of the CMFB amplifier should always less than or equal to unity [1].

A diode-connected load can be used instead of the current mirror load in the CMFB amplifier but then the output swing of such amplifier will be limited around V_{biasp}. Such a topology may not be desirable if the required common-mode level, V_{CM}, is not close to V_{biasp}[1]. A better approach to achieve low CMFB gain is to reduce the g_{md} associated with the common load loop. This leads to the condition

$$g_{md,\,CM} \leq \frac{g_{md}}{A_{CM}} \tag{4.2}$$

where $g_{md,CM}$ is the g_m associated with the common-mode loop [1].

Figure 4-4 shows a low-voltage, two-stage, fully-differential op-amp employing split-length diff-pair indirect compensation. Here a PMOS diff-amp is used as the CMFB amplifier. The CMFB amplifier controls the output common-mode level by varying the bias current in the first stage. A simplified block diagram for this CMFB topology is shown in Figure 4-9. The second stage is implemented as a class AB output buffer using the criss-crossed biasing discussed in [1]. A trioded NMOS device is used in the output branches of the topology. This trioded device lets the op-amp outputs swing freely without consuming large additional current. A pair of $30K\Omega$ resistors are used to track the average of the dif-

ferential outputs which is compared with V_{CM} using a two input CMFB amplifier. Two 100fF capacitors are added in parallel to the 30KΩ resistors for high-speed averaging. The two 30KΩ averaging resistors load the output-stage and may degrade the overall gain, and must be accounted for while designing the op-amp [1]. Figures 4-6 and 4-8 demonstrate the DC and step input response respectively for the two-stage op-amp. The DC gain (in Figure 4-9) is reduced and has dual peaks due to the CMFB affecting the bias for the second stage.

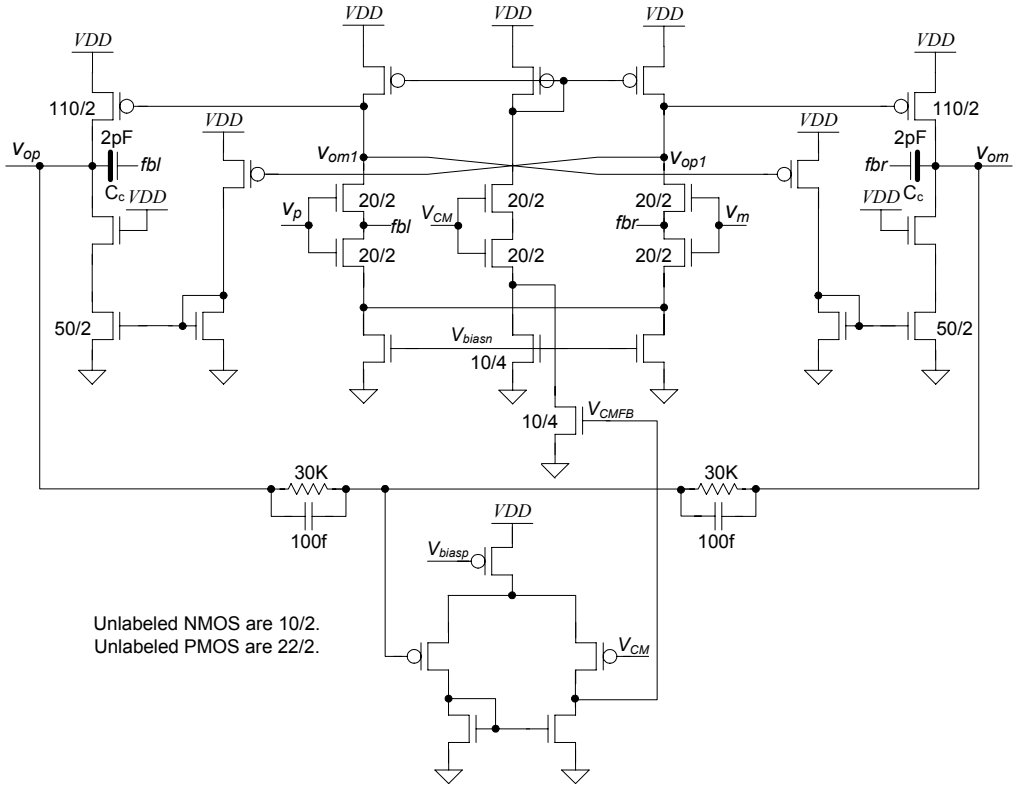

Figure 4-4. A fully-differential indirect compensated two-stage op-amp. The output common-mode level is maintained by controlling the current in the first stage [1].

The DC behavior of this op-amp topology, obtained by the simulation setup shown in Figure 4-5, is illustrated in Figure 4-6.

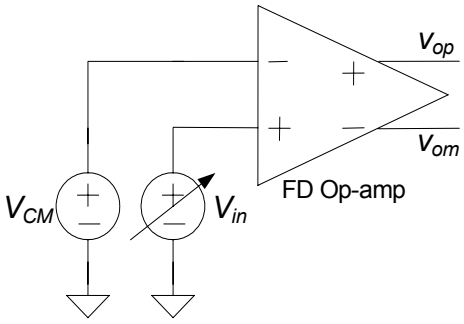

Figure 4-5. Simulation setup for ascertaining the DC behavior of the designed fully-differential (FD) Op-amp.

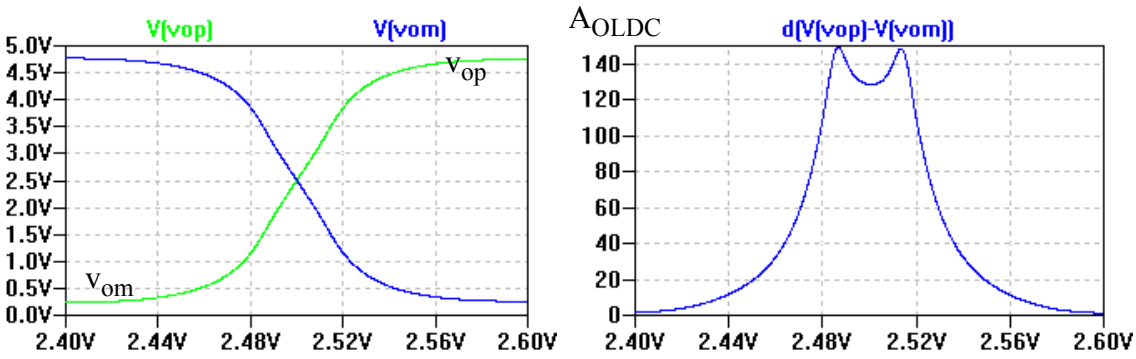

Figure 4-6. Simulated DC behavior and gain of the two-stage op-amp seen in Figure 4-4.

The stability of the fully-differential op-amps is generally shown by placing them in a Y-feedback topology with a gain of -1, as depicted in Figure 4-7 [1].

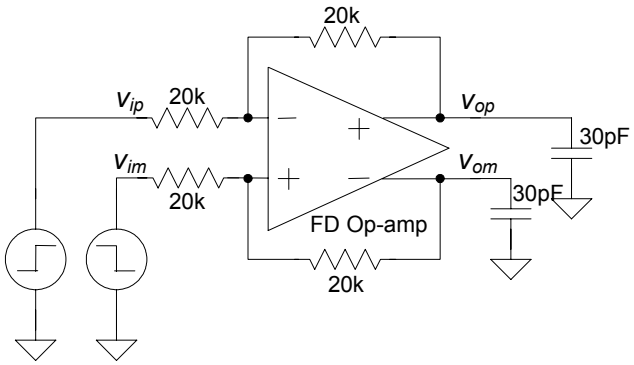

Figure 4-7. Simulation setup for obtaining the step input response of the designed fully-differential (FD) Op-amp.

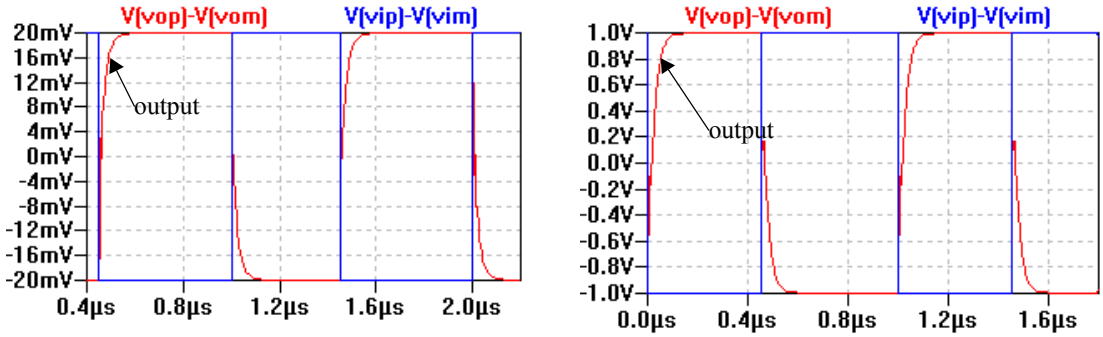

Figure 4-8. Simulated small and large step input response for the two-stage op-amp seen in Figure 4-4.

The gain of the CMFB amplifier (designed with AMI C5N process) used in fig 4-4 has a gain of 26, and thus it is difficult keep A_{CM} less than unity. Here the $g_{md,cm}$ is weakened by effective using one-sixth of g_{md}.

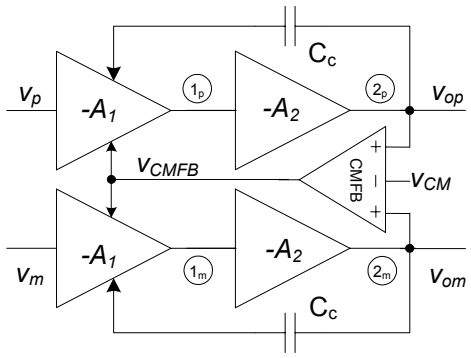

Figure 4-9. Block diagram for the op-amp topology shown in Figure 4-4. Here the output common-mode level is controlled by varying the current in the first stage.

Instead of incorporating a CMFB loop around the first and second stages as shown in Figures 4-4 and 4-9, we can maintain the output common-mode level by controlling the current only in the second stage, which is the output buffer in this case. The block diagram in Figure 4-10 shows the CMFB amplifier controlling the current in the second stage.

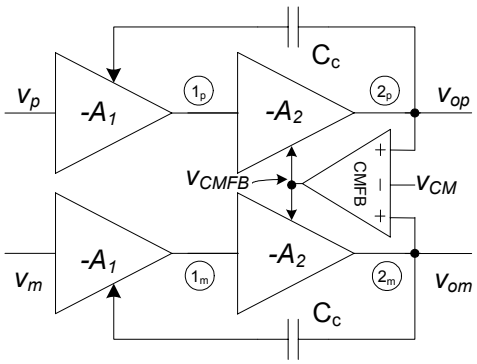

Figure 4-10. Block diagram of a fully-differential op-amp where the output common-mode level is maintained by controlling the current in the second stage (output-buffer).

Figure 4-11 shows a two-stage, fully-differential op-amp where CMFB is employed only in the output stage. This is accomplished by using trioded devices in the source of the NMOS pull-down device in the output buffer. The bottom 100/2 NMOS devices in the output buffer are sized up and biased such that they are always in triode region. The trioded devices provide the required relatively weaker control in adjusting the output common-mode level, without affecting the swing of the output buffer [1].

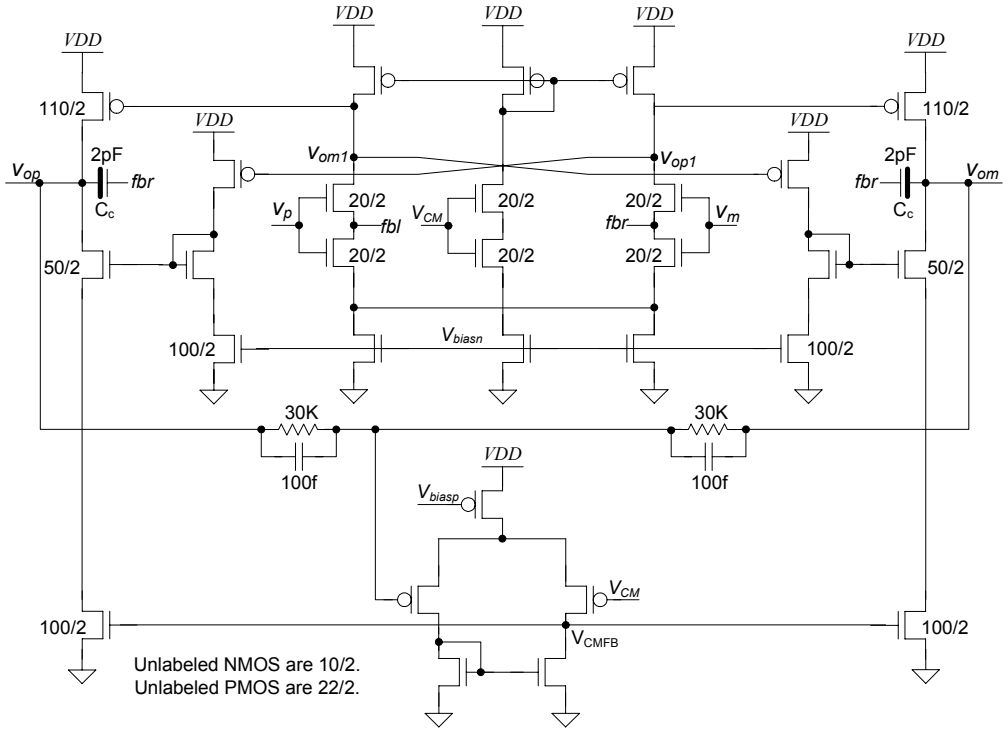

Figure 4-11. A fully-differential indirect compensated two-stage op-amp. The output common-mode level is maintained by controlling the currents in the output-stage alone [1].

Figures 4-12 and 4-13 show the DC behavior and the step input response respectively for the two-stage op-amp seen in Figure 4-11. The dc gain in Figure 4-12 is higher (800 here compared to 150 in Figure 4-6) when CMFB is used only in the output stage. This is due to the fact that the CMFB loop doesn't interfere in second stage biasing, and allows it to achieve the intended differential gain.

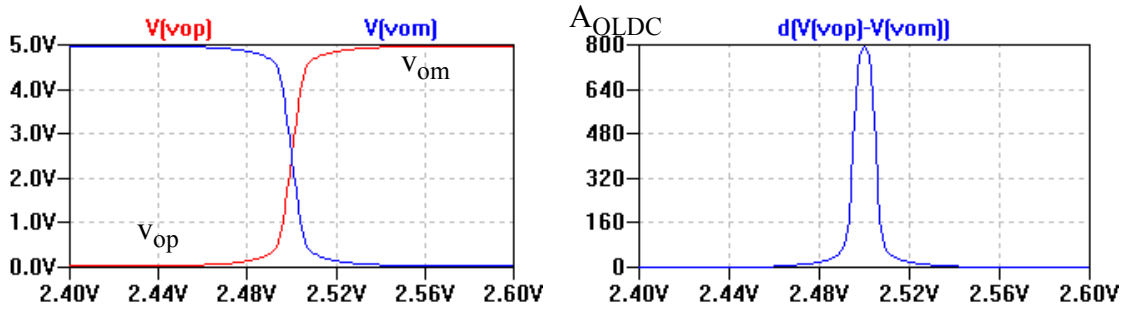

Figure 4-12. Simulated DC behavior and gain of the two-stage op-amp seen in Figure 4-11.

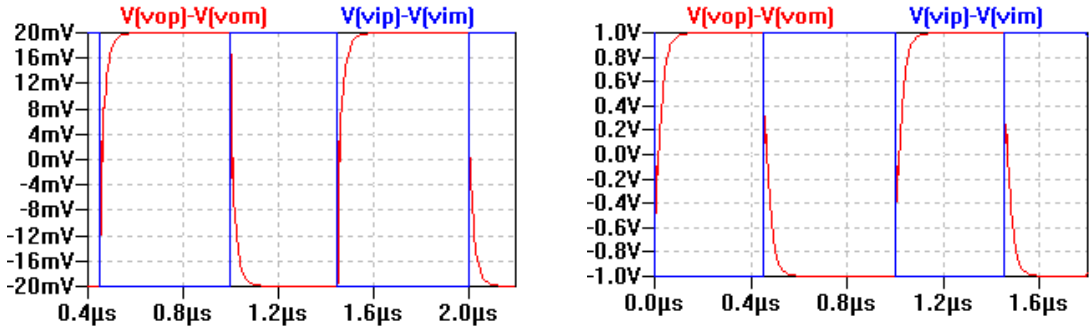

Figure 4-13. Simulated small and large step input response for the two-stage op-amp seen in Figure 4-11.

Although the op-amp topology seen in Figure 4-11 displays good performance, it is advisable to employ CMFB circuits around both the op-amp stages in presence of large off-sets [1]. In reference [1], switched capacitor CMFB is used to maintain the output common mode levels of both the stages. This idea is demonstrated in the block diagram shown in Figure 4-14. This topology is easier to implement using switched capacitor feedback, but it may not be suitable for low-voltage designs in sub 100nm processes. Here, we can use a three input CMFB amplifier for the first stage so that averaging resistors do not "kill" the open loop DC gain. Also since in feedback configuration the first stage output swing will be small, the three input CMFB amplifier will not require a wide input common-mode range. A resistor averaging two-input CMFB amplifier can be used around the second stage.

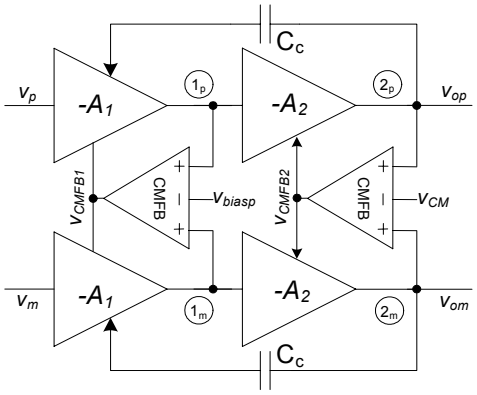

Figure 4-14. Block diagram of a fully-differential op-amp CMFB is used around both the stages.

Three-Stage Fully Differential Op-Amp Design

We can begin by extending the two-stage fully-differential op-amp design techniques to design a three-stage fully-differential op-amp. The first topology in the logical sequence is the one with a single CMFB loop around all the three stages as depicted in Figure 4-15. Topologies based upon this block diagram have been proposed in [30],[31] and [32]. Also [32] uses the RNMC compensation which is marked by the limitations discussed in Chapter 3 earlier. However, it can be observed through simulations that the CMFB loops disturbs the biasing of the second and third stages as the common mode level at node-1 and node-2 varies widely. This may affect the stability of the three stage opamp as g_{m2} and g_{m3} keep varying with V_{CMFB} and it may also introduce distortion due to variation of g_m's in the internal gain stage. Also when pole-zero cancellation is employed to stabilize the op-amp, variation in g_m's may lead to the breakdown of the compensation scheme.

Thus instead of using a CMFB loop across all the gain stages, it can be employed in the last two stages or just in the last gain stage. As the third stage (output buffer here) consists of power devices whose transconductance, g_{m3}, varies by order of magnitude while driving the load, variation in g_{m3} due to CMFB is not much of a concern. This design approach is demonstrated through the block diagram in Figure 4-16.

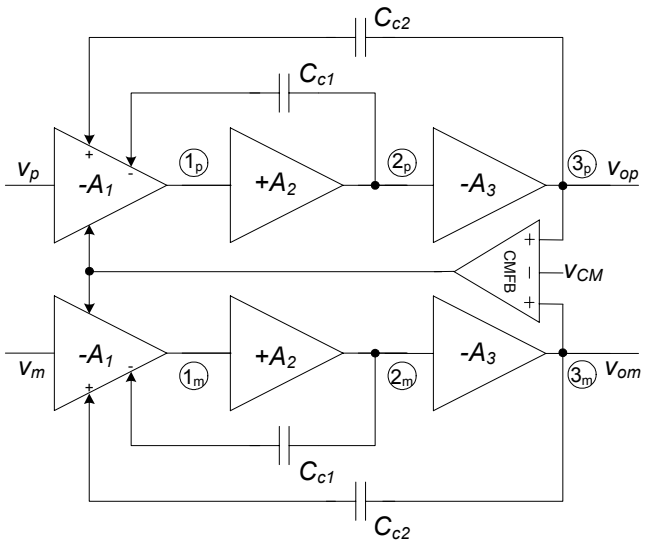

Figure 4-15. Block diagram of a three-stage fully-differential op-amp topology employing indirect compensation. This topology doesn't work well as the CMFB disturbs the biasing of second stage.

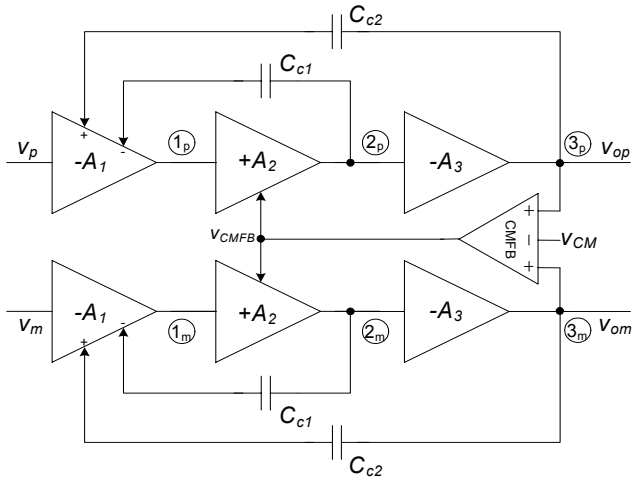

Figure 4-16. Block diagram of a three-stage fully-differential op-amp topology employing indirect compensation. The CMFB loop is wrapped around the last two stages so that the critical biasing is not affected.

Again, as implemented for the two-stage op-amp in Figure 4-11, the output common-mode level can be adjusted by controlling the current only in the output buffer. This design approach, depicted in Figure 4-17, is simple to implement and consumes lowest power of all the topologies.

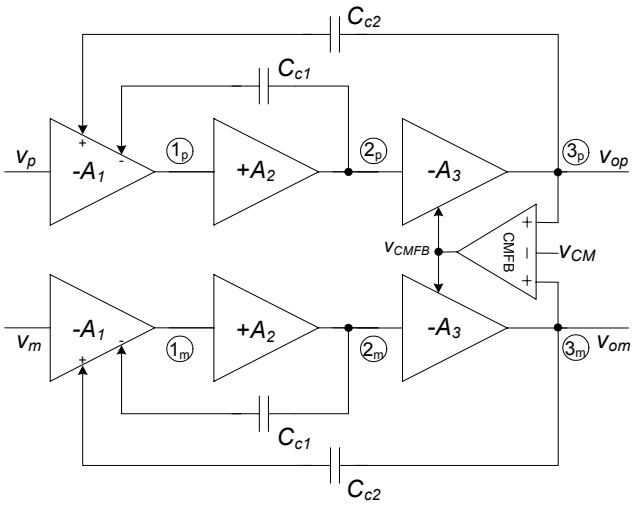

Figure 4-17. Block diagram of a three-stage fully-differential op-amp topology employing indirect compensation. CMFB loop is used around the third stage buffer and it doesn't affect the biasing of the internal stages.

Figure 4-18 illustrates the circuit implementation of the block diagram shown in Figure 4-17. This topology is been obtained by converting a Class A, singly-ended, three-stage op-amp, as seen in Figure 3-28, into its fully differential version by symmetrically laying out the gain stages. Then, the averaging resistors ($30K\Omega$ here) are accounted for in the third stage nodal resistance R_3, for estimating the open-loop dc gain and the small signal frequency response of the op-amp. The compensation network capacitors and resistors

values are updated for the new topology by applying the pole-zero cancellation equations 3.56 and 3.58. The compensation network values used in the circuit seen in Figure 4-18 are $C_{c1} = C_{c2} = 4pF$, $R_{1c} = 450\Omega$ and $R_{2c} = 950\Omega$. The differential open loop DC gain (A_{OLDC}) of this op-amp is around 12k or 81.6dB. Figure 4-20 demonstrates the simulated small and large step input response for this fully differential op-amp.

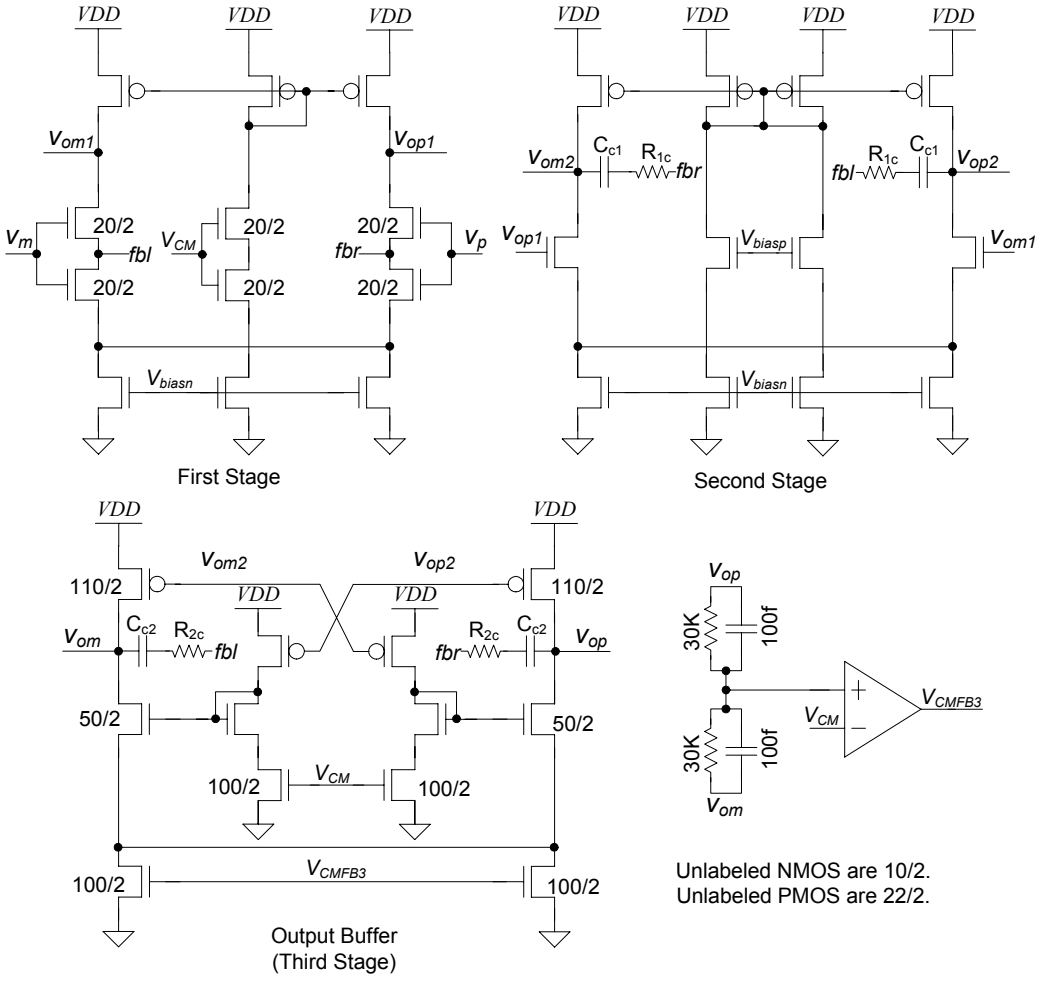

Figure 4-18. A fully-differential, indirect compensated three-stage op-amp implementing the block diagram shown in Figure 4-17. The output common-mode level is maintained by controlling the currents in the output-stage alone. Here, the circuit parameters for the compensation networks are $C_{c1} = C_{c2} = 4pF$, $R_{1c} = 450\Omega$ and $R_{2c} = 950\Omega$.

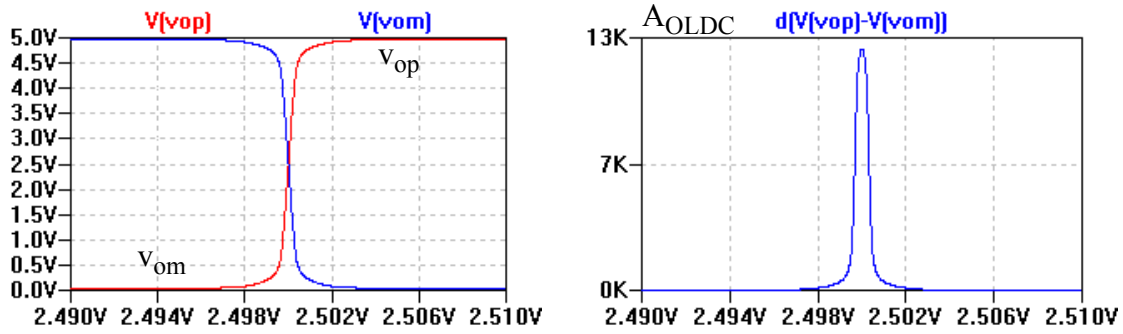

Figure 4-19. Simulated DC behavior and gain of the three-stage op-amp seen in Figure 4-18.

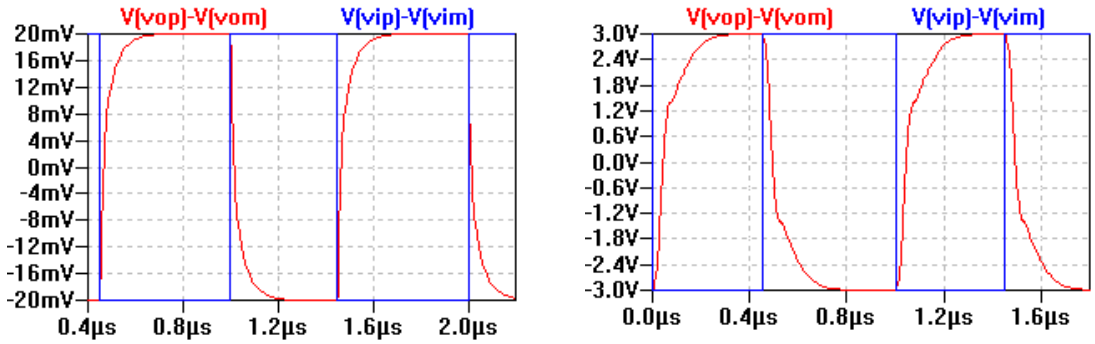

Figure 4-20. Simulated small and large step input response for the three-stage op-amp seen in Figure 4-18.

The most robust fully-differential amplifier design will be the one in which every stage has its own individual CMFB loop as shown in Figure 4-21. This topology consumes maximum power amongst all related topologies but performs best in presence of large off-sets. Again, here the internal CMFB amplifiers should be three-input diff-amps so that they do not load the internal gain stages. The CMFB amplifier used for the output buffer should use a two-input diff-amp with averaging resistors for larger input range of CMFB amplifier.

The block diagram in Figure 4-21 is shown for the case when the first and second stages are NMOS diff-amps, and the third or output stage is a class AB buffer. The respective CMFB loops set the outputs of the first, second and third stages to the required levels V_{bi-asp}, V_{biasp} and V_{CM} respectively. This arrangement may vary with the choice of gain stage topologies.

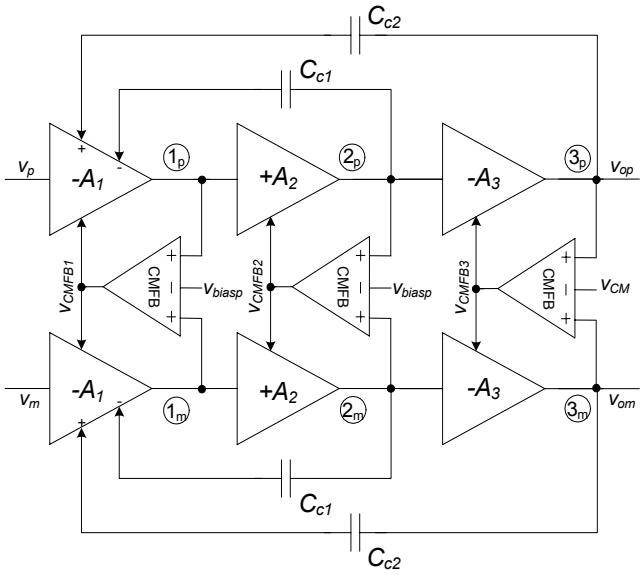

Figure 4-21. An example block diagram of a three-stage fully-differential op-amp topology employing indirect compensation. Three CMFB loops are used across each stage for robust operation in presence of large offsets.

Figure 4-22 illustrates the circuit implementation of the block diagram seen in Figure 4-21. The schematic in Figure 4-22 employs two NMOS diff-amps for the internal stages. The center sticks in each of the diff-amps are employed to set the bias for the next stages. Also CMFB loops are thrown around each of the stages for robust output common-mode level control. This topology is a fully-differential version of the single stage topology

presented in Figure 3-28. This widths of the devices in the output buffer have been increased to adjust for the loading by the averaging resistors.

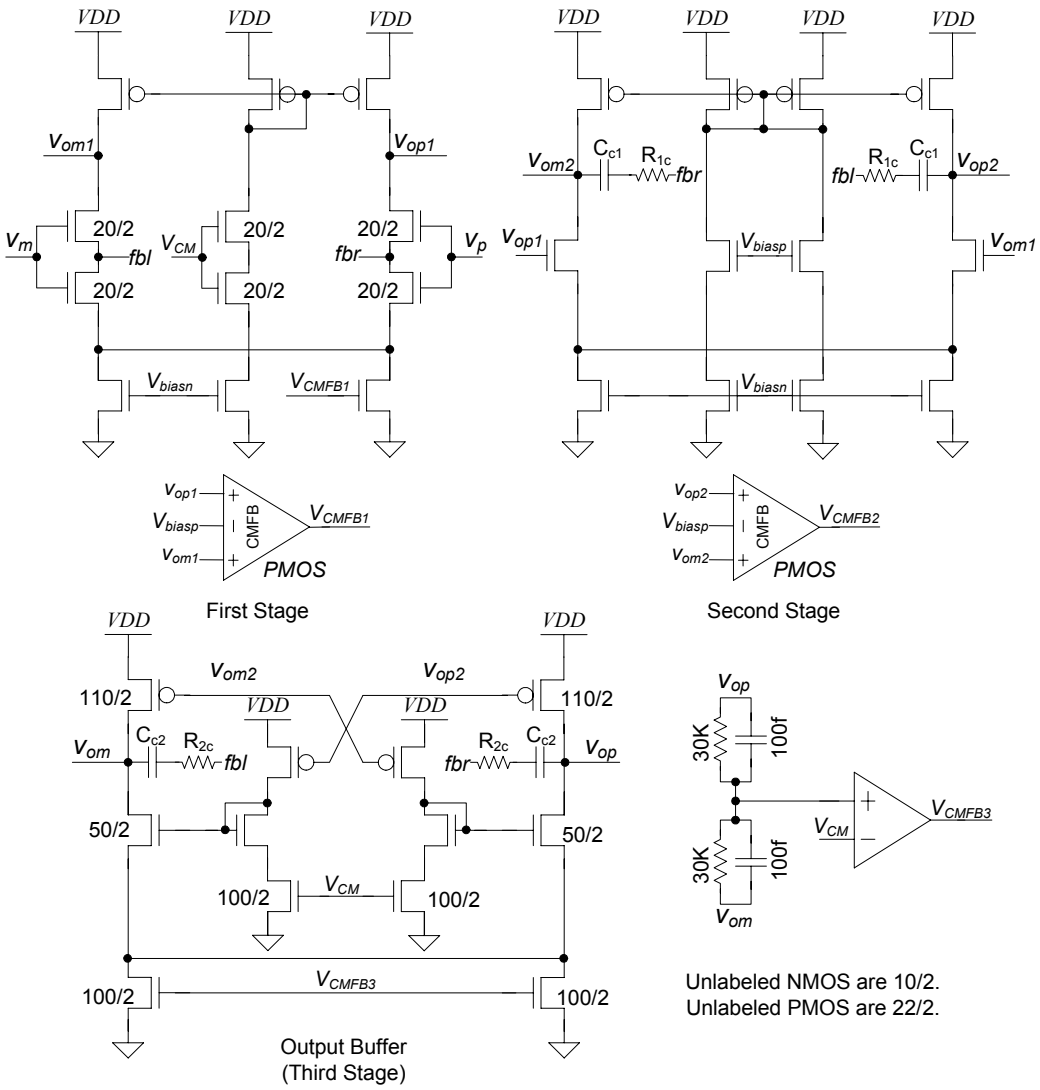

Figure 4-22. Implementation of the three-stage, pol-zero cancelled, fully-differential op-amp with the block diagram shown in Figure 4-21. Here three separate CMFB loops are used across each stage. Here, the circuit parameters for the compensation networks are, $C_{c1} = C_{c2} = 4pF$, $R_{1c} = 450\Omega$ and $R_{2c} = 950\Omega$.

The schematic here displays the different gain stages separately, but in the layout the gain stages devices must be laid out symmetrically about the vertical line passing through the first stage. The net power consumed in this op-amp topology, including the bias circuit, is given as $22 \cdot V_{DD} \cdot I_{bias}$.

Figure 4-23 presents another circuit implementation of the block diagram seen in Figure 4-17. The circuit is fully-differential version of the low power class AB three stage topology presented in Figure 3-37. The only difference between this circuit topology and the topology seen in Figure 4-11 is that instead of using the single-gain path criss-cross class AB buffer, the outputs of the first stage are used to obtain the class AB action in the output stage. However due to the use to two gain-paths the total harmonic distortion (THD) may be higher for this op-amp topology. The net power consumption in this topology is given as $17 \cdot V_{DD} \cdot I_{bias}$, which is the lowest amongst all the three-stage op-amp topologies presented to drive the requisite 30 pF load.

The schematic depicted in Figure 4-23 is drawn in a true to layout fashion. The gain stages are splitted around the first stage and laid out symmetrically to perfectly cancel the common-mode noise in the op-amp. Figures 4-24 and 4-25 demonstrate the DC and step input response respectively for this op-amp.

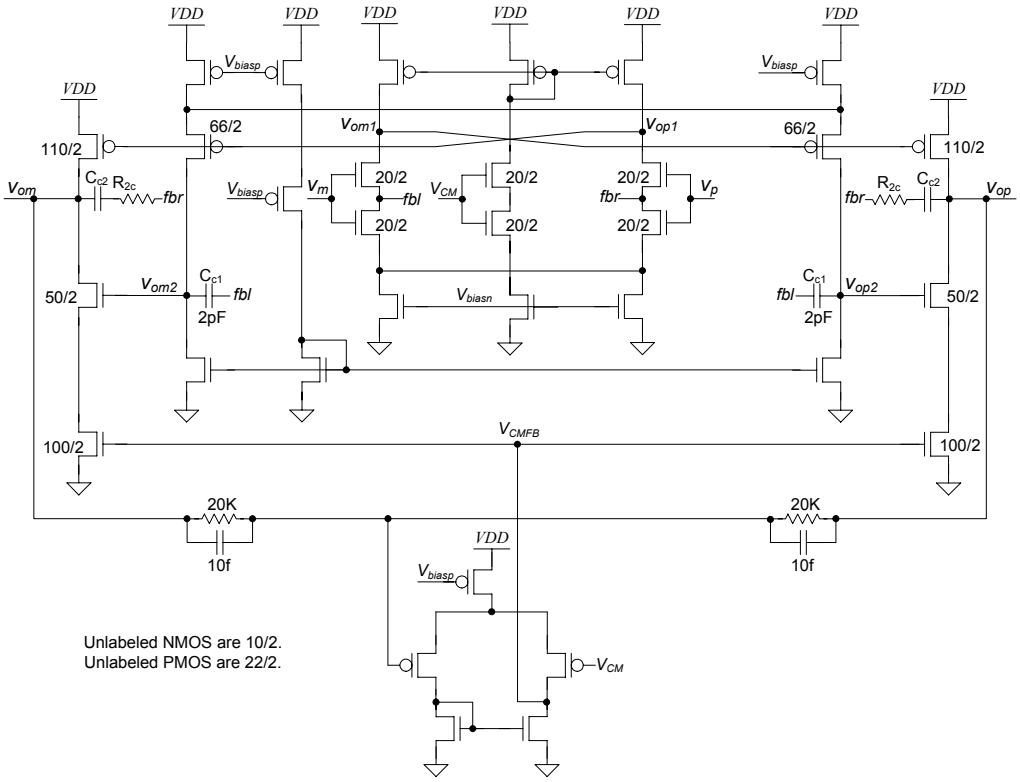

Figure 4-23. A low-power implementation of a three-stage, indirect compensated, pole-zero cancelled, fully-differential op-amp using two gain paths. The CMFB is implemented in the output buffer. The schematic is drawn symmetrically and can be directly translated into layout with same device placements.

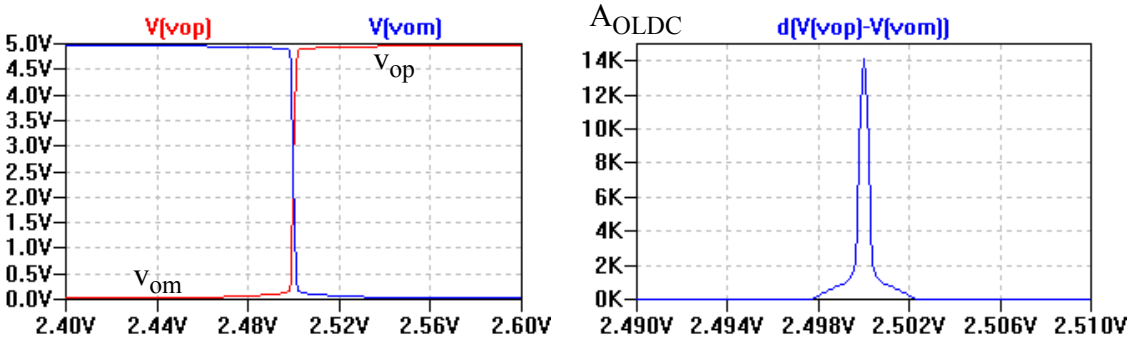

Figure 4-24. Simulated DC behavior and gain of the three-stage op-amp seen in Figure 4-23.

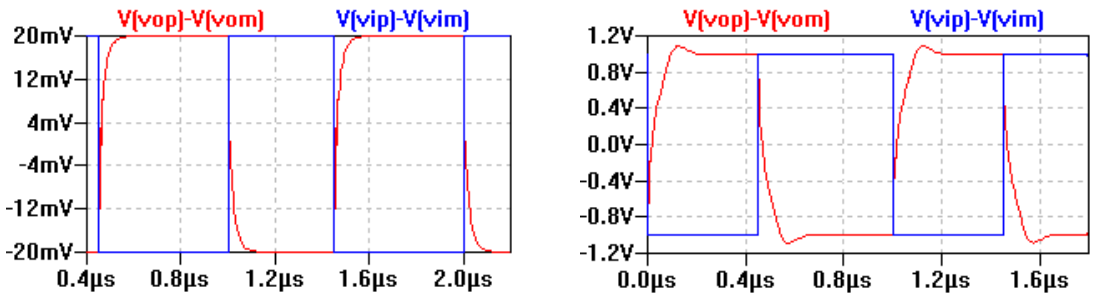

Figure 4-25. Simulated small and large step input response for the three-stage op-amp seen in Figure 4-23.

Another robust fully-differential three-stage op-amp topology is presented in Figure 4-26. Here, two single-ended differential amplifiers are used symmetrically to construct the second gain stage. One of the inputs of the second stage diff-amps are connected to the PMOS bias generated by the first stage, which should be same as V_{biasp}. The other inputs are connected to the differential outputs of the first stage. Because of the symmetry in the diffamps, the bias levels for second and third gain stages are precisely set. This scheme works well even in the presence of large offsets. Here, CMFB is implemented only for the output buffer.

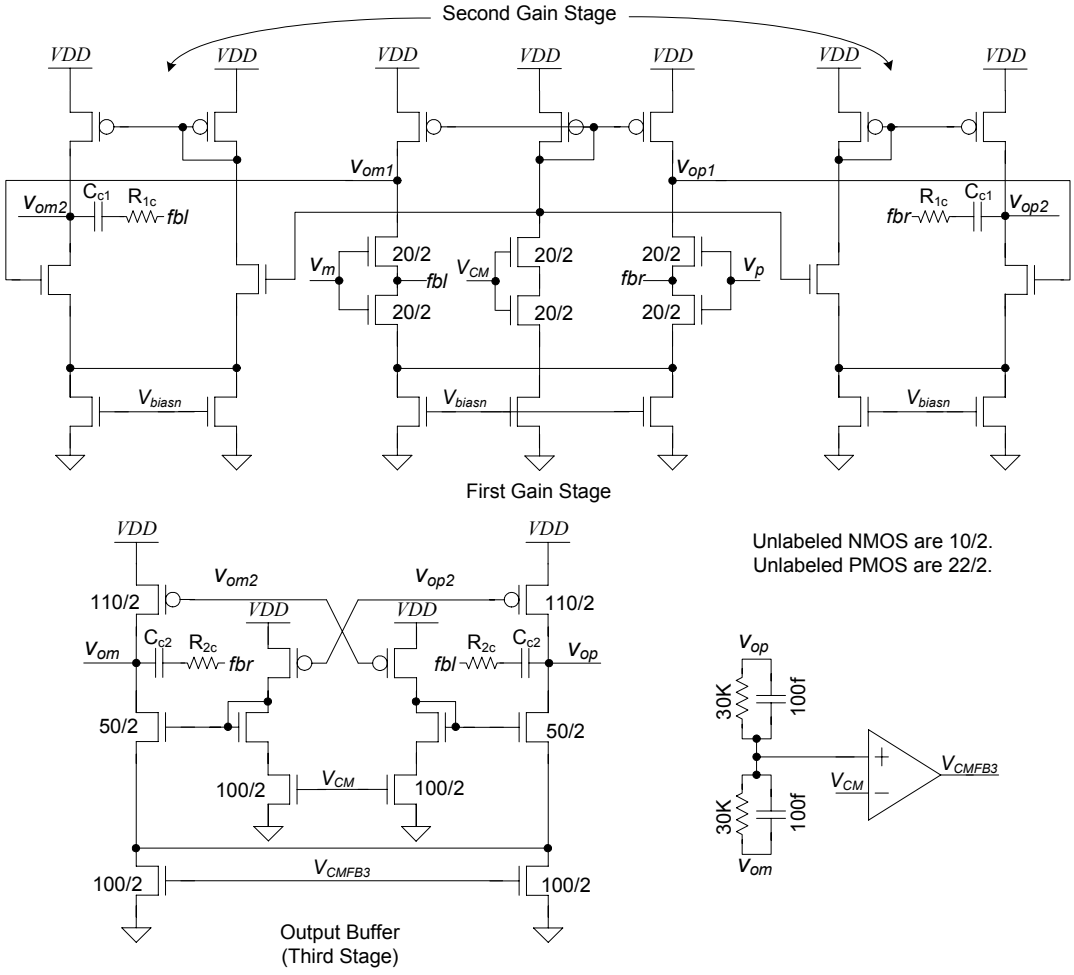

Figure 4-26. Another novel implementation of the three-stage, indirect compensated, pole-zero cancelled, fully-differential op-amp. Here the op-amp is designed so as to ensure that the second and third stages bias up correctly. The CMFB is employed only in the output buffer. This topology is also robust in presence of large offsets. Here, the circuit parameters for the compensation networks are $C_{c1} = C_{c2} = 4\text{pF}$, $R_{1c} = 450\Omega$ and $R_{2c} = 950\Omega$. This topology is henceforth referred to as RNIC-1-FD.

Figures 4-27 and 4-28 demonstrate the DC and step input responses respectively for the op-amp seen in Figure 4-26. This op-amp achieves an open loop differential gain of around 12k or 82dB in the $0.5\mu\text{m}$ CMOS process used. The small and large step input

responses also look clean with an approximate settling time of 200ns, which is considerably fast for a fully-differential op-amp driving 30pF capacitive load along with the 20kΩ feedback resistors. The total power consumption in this op-amp topology is $20 \cdot V_{DD} \cdot I_{bias}$, which is lesser than in the topology in Figure 4-22, where CMFB is used for all the three stages. This topology provides simple and robust fully-differential implementation with only one CMFB loop in the output stage.

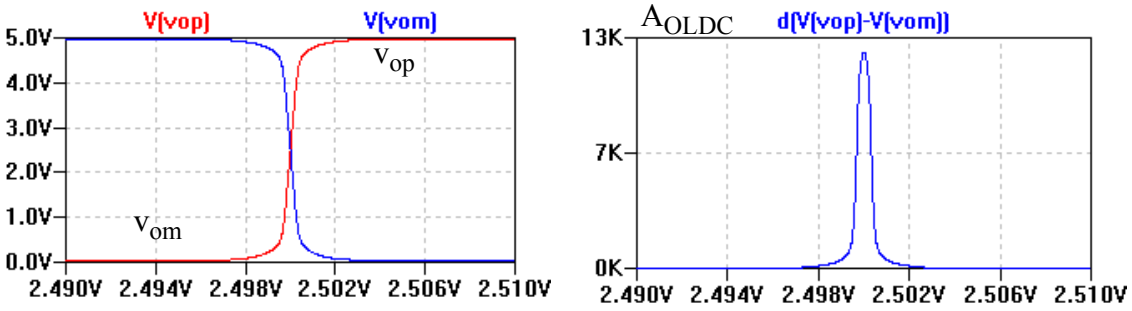

Figure 4-27. Simulated DC behavior and gain of the three-stage op-amp seen in Figure 4-26.

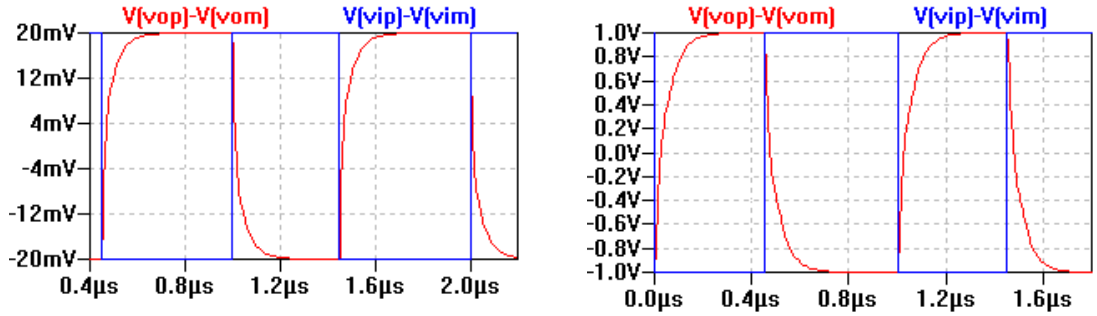

Figure 4-28. Simulated small and large step input response for the three-stage op-amp seen in Figure 4-26.

Performance Comparison

Again as in Chapter 3, a fully-differential indirect compensated opamp has been designed to drive the 500pF symmetric load for performance comparison. This topology is shown in Figure 4-29 and its frequency response is presented in Figure 4-30. The DC behavior of the opamp is displayed in Figure 4-31 which shows an open loop DC gain of 82.2dB.

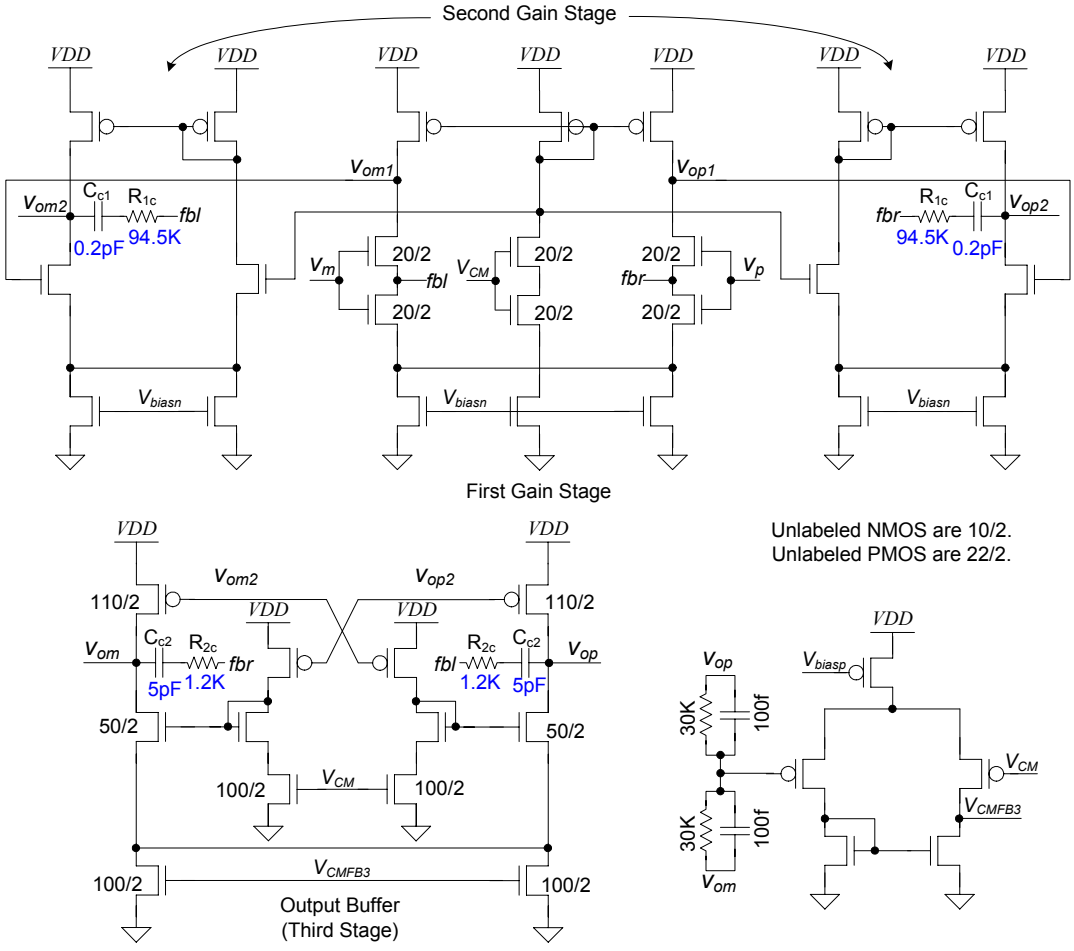

Figure 4-29. A three-stage, indirect compensated, pole-zero cancelled, fully-differential op-amp to drive 500pF load. Here, the CMFB is employed only in the output buffer. This topology is henceforth referred to as RNIC-2-FD.

The step input response of the designed op-amp is shown in Figure 4-32. The gain bandwidth of the op-amp is 20MHz and its settling time is around 370ns.

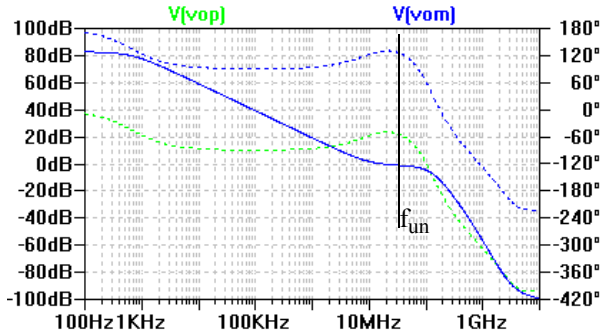

Figure 4-30. Frequency response for the fully-differential three stage op-amp seen in Figure 4-29. Here, the unity gain frequency, f_{un} is 20MHz.

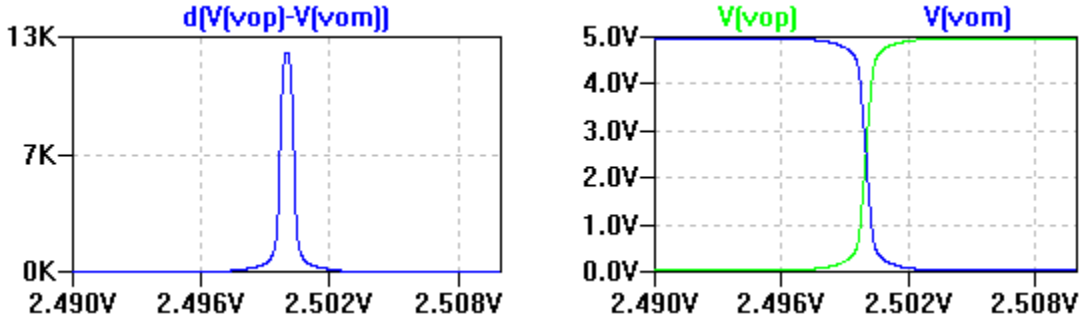

Figure 4-31. Simulated DC behavior and gain of the three-stage op-amp seen in Figure 4-29. Here, the open loop DC gain is 12K, or 82dB.

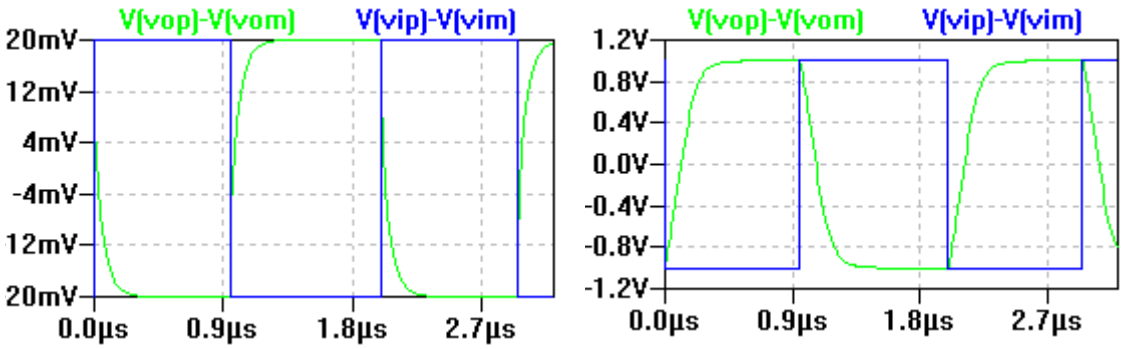

Figure 4-32. Simulated small and large step input response for the two-stage op-amp seen in Figure 4-29. Here, the settling time is 370ns.

Table 4-1 compares the fully-differential op-amp topologies presented in this chapter with the only practically demonstrated three-stage fully-differential op-amp found in literature i.e. the buffered RNMC topology in [32].

Table 4-1. Comparison of fully differential three-stage op-amp topologies [32]

Topology	C_L (pF)	V_{DD} (V)	I_{DD} (mA)	Power (mW)	f_{un} (MHz)	Avg. SR (V/µs)	C_{c1}, C_{c2} (pF)	t_s (ns)	FoM_S (MHz.pF/mW)	FoM_L (V/µs.pF/mW)
Buffered RNMC [32]	100	1.2	0.285	0.342	8.9	5.5	2, 0.65	2400	2602	1608
RNIC-1-FD (This work)	**30**	**3**	**0.4**	**1.2**	**12**	**10**	**4, 4**	**275**	**300**	**250**
RNIC-2-FD (This work)	**500**	**3**	**0.4**	**1.2**	**20**	**8**	**5, 0.2**	**370**	**8333**	**3333**

The topologies presented in this chapter are a significant advancement in low-voltage analog circuit design. Among all the fully-differential op-amp topologies reported in chapter, the op-amp topology seen in Figure 4-26 (or 4-29) is most suitable for application in high-speed, low-voltage, low-power data converter and analog filter design. Figure 4-33

shows a flowchart describing the procedure to design a fully-differential three-stage op-amp employing RNIC topology.

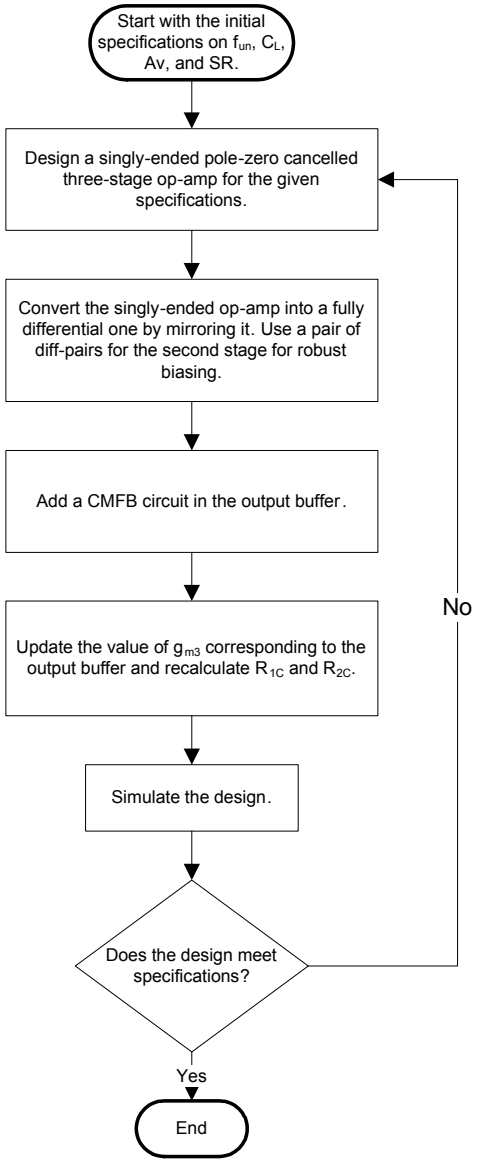

Figure 4-33. Flowchart illustrating the design procedure for a pole-zero cancelled, three-stage, fully-differential op-amp.

N-Stage Fully Differential Op-Amp Design

The design techniques developed for there-stage fully-differential op-amps, developed in the last section, can be easily applied to the generic n-stage op-amp scenario. Figure 4-34 shows a n-stage fully-differential op-amp topology where a CMFB loop is used in the output buffer (i.e. the n-th stage) to set the output common-mode level. Its recommended to employ diff-amps for inner gain stages, i.e. from first to (n-1)th stage, as in the op-amp topology seen in Figure 4-26 for robust biasing and low-power operation.

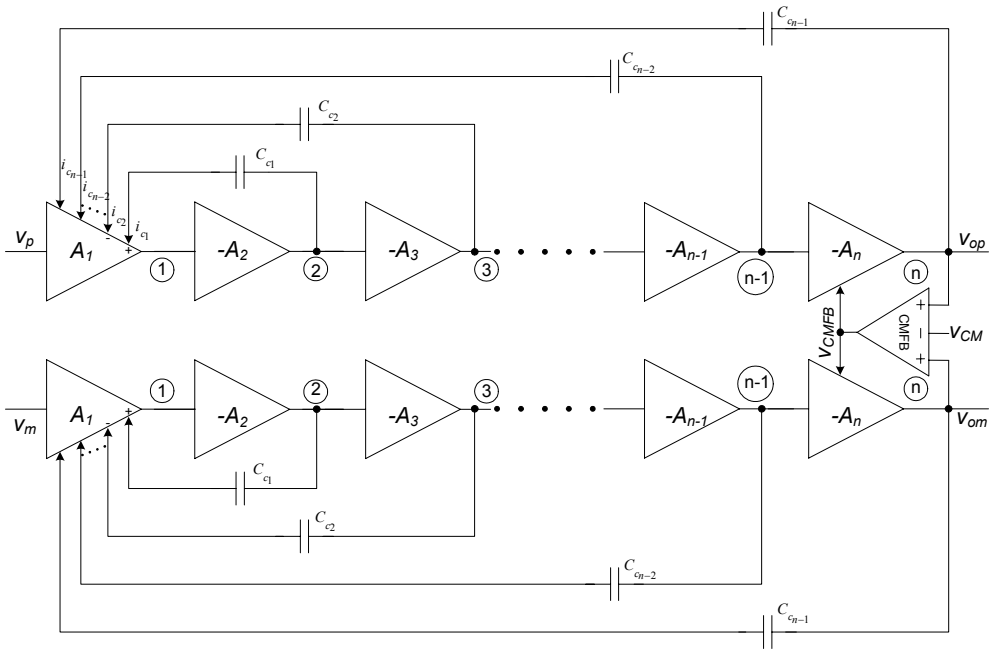

Figure 4-34. A simple implementation of N-stage, indirect compensated, fully-differential op-amp. The CMFB loop is used only around the last stage i.e. the output buffer.

Summary

A set of methodologies for the design of fully-differential three-stage op-amps have been presented. The three-stage fully-differential op-amp design uses the compensation schemes introduced in chapter 3 for singly-ended op-amps. In addition to the conversion of the singly ended op-amp topology to a fully differential one by mirroring, we need a common mode feedback (CMFB) circuit to set the output common mode level of the op-amp to a known voltage. This can be accomplished by inserting a CMFB circuits around the fully-differential gain path in many ways. Also the biasing of the intermediate gain stages is important in order to design the op-amp which is robust against large process off-sets. A fully-differential topology has been proposed which employs diff-amps as inner gain stages for robust biasing, and uses CMFB only in the output stage. This op-amp, designed in AMI's 0.5μm process, achieves a simulated gain-bandwidth of 20MHz, a gain of 82dB, exhibits 370ns settling time for an step input for a fully differential loads of 500pF each, and consumes only 1.2mW power for a supply of 3V. This is a more than three times improvement in performance over the state-of-the-art.

Finally, a scheme for constructing N-stage fully-differential op-amps has been introduced, which will enable design of op-amps with four or more gain stages.

CHIP DESIGN AND TESTING

A set of test chips have been designed to demonstrate the novel op-amp topologies illustrated in Chapters 2,3 and 4. As mentioned earlier in chapter 2, the test chips are designed in AMI's C5N 0.5μm process using the MOSIS fabrication service. The first test chip consists of the Miller and indirect compensated two-stage topologies along with a class AB three-stage op-amp. The first chip has been fabricated and successfully tested. The second test chip consists of six three-stage op-amp topologies has been fabricated and is presently getting packaged. Further to that, the third test chip consisting of fully-differential op-amp topologies discussed in Chapter 4 is in fabrication. Considering the enormity of material presented in this thesis, the test results for the second and third test chips are not covered in this dissertation. The results of the second and further test chips will be presented in the papers scheduled to be published, based upon this work.

Test Chip Layout

The test chips have been laid out using the Electric CAD system [34]. The Electric layout of the first chip is shown in Figure 5-1, and the chip micrograph is shown in Figure 5-2. All the three test chips have a die size of 1500μm by 1500μm and use a 40-pin pad-frame.

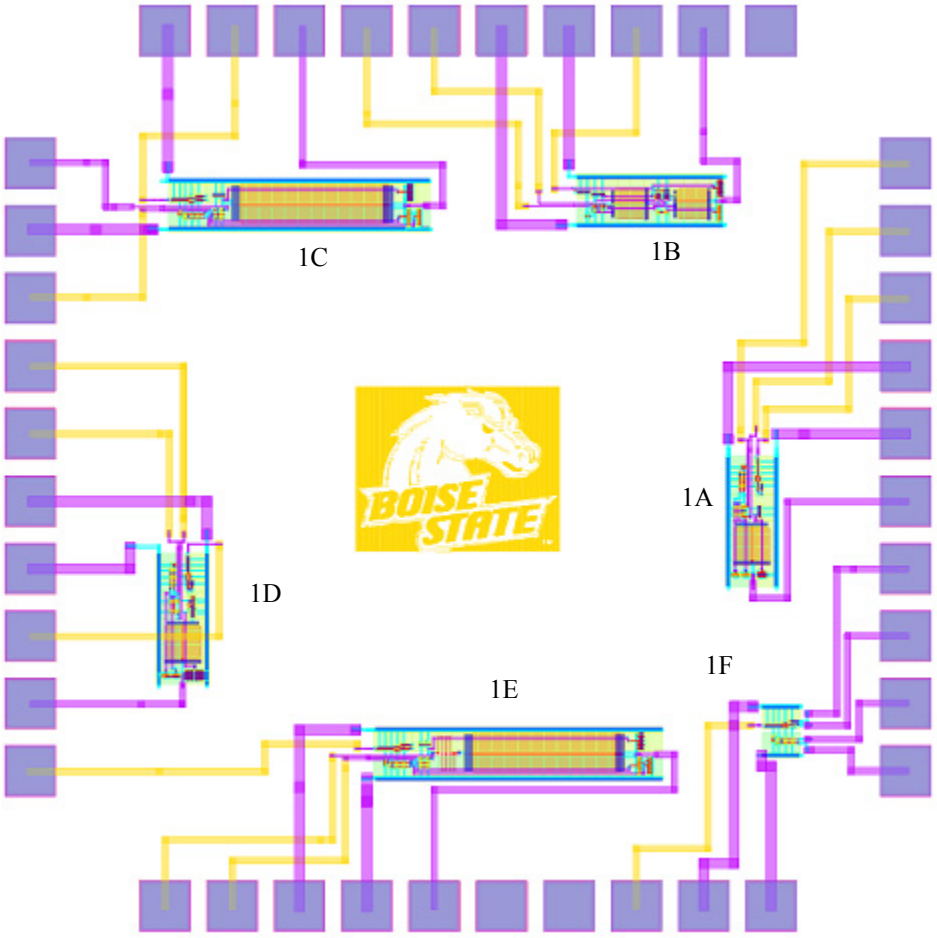

Figure 5-1. Layout view of the first test chip, showing the constituent circuits.

The test circuits included in the first chip are described in Table 5-1.

Table 5-1. Test circuit structures in chip 1.

ID	Circuit Description	Schematic
1F	Wide-swing cascoding bias circuit test structure.	Figure 2-7
1C	Miller compensated, two-stage op-amp to drive 30pF off-chip load.	Figure 2-5
1E	Miller compensated, two-stage op-amp with a zero-nulling resistor, to drive 30pF off-chip load	Figure 2-11
1D	Split-length load indirect-compensated (SLCL), two-stage op-amp to drive 30pF off-chip load	Figure 2-28

Table 5-1. Test circuit structures in chip 1.

ID	Circuit Description	Schematic
1A	Split-length diff-pair indirect-compensated (SLDP), two-stage op-amp to drive 30pF off-chip load	Figure 2-34
1B	Indirect-compensated, three-stage op-amp to drive 30pF off-chip load	Figure 3-45

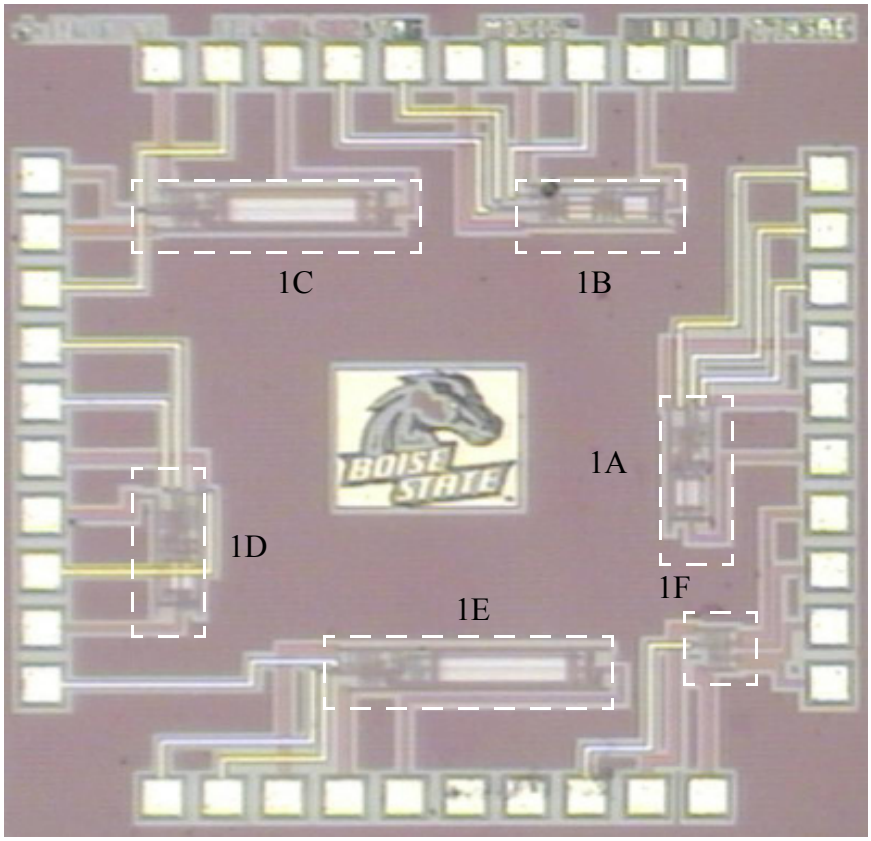

Figure 5-2. Micrograph of the first test chip, containing two-stage op-amps.

The individual circuits on the first test chip are illustrated in Figures 5-3 to 5-8.

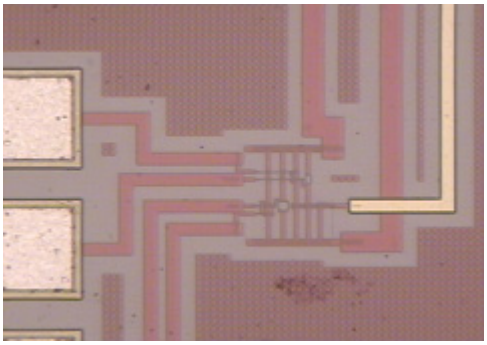

Figure 5-3. Micrograph of the bias circuit (1F).

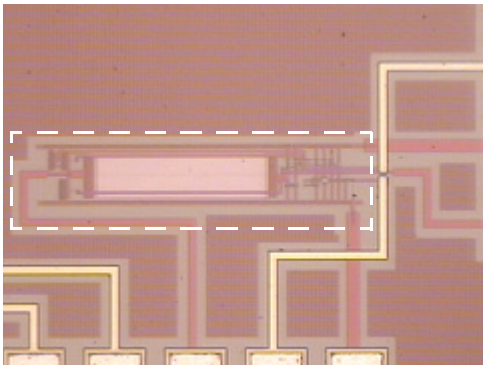

Figure 5-4. Micrograph of the Miller compensated, two-stage op-amp (1C).

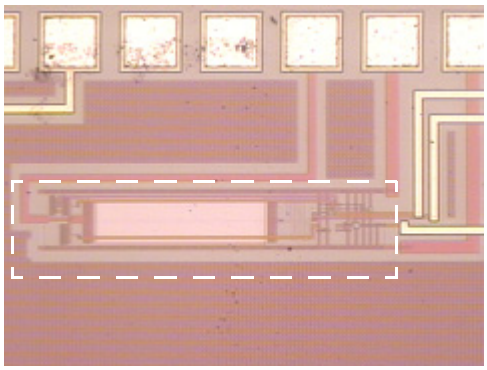

Figure 5-5. Micrograph of the Miller compensated, two-stage op-amp with zero-nulling R (1E).

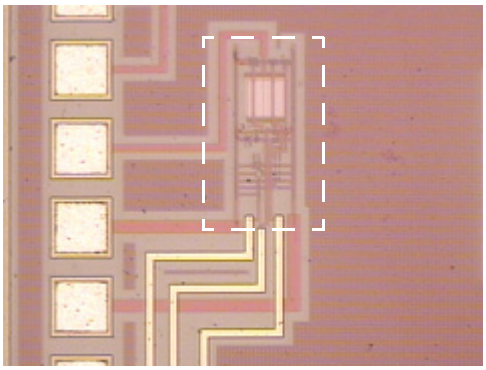

Figure 5-6. Micrograph of the split-L load indirect compensated, two-stage op-amp (1D).

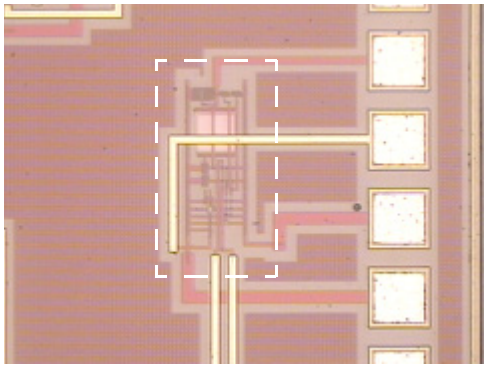

Figure 5-7. Micrograph of the split-L diff-pair indirect compensated, two-stage op-amp (1A).

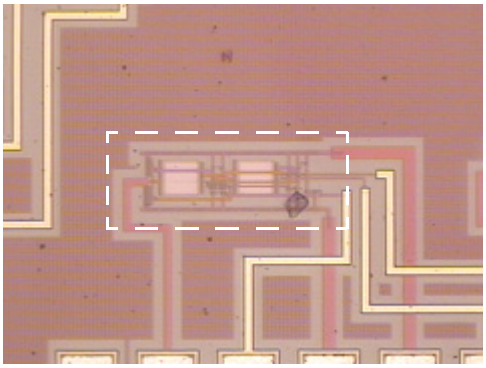

Figure 5-8. Micrograph of the indirect compensated, three-stage op-amp (1B).

The layout of the second test chip is shown in Figure 5-9. The test circuits to be fabricated on the second chip are described in Table 5-2.

Table 5-2. Test circuit structures in chip 2.

ID	Circuit Description	Schematic
2A	Indirect compensated, class AB, three stage op-amp with pole-zero cancellation, driving 30pF load.	Figure 3-37
2B	Indirect compensated, class A, three stage op-amp with pole-zero cancellation, driving 30pF load.	Figure 3-23
2C	Indirect compensated, class A, three stage op-amp without pole-zero cancellation, driving 30pF load.	Figure 3-34
2D	Low power, indirect compensated, class AB, three stage op-amp with pole-zero cancellation, with two gain paths, driving 500pF load.	Figure 3-50
2E	Low power, indirect compensated, class AB, three stage op-amp with pole-zero cancellation, with single gain path, driving 500pF load.	Figure 3-51
2F	High performance, indirect compensated, class AB, three stage op-amp with pole-zero cancellation, with two gain paths, driving 500pF load.	Figure 3-51

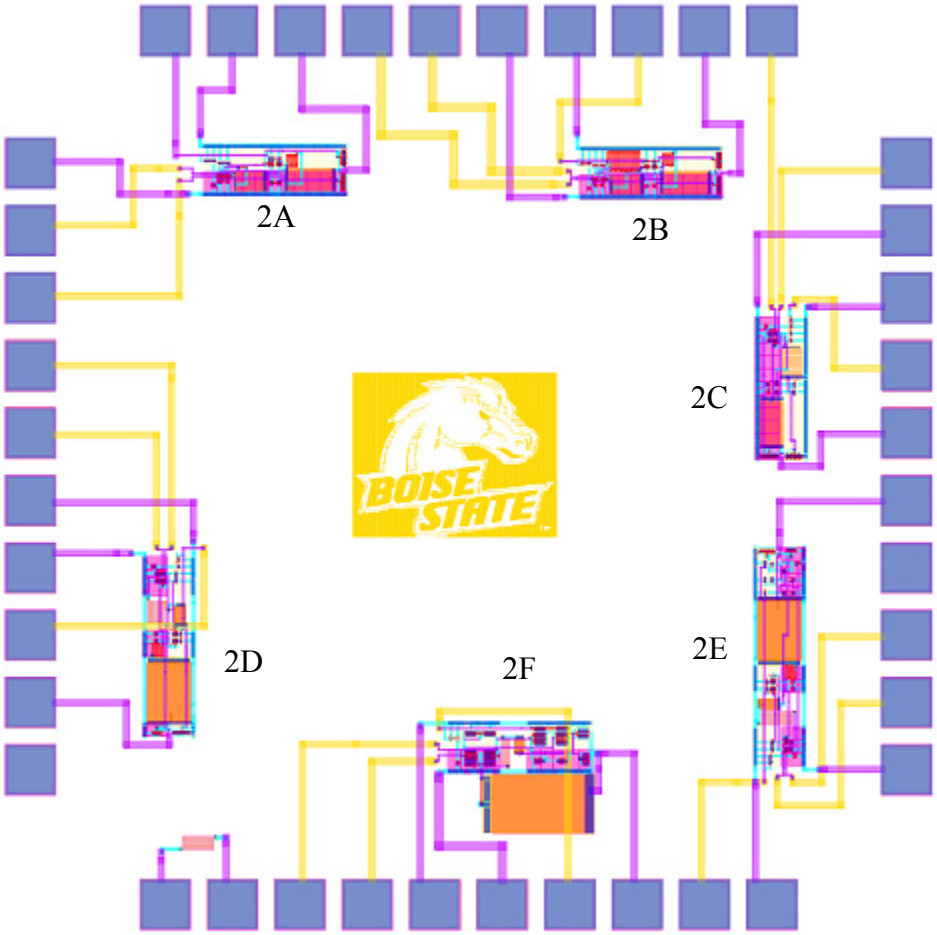

Figure 5-9. Layout view of the second test chip, showing the designed three-stage op-amps.

The test circuits on chip 3 are shown in Figure 5-10 and described in Table 5-3.

Table 5-3. Test circuit structures in chip 3.

ID	Circuit Description	Schematic
3A	Two stage, fully differential op-amp with CMFB across both the stages driving a 30pF symmetric load.	Figure 4-11
3B	Two stage, fully differential op-amp with CMFB only in the output buffer driving a 30pF symmetric load.	Figure 4-11

ID	Circuit Description	Schematic
3C	Three stage, fully differential op-amp with CMFB only in the output buffer driving a 30pF symmetric load.	Figure 4-18
3D	Three stage, fully differential op-amp with CMFB only in the output buffer (third stage) driving a 30pF symmetric load.	Figure 4-23
3E	Three stage, fully differential op-amp with CMFB only in the output buffer (third stage) driving a 500pF symmetric load.	Figure 4-29

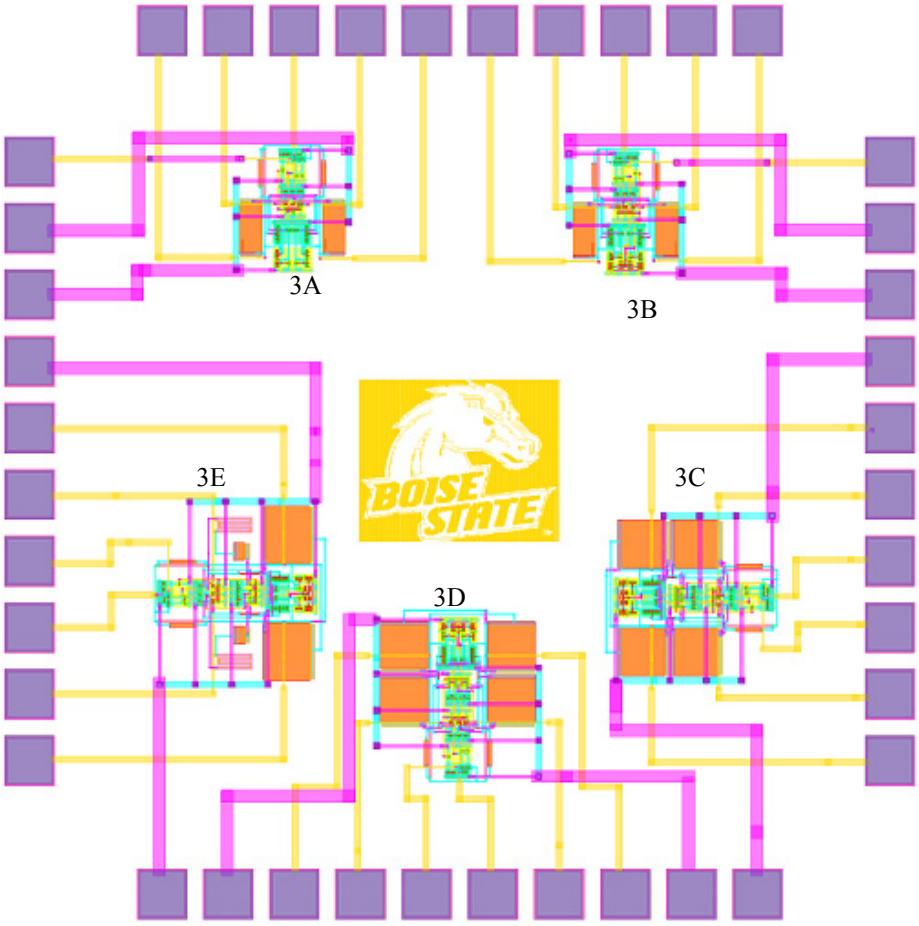

Figure 5-10. Layout view of the third test chip, showing the designed fully-differential two and three stage op-amps.

Chip Testing

The fabricated op-amp circuits are tested for their functionality by performing a step input response in follower (unity gain feedback) configuration. The simulated frequency and time domain responses for the designed op-amps have already been illustrated in Chapters 2 and 3. Figure 5-11 illustrated the test setup used for the op-amp step input response testing. A photograph of the physical test setup is shown in Figure 5-12.

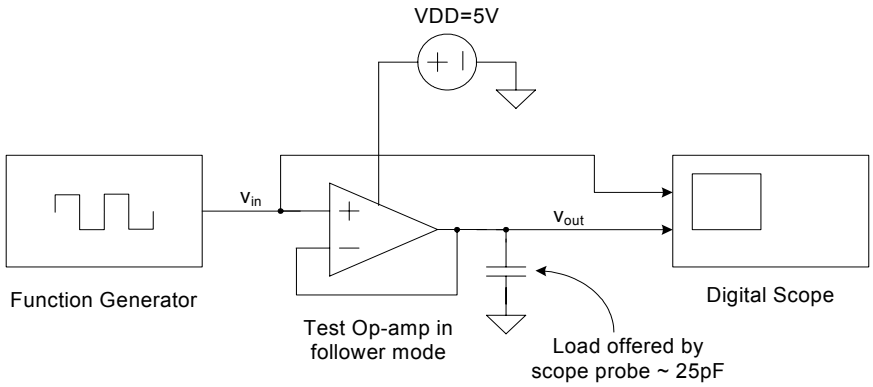

Figure 5-11. Block diagram showing test setup for step input response testing of the op-amps.

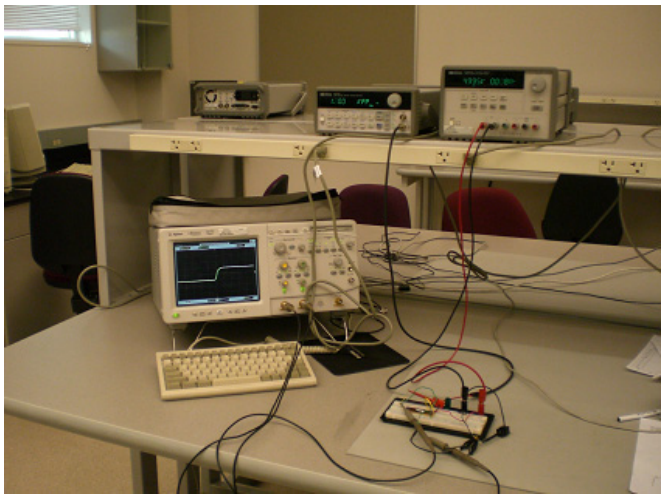

Figure 5-12. Test setup for testing of designed op-amp chip. The test-setup involves the device under test (DUT), a digital scope, DC power supplies and a function generator.

Figure 5-13 shows the fabricated chip under test. The chip has been bonded into a 40-DIP package and is breadboarded for testing.

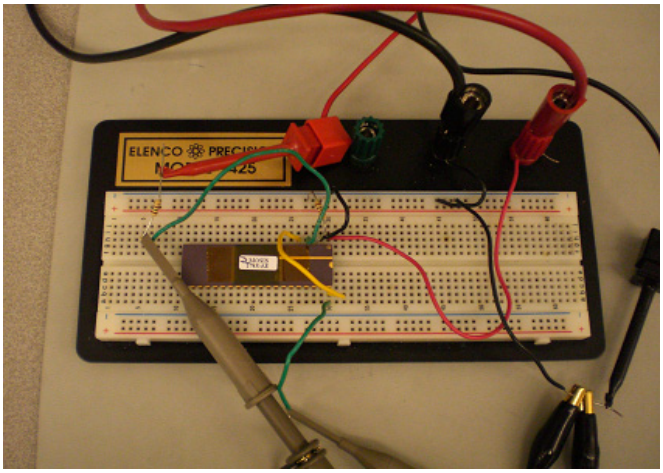

Figure 5-13. The test chip is bonded into a 40-pin DIP package which is bread-boarded for testing.

A function generator is used to generate a 100KHz square pulse train varying from 1.5V to 2.5V. A supply of 5V is used for the op-amp. A digital scope is use to view the input and outputs superimposed in the time domain.

The cascoding bias circuit (1F) was tested first and the output bias voltages were found to be in accordance with the simulated values in Figure 2-8. Figures 5-14 to 5-18 show the screen capture of the digital scope showing the op-amp settling times for the unity gain configuration. Since, the indirect compensated op-amps have settling times compara-

ble to the settling time of the input pulse, the observed settling times for the indirect-compensated op-amps are approximated.

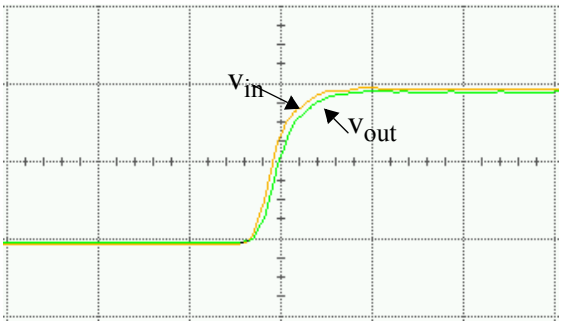

Figure 5-14. Large input step input response for the op-amp 1A (SLDP). Grid size is 50ns by 500mV. Measured settling time (t_s) is around 75ns.

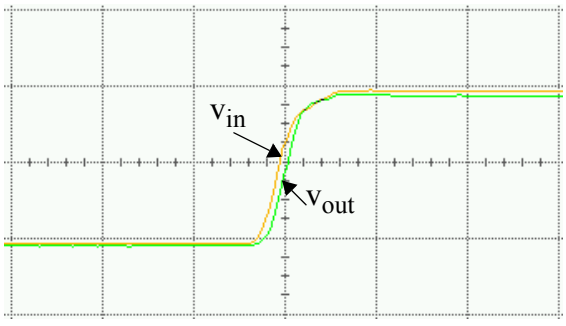

Figure 5-15. Large input step input response for the op-amp 1B (3-stage). Grid size is 50ns by 500mV. Measured settling time (t_s) is around 60ns.

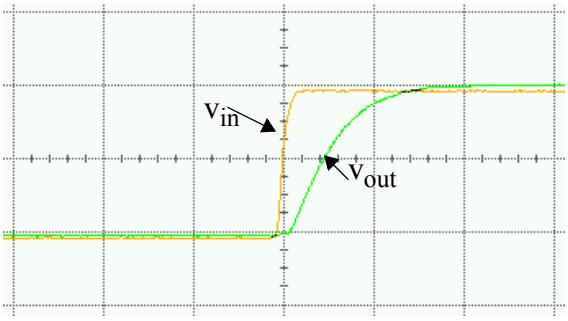

Figure 5-16. Large input step input response for the op-amp 1C (Miller). Grid size is 200ns by 500mV. Measured settling time (t_s) is around 270ns.

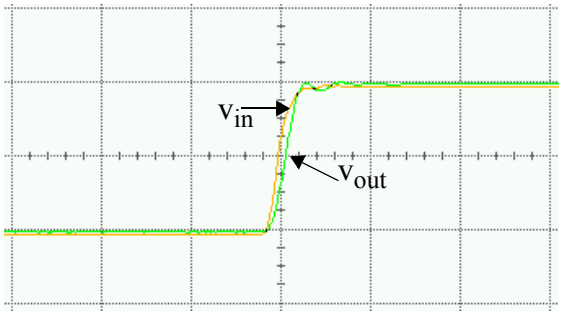

Figure 5-17. Large input step input response for the op-amp 1D (SLCL). Grid size is 50ns by 500mV. Measured settling time (t_s) is around 55ns.

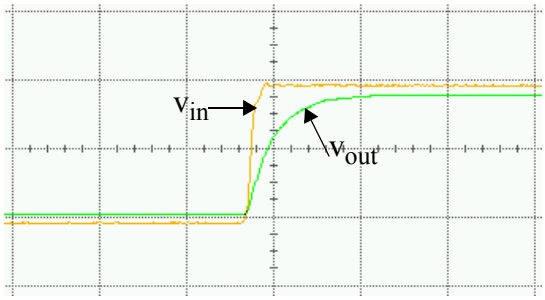

Figure 5-18. Large input step input response for the op-amp 1E (Miller with Rz). Grid size is 200ns by 500mV. Measured settling time (t_s) is around 250ns.

The test results for the op-amps on the first chip are tabulated in Table 5-4.

Table 5-4. Comparison of op-amp topologies in chip 1, designed to drive 30pF off-chip load.

Op-amp Topology	**DC Gain (dB)**	**GBW (MHz)**	**C_C (pF)**	**Phase Margin**	**Settling time (ns)**	**Power (mW)**	**Layout Area (mm^2)**
Miller compensated (1C)	57	2.5	10	74°	270	1.2	0.031
Miller compensated with zero nulling R (1E)	57	2.64	10	89°	250	1.2	0.034
Split-L load indirect compensated (1D)	66	20	2	75°	60	0.7	0.015
Split-L diff-pair indirect compensated (1A)	60	35	2	62°	75	0.7	0.015
Indirect compensated three-stage op-amp (1B)	88.6	19	1.5,1.5	76°	60	1.4	0.017

The test results re-affirm that Indirect Compensation can be used to obtain much faster op-amps with significantly lower power consumption and layout area, when com-

pared to the Miller compensated op-amps. Also, the test results are in close accordance with the simulations as expected for the fabrication process employed. Again, we re-iterate that the indirect-compensated two-stage op-amps exhibit ten times improvement in the gain-bandwidth and four times faster transient settling when compared to the Miller compensated op-amps. Also the indirect compensation results in 40% reduction in power and 50% reduction in the layout area of the op-amps. The encouraging test results for the indirect-compensated three-stage op-amp pre-validate the efficacy of the three-stage topologies by matching well with the simulated performance.

CONCLUSIONS

THE indirect feedback compensation technique, discussed in this dissertation, is a practical and superior technique for compensation of op-amps, and results in faster and low power op-amp topologies with significantly smaller layout area. The indirect feedback compensation technique can also be extended to op-amps with three or more gain stages. The two-stage op-amps employing split-length indirect feedback compensation and fabricated using 0.5μm CMOS technology demonstrate a ten times enhancement in gain-bandwidth and four times faster transient settling when compared to the Miller compensated op-amps. Also these op-amps consume 40% less power and occupy only 50% the layout area. Further, these op-amps perform reasonably well at 25% of the nominal supply voltage.

The three-stage op-amps utilizing indirect compensation and pole-zero cancellation can achieve excellent phase margins and stability. The three-stage op-amps, designed using pole-zero cancellation method, are fairly robust to large process variations in transistor devices, resistors and capacitors. The proposed compensation method alleviates many limitations of the conventional methods of designing multi-stage op-amps. The novel Reversed Nested Indirect compensated (RNIC) op-amp topology designed with the 0.5μm CMOS process drives a 500pF load with a unity gain bandwidth of 35MHz, consumes only 1.5mW power at 3V supply, with 70ns transient settling and 89dB gain. This is an over two times improvement in performance over the state-of-the-art. Also the proposed three-stage topology result in around 26dB higher gain with the same unity-gain frequency by consum-

ing only 20% more power and occupying the same layout area as the corresponding two-stage op-amp.

The compensation method developed for the singly-ended op-amps has been successfully extended to realize multi-stage fully-differential op-amp topologies. The fully-differential multi-stage op-amp design necessitates improvisation in common-mode feedback circuit. It was observed that the common-mode feedback, when used in multi-stage op-amp topologies, affects the open loop gain and the stability of the op-amp by varying the common-mode output level of the inner gain stages. This was overcome by using a topology which uses diff-amps as inner gain stages for robust biasing and by using common-mode feedback only in the output stage. This op-amp, again designed in 0.5μm CMOS process, achieves a simulated gain-bandwidth of 20MHz, a gain of 82dB, exhibits 370ns transient settling for fully differential loads of 500pF each, and consumes only 1.2mW power on a 3V supply. This is a more than three times enhancement in performance over the latest reported three-stage fully-differential op-amp. This performance demonstrated by the proposed three-stage fully-differential op-amp is suitable for design of data-converters and other signal processing circuits in low-voltage and low-gain sub-100nm CMOS processes.

The low-voltage, low-power op-amp design techniques, presented in this thesis can be used to construct high performance data converter, analog filters, and other signal processing circuits in the modern CMOS processes with low supply voltage and lower device gains. The techniques presented in this thesis should facilitate the integration of analog circuits in the modern low-voltage digital CMOS processes.

APPENDIX A

Matlab script for simulation of indirect-compensated, pole-zero cancelled, class AB three-stage op-amp shown in Figure 3-40.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Indirect Feedback Reverse Nested Compensation for
% Class AB Three Stage Opamp
% Vishal Saxena
% Boise State University
% Copyright 2007
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all; clc;
% Define the circuit symbols here
syms s vs v1 v2 vo s R1 R2 R3 Rc1 Rc2 gm1 gm2 gm3 C1 C2 Cc1 Cc2;
% Nodal Analysis Equations
eq1 = 'gm1*vs + v1/R1 + v1*s*C1 + v2/(1/(s*Cc1)+Rc1)- vo/(1/(s*Cc2)+Rc2)=0'
eq2 = '-gm2*v1 + v2/R2 + v2/(1/(s*Cc1)+Rc1) + v2*s*C2=0'
eq3 = 'gm3*v2 + gm3*v1 + vo/R3 + vo/(1/(s*Cc2)+Rc2) + vo*s*C3=0'
[v1,v2,vo]=solve(eq1,eq2,eq3,v1,v2,vo);

% Define DC gain
Av = gm1*R1*(gm2*R2+1)*gm3*R3;

% Get Num and Den
[n,d]=numden(vo/vs);
%pretty(sort(n)/sort(d));

% Extract the coefficients from Num and Den
n1=expand(n/Av);

b = sym2polys(n1,s);
pretty(b)

a = sym2polys(d,s);
pretty(a')

% Define SPICE circuit constants
```

```
gm1=170e-6; gm2=218e-6;gm3=1960e-6;
R1=160e3;R2=160e3;R3=19.5e3;
C1=10e-15;C2=17.2e-15;C3=30e-12;
Cc1=1e-12;Cc2=2e-12;


% Resistance attached to the low-Z nodes used for
% indirect compensation.
Rc0=1/(sqrt(2)*gm1);

% Apply pole-zero cancellation criterion
Rc2 = (Cc1/Cc2^2)*((C3+Cc2)/gm3);
Rc1 = C3/(gm3*Cc2) - 1/gm2;

format short e

% Substitute the constants
b_num=subs(b);
a_num=subs(a);
Av_num=subs(Av);

% Find pole and zero locations
z = roots(b_num)
p = roots(a_num)

% Define AC transfer function
H1=tf(Av_num*b_num,a_num);

% Plot Spectrum
figure(1)
h1=pzplot(H1);
setoptions(h1,'FreqUnits','Hz');

% Pole zero plot
figure(2)
h2=bodeplot(H1);
setoptions(h2,'FreqUnits','Hz');

% Calculate the values of resistors in series with
% the compensation capacitors
R1c = Rc1-Rc0
R2c = Rc2-Rc0
```

```
% Display the unity gain frequency
fun=gm1/(2*pi*Cc2)

% End of file
```

REFERENCES

[1] Baker, R.J., "*CMOS: Circuit Design, Layout, and Simulation,*" 2nd Ed., Wiley Interscience, 2005.

[2] The International Technology Roadmap for Semiconductors (ITRS), 2006 [Online]. Available: http://www.itrs.net/Links/2006Update/2006UpdateFinal.htm

[3] Zhao, W., Cao, Yu, "New Generation of Predictive Technology Model for sub-45nm Design Exploration" [Online]. Available: http://www.eas.asu.edu/~ptm/

[4] Grasso, A.D., Marano, D., Palumbo, G., Pennisi, S., "Improved Reversed Nested Miller Frequency Compensation Technique with Voltage Buffer and Resistor," *IEEE Transactions on Circuits and Systems-II, Express Briefs*, vol.54, no.5, May 2007.

[5] Baker, R.J., "*CMOS: Mixed-Signal Circuit Design,*" 1st Ed., Wiley Interscience, 1998.

[6] Gray, P.R., Hurst, P.J., Lewis, S.H., Meyer, R.G., "*Analysis and Design of Analog Integrated Circuits*," 4th Ed., John Wiley & Sons, 2001.

[7] Hurst, P.J., Lewis, S.H., Keane, J.P., "Miller Compensation Using Current Buffers in Fully Differential CMOS Two-Stage Operational Amplifiers," *IEEE Transactions on Circuits and Systems I- Regular Papers*, vol.51, no.2, Feb 2004.

[8] Ahuja, B.K., "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE Journal of Solid State Circuits*, vol.18, pp. 629-633, Dec. 1983.

[9] Saxena, V., and Baker, R. J., Indirect Feedback Compensation of CMOS Op-Amps, proceedings of the *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 3-4, April, 2006.

[10] R. J. Baker, "Design of High-Speed CMOS Op-Amps for Signal Processing," Invited Lecture, *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2005.

[11] Mahattanakul, J., "Design Procedure for Two-Stage CMOS Operational Amplifiers Employing Current Buffer," *IEEE Transaction on Circuits and Systems II- Express Briefs*, vol. 52, no. 11, Nov 2005.

[12] Chatterjee, S., Tsividis, Y., Kinget, P., "0.5-V Analog Circuit techniques and Their Application in OTA and Filter Design," *IEEE Journal of Solid State Circuits*, vol.40, no. 12, pp. 2373-2387, Dec 2005.

[13] Leung, K.N., Mok, P.K.T., "Analysis of Multistage Amplifier-Frequency Compensation," *IEEE Transactions on Circuits and Systems I, Fundamental Theory and Applications*, vol. 48, no. 9, Sep 2001.

[14] You, F., Embabi, S.H.K., Sanchez-Sinencio, E., "Multistage Amplifier Topologies with Nested Gm-C Compensation," *IEEE Journal of Solid State Circuits*, vol.32, no.12, Dec 1997.

[15] Hellums, J., "CMOS Amplifiers for Driving Speakers in Cell Phones," Talk given at University of Texas, Dallas, [Online]. Available: http://www.utdallas.edu/~hellums/docs/EE7329/Spring2007/UTSeminar06.pdf

[16] Palumbo, G., Pennisi, S., "Design methodology and advances in Nested-Miller compensation," *IEEE Transactions on Circuits and Systems I, Fundamental Theory and Applications*, vol. 49, no. 7, pp. 893-903, July 2002.

[17] Eschauzier, R.G.H., Huijsing, J.H., "A 100-MHz 100-dB operational amplifier with multipath Nested Miller compensation," *IEEE Journal of Solid State Circuits*, vol. 27, no. 12, pp. 1709-1716, Dec. 1992.

[18] Mita, R., Palumbo, G., Penissi, S., "Design Guidelines for Reversed Nested Miller Compensation in Three-Stage Ampifiers," *IEEE Transaction on Circuits and Systems II, Analog and Digital Signal Processing*, vol.50, no.5, pp. 227-233, May 2003.

[19] Zhu, F., Yan, S., Hu, J., Sanchez-Sinencio, E., "Feedforward Reversed Nested Miller Compensation Techniques for Three-Stage Amplifiers," *IEEE International Symposium on Circuits and Systems*, vol.3, pp. 2575-2578, May 2005.

[20] Leung, K. N., Mok, P. K. T., "Nested Miller compensation in low-power CMOS design," *IEEE Transaction on Circuits and Systems II, Analog and Digital Signal Processing*, vol. 48, no. 4, pp. 388-394, Apr. 2001.

[21] Leung, K. N., Mok, P. K. T., Ki, W. H., Sin, J. K. O., "Three-stage large capacitive load amplifier with damping factor control frequency compensation," *IEEE Journal of Solid State Circuits*, vol. 35, no. 2, pp. 221-230, Feb. 2000.

[22] Lee, H., Mok, P.K.T., "Active-Feedback Frequency-Compensation Technique for Low-Power Multistage Amplifiers," *IEEE Journal of Solid State Circuits*, vol.38, no.3, March 2003.

[23] Lee, H., Mok, P.K.T., "Advances in Active-Feedback Frequency Compensation With Power Optimization and Transient Improvement," *IEEE Transactions on Circuits and Systems I, Fundamental Theory and Applications*, vol.51, no.9, Sep 2004.

[24] Peng, X., Sansen, W., "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE Journal of Solid State Circuits*, vol. 39, no. 11, pp. 2074-2077, Nov. 2004.

[25] Peng, X., Sansen, W., "Transconductances with capacitances feedback compensation for multistage amplifiers," *IEEE Journal of Solid State Circuits*, vol. 40, no. 7, pp. 1515-1520, July 2005.

[26] Grasso, A.D., Palumbo, G., Pennisi, S., "Three stage CMOS OTA for large capacitive loads with efficient frequency compensation scheme," *IEEE Transactions on Circuits and Systems-II, Express Briefs*, vol.53, no.10, pp-1044-1048, Oct 2006.

[27] Ho, K.-P.,Chan, C.-F., Choy, C.-S., Pun, K.-P., "Reverse nested Miller Compensation with voltage buffer and nulling resistor," *IEEE Journal of Solid State Circuits*, vol. 38, no. 7, pp. 1735-1738, Oct 2003.

[28] Fan, X., Mishra, C., Sanchez-Sinencio, "Single Miller capacitor frequency compensation technique for low-power multistage amplifiers," *IEEE Journal of Solid State Circuits*, vol. 40, no. 3, pp. 584-592, March 2005.

[29] Grasso, A.D., Palumbo, G., Pennisi, S., "Advances in Reversed Nested Miller Compensation," *IEEE Transactions on Circuits and Systems-I, Regular Papers*, vol.54, no.7, July 2007.

[30] Pernici, S., Nicollini, G., Castello, R., "A CMOS Low-Distortion Fully Differential Power Amplifier with Double Nested Miller Compensation," *IEEE Journal of Solid State Circuits*, vol.28, no.7, July 1993.

[31] Xu, G., Embabi, S.H.K., "A Systematic Approach in Constructing Fully Differential Amplifiers," *IEEE Transaction on Circuits and Systems II, Analog and Digital Signal Processing*, vol.47, no.12, Dec 2000.

[32] Shen, Meng-Hung et al., "A 1.2V Fully Differential Amplifier with Buffered Reverse Nested Miller and Feedforward Compensation," *IEEE Asian Solid-State Circuits Conference*, 2006, p 171-174.

[33] Manoli, Y., "Tutorial on Continuous-Time Delta Sigma Data Converters," *IEEE Solid State Circuits Conference*, San Francisco, Feb 11, 2007.

[34] Electric VLSI CAD System [Online]. Available: http://www.staticfreesoft.com/productsFree.html